SynTest TurboBIST-Memory™ Tutorial

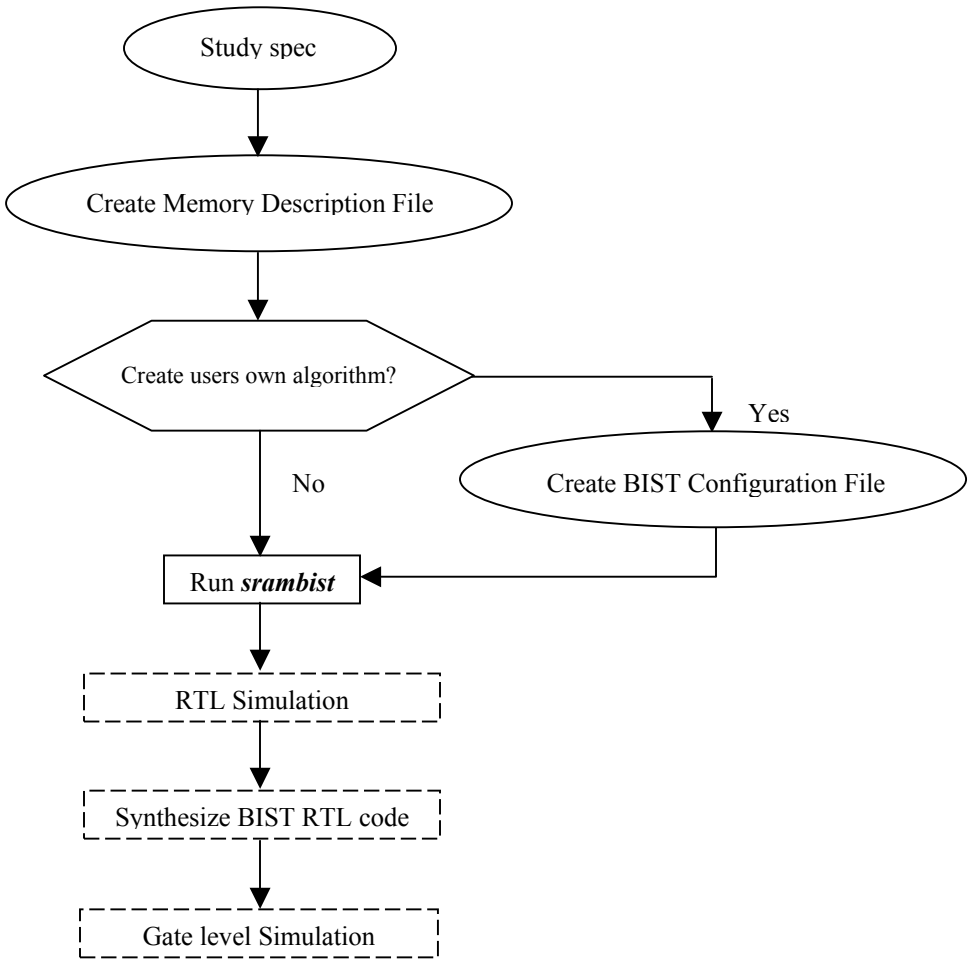
1. TurboBIST-Memory Capabilities

SynTest's TurboBIST-Memory generates Built-In- Self-Test (BIST) circuitry for embedded memory of SRAM or ROM types such that the memories embedded within a circuit can be tested at-speed from the circuit's Primary Inputs/Outputs. Only SRAM is included in this tutorial.

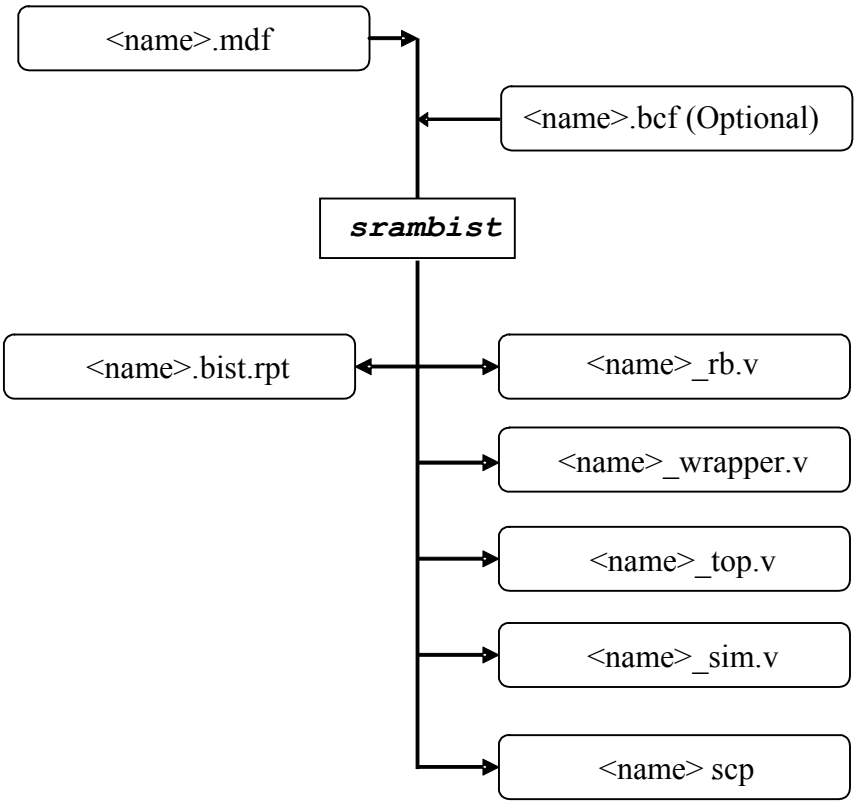
The tool for this tutorial includes only a subset of full-fledge features but the features are sufficient to demonstrate the following.

1. Offers at-speed BIST test for synchronous SRAM.
2. Uses Moving Inversion 13M March algorithm as a base for memory defect detection and identification.
3. Allows users to specify preferred algorithms.
4. Generates memory BIST logic in synthesizable RTL and associated test benches.
5. Allows up to two (2) memories (modules and/or instances) to share one BIST controller, and flexibility in grouping.
6. Automatic insertion of memory wrappers.

2. Tool Flow



2. srambist Input and Output Files



<name>.mdf	Memory description file
<name>.bcf	BIST configuration file
<name>_rb.v	BIST Controller RTL code
<name>_wrapper.v	Memory wrapper module.
<name>_top.v	Top module including BIST controller and memory wrapper.
<name>_sim.v	Simulation testbench file
<name>.scp	TCL script for Synopsys/Cadence Ambit synthesis
<name>.bist.rpt	Syntest BIST report file

3. Memory BIST for Single Port 256x8 RAMs

Here we use a set of single port 256x8 RAMs for this tutorial. First time users should familiar themselves with the Readme, the run script, and all the prepared files under the directories before invoking the run script. At the end of the run, users should examine tool-produced intermediate and output files to gain an understanding of the flow, operation and DFT technology. Advanced users can use –help in each software module to see other options available in the demo software.