==========

Readme File

SynTest Design-For-Test Software

Usage Description of Tool Options

SynTest Technologies, Inc.

September, 2006

==========

This package includes a demonstration version of SynTest TurboBIST-Logic tool. SynTest TurboBIST-Logic is a powerful and easy-to-use tool to implement Logic Built-In Self-Test (LBIST) for a circuit's core logic, an embedded core or an Intellectual Property core. The package includes one sample circuit, s382_s0, and the following prepared directories, files, and run script for users to try. Users are encouraged to study all the prepared material before running the tool. s382_s0 has three clocks and the tool will incorporate at-speed logic BIST into the circuit.

Restrictions for this demonstration software are as follows.

1) The port count of PRPG+MISR must be < = 100.
2) The clock domain count must be < = 3.

Prepared directories and files are as follows.

netsrc/ The original design netlist directory. In this demo, the design is a core logic with full scan implementation by TurboScan. See TurboScan documentation for more information.

simsrc/ The source of the original verilog simulation library.

libsrc/ In this directory, the original verilog simulation library in simsrc/ is remodeled into SynTest library. In the SynTest library files, remodeled text is listed under SYNTEST_TS keyword.

Note: As can be seen, the library sources and netlist are in different directories.

.map There are two sections in the mapping file. One maps non-scan flip-flops to their scan equivalent and the other shows "repairs" that need to be done when a DFT Rule Check (DRC) violation is found.

lbist.sc This is a design specific Logic BIST configuration script file if users choose to run commands in software module, lbconfig, in batch mode.

Run_BIST Run script for TurboBIST-Logic flow for the sample circuit.

The information below describes the software modules and options used in the run scripts.

[1] vlogin

Compile the library & netlist into SynTest database (sdb).

1. -define ifdef_cmd

    ex. -define SYNTEST_TS

    This tells vlogin that SYNTEST_TS sections in the library files contain the remodeled text.

    For example,
    ```
    `ifdef SYNTEST_TS
    …
    `endif
    ```

2. –lib <file>

    The file(s) given in <file> are the incoming library files and the compiled .sdb files. SynTest design data base files are redirected to the subdirectory lib/ if lib/ exists.

3. –o <path>

    Redirect output files to the specified <path> directory.

[2] expin

Expand the design database into SynTest primitive level.

1. -keepempty

    Use this option when there are empty cells in the design. If this option is not used, expin will try to expand such empty cells and a FATAL error will be generated.

2. -o <path>

    Redirect output files to the specified <path> directory.

[3] stil2dft

Generate SynTest .dft file from the STIL file.

Note: A .dft file, with ".dft" as its suffix contains DFT specification, is used.
Its updates are produced throughout the entire flow. Users should pay special attention to the .dft file(s) as it evolves.

1. -map_file

    Specify cell mapping file name. This map file maps cells in user's IC technology to SynTest primitives.

    Usage: -map_file <map_file_name>

2. -scan_mode

    Specify the scan enable signal.

    Usage: -scan_mode <port_name>

3. -test_mode

    Specify the test enable signal.

    Usage: -test_mode <port_name>

4. –o

    Name of the produced <top_module_name>.dft file and report files.

    Usage: -o <top_module_name>

[4] asic123

A testability analysis tool.

Usage: asic123 <sdb_name> [Options]

1. –o <path/output_file>

    Redirect output files to the specified <path> directory.

[5] scansyn

Performs scan synthesis to form scan chains.

1. –lbist <file>

   Do Logic BIST synthesis. Load and save Logic BIST information in <file>.lbist.

2. -extract_only

   Extract scan chain information from the scan synthesized netlist.

3. –o <file name>

   Output report saved in the file with prefix file name.

   Note: After the design goes through scan synthesis, using <top_module_name>.dft, a new .dft file, <top_module_name>_s#.dft is generated. For example, s382.dft now has a new updated file called, s382_s0.dft

[6] lbconfig

lbconfig can be set to interactive mode or a batch mode to describe Logic BIST configuration for a design. The specified results are saved in <top_module_name>.lbist by default.

1. bist.sc

   Design specific Logic BIST configuration script file if users choose to run lbconfig command in batch mode.

   The information below describes the commands used in the sample case.

   1.1 File I/O

   - load

     Load a Logic BIST configuration.

     Usage: load –design <top_module_name>

   - save

     Save Logic BIST configuration.

     Usage: save –o <Logic BIST configuration file name>

1.2 Define Logic BIST

- set_bist_mode
  This tool supports AT_SPEED in TurboBIST-Logic only. In AT_SPEED BIST mode, circuit captures twice to do at-speed testing of each clock domain.

  Usage: set_bist_mode AT_SPEED

- add_prpg
  lbconfig will insert PRPG for each clock domain automatically.

  Usage: add_prpg <PRPG_name>

- add_misr
  lbconfig will insert MISR for each clock domain automatically.

  Usage: add_misr <MISR_name>

- faultsim
  Do simulation to report fault coverage and calculate signature.
  BIST simulation stops when maximal number of patterns is eached.

  Usage: faultsim –pattern <maximum number of BIST patterns>

  Note : This option <-pattern> must be specified.

- lbgen
  This command is used to generate BIST wrapper and interface logic.
  The default BIST wrapper and interface file is
  TOP_Lb_<top_module_name>_s#.v.

  Note: Logic BIST controller logic is a black box. Only wrapper and interface signals are shown.

  Usage: lbgen –lbist <file>

- set_design
  Set design status.

  Usage: set_design SCAN_READY

[7] lbsim

Do fault simulation and get golden signature.

1. –lbist <file>

    Load and save BIST information in <file >.lbist to be used later by lbgen software module.

2. –o < file name>

    Output report saved in the file with prefix file name.

[8] lbgen

Create the BIST wrapper and interface for the sample circuit.

1. –lbist <file>

    Enable LBIST mode per information given in the <file>.lbist file produced by the lbconfig software module.

