Chapter 5

SIP Test Architectures
What is this chapter about?

- Introduce fundamental concepts and various aspects of SIP testing

- Focus on
  - Specific challenges from the testing point of view
  - Known-Good-Die
  - Solutions for testing a SIP at system level
  - Test and access of embedded dies

- Provide overview of SIP assembly and test technology
SIP Test Architectures

- Introduction
  - Definition
  - SIP examples
  - Yield and quality challenges
  - Test Strategy
- Bare Die Test
  - Mechanical probing techniques
  - Electrical probing techniques
  - Reliability screens
- Functional system test
  - Path-based testing
  - Loopback techniques: DFT and DSP
- Test of Embedded Components
  - SIP TAP
  - Interconnections
  - Digital logic and memories
  - Analog and RF Components
  - MEMS
- Concluding Remarks
What is an SIP?

System-in-package (SIP) = any combination of semiconductors, passives, and interconnects integrated into a single package

SIP (System-in-Package) is a functional system or subsystem assembled into a single package
**SIP vs. SoC**

- **SIP** is a **single package** that includes one or more **Integrated Circuits** and/or passive devices with multiple interconnections. It provides the option of combining multiple technologies to form a complete (sub-)system.

- **SoC** is a **single Integrated Circuit** connected inside a **single package** dedicated to a specific application.
Selection options: SIP vs. SoC

Factors to Consider:
- Production Volume
- Design & Market Environment
- NRE (Incl. IP Cost)
- Reliability
- Die Maturity
- Technologies (RF, Memories…)

Source: Gartner 2006
**SIP vs. SoC: so what?**

SIP and SoC are not competitors, but partners!

- **SIP**:
  - NFC
  - GPS
  - TVoM
  - DSC
  - MP3
  - BlueTooth™
  - Memory
  - Base-band
  - RF TRx
  - RF FE
  - PMU

- **SoC**:
  - NFC
  - GPS
  - TVoM
  - DSC
  - MP3
  - BlueTooth™
  - Memory
  - Base-band
  - RF TRx
  - RF FE
  - PMU

- **SIP**:
  - Health monitor
  - Wii-like
  - e-Compass

- **SoC**:
  - NFC
  - GPS
  - TVoM
  - DSC
  - MP3
  - BlueTooth™
  - Memory
  - Base-band
  - RF TRx
  - RF FE
  - PMU

A cell phone…

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Compared to an SOC, an SIP may have more…

SIP vs. SoC

Circuit Functions

Process Techno.

Suppliers

Quality Levels

Supply Voltages

Signal Frequencies

Signal Levels

Failure mod./mec.
SIP Platforms

Discretes Solutions

MCM Solutions

Laminate + SMDs Solutions

Laminate + SMDs + Passive die

Double Flip Chip assembly

Wafer Level Packaging

Integration Trend

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Leading Applications for SIPS

- Applications include portable consumer products such as 
  *digital camcorders and cameras*

- *Mobile phone* is the volume driver
  - Logic and memory combo
  - Digital baseband section
  - Transceiver section
  - RF section
This device is a credit-card sized digital camera with audio recording functions, an integrated MP3 player, 12MB of internal storage, and an SD or MMC card slot. Its thickness dimension is only 13.5 mm.
SIP examples

SIPs show up in portable devices

- The Sony DCS-T1, a 5MPixel camera, has the height and width of that of a credit card.
SIP examples

Camera Module & LCD Board

FBGA(L) 277pin
10x10x1.0t
P=0.50
Substrate 0.30 t
4layer(1+2+1)

ROHM QFN20pin
4.2x4.2x0.8t

FBGA(L) 111pin
10x11x1.4t
P=0.80
Substrate 0.15 t
2 layer

4 chips stacked
(3chips+1spacer)

SON 8pin
3x3x1.0t
P=0.65

Source: TPSS

The recently introduced E100 phone contains 4 complex mcps that illustrate the progress in mcp adoption over the past 3 years, and serves as an indicator of packaging trends.
SIP examples

Bluetooth
Radio

Stacked Integrated Passive die

Diodes

Laminate-based module
7.0mm x 8.0mm, Lamp2
Transceiver SiP building block
example, UAA3537 on PICS in HVQFN

Transceiver application diagram
- Supply: 8 capacitors, 1 resistor
- RF loop filter: 2 cap, 1 resistor.
- LNA matching: 4 cap, 2 ind
- Clock ref: 2 cap 2 resistor.

UAA3587GHN
Samsung GSM
TRx module
~25 mm²
to be packaged in
6x6mm² HVQFN
UAA3587 GSM multiband transceiver
Yield and Quality Challenges

Defect level:
\[ DL_i = \frac{F_{d_i}^{go}}{F_i^{go}} = \frac{F_{d_i}^{go}}{(F_{c_i}^{go} + F_{d_i}^{go})} \]

\[ Y_{SIP} = 100 \left[ P_1 \times P_2 \times \ldots \times P_n \right] \times P_s \times P_{int}^Q \times P_w \]

With \( P_i = 1 - DL_i \)

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Yield and Quality Challenges

\[
Y_{\text{SIP}} = 100 \left( P_1 \times P_2 \times \ldots \times P_n \right) \times P_s \times P_{\text{int}}^Q \times P_w
\]

Final yield = Multi-Die quality \times Assembly quality
Yield and Quality Challenges

In this example, with DL = 20000 ppm (i.e. 4100 ppm), SIP yield becomes 95.33%

<table>
<thead>
<tr>
<th></th>
<th>DLi (ppm)</th>
<th>Pi (%)</th>
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<tbody>
<tr>
<td>Substrate</td>
<td>600</td>
<td>99.94</td>
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<tr>
<td>Die 1</td>
<td>4100</td>
<td>99.59</td>
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<tr>
<td>Die 2</td>
<td>35500</td>
<td>97.45</td>
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<tr>
<td>Die 3</td>
<td>1200</td>
<td>99.88</td>
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<tr>
<td>$Y_{SIP}$</td>
<td></td>
<td>96.87</td>
</tr>
</tbody>
</table>
A Complex Test Flow...

Wafer Test

- Fab of X & PCM Test
- Fab of B & PCM Test

Final Test

- SiP Packaging
- SiP Final Test

System-level Test:
- DfT
- Fast Diagnosis and...
- Known-Good-Dies!

Known Good Dies!

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**Known-Good-Die**

**KGD Definition:**
(from a test perspective)

- Good enough to meet, at die level, at least the same quality level as a packaged IC

- Implies that:
  - **KGD test = WT + FT of a packaged die!!**

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A challenge for...

- RF
  - High-speed, high-res. Mixed-Signal
  - High pin-count digital (with small pad sizes)
**SIP Test Vision**

**Today:**
- Test of PCB
- Interconnects
- Passives
- Functional

**Future (w SIP):**
- Test of PCB
- Interconnects
- Passives (almost 0!)
  = Functional

**Test cost = 3U**

**Test cost = 4U**

**Test cost < 3U**

**Test cost << 4U**
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Bare Die Testing

- Objective = KGD quality

Because of probing limits.
RF Probing Challenges

**Package:**
- Wire bonding length

**Die under probes:**
- Needle length

**Bonding:** 1-3mm
**Leadframe:** mm size

**Probe tips:** 3-5mm

**Total Probe length:** 10-15mm

**Rule of thumb:**
- 10mm represent 10nH serial inductance
- impossible to test some devices @freq, or difficult correlation process!

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Thin film technologies for RF probing

Rule of thumb:
0.05mm represents less than 0.5nH serial inductance (typical 0.2nH specified)
MEMS technologies for RF probing

**KGD RF/MS**

- Springs for solder bumps
- Cantilevers for contact pads
- Length < 600 µm
- Width < 60 µm
- Thickness ~ 10 µm

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Signature-based Testing

- Power supply sweep
- I-V Signatures
- Multiple observation points
- Simple method
  - “black-box” methodology
- No functional testing
- Short test time
Non-contact die testing

Non-contact wafer probing eliminates scrubbing, while reducing the test cost, thanks to massive parallelism.

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Test at the System Level

SIP testing requires a greater diversity of ATE resources than SoC and leads to large disparities in test times and resource utilization among die.

**Solutions:**

✓ Insert in multiple testers (temporary acceptable, but not cost-effective!!!)
✓ Better scheduling of test resources to allow independent, simultaneous test of each accessible die in SIP (temporary acceptable, but not cost-effective!!!)
✓ BIST / DFT / DSP: still emerging in many areas!!!
Interim Test Points may affect signal integrity and leads to longer test times

**System Function Testing Issues**

So, what to do?
Test Rx and Tx paths independently

Pro:
- close to the application conditions
- two-pass test = reduced test time
- reduced risk of signal degradation

Contra:
- expensive ATE
- quality of contacts critical
- diagnosis??

Ref: “Seamless test of Digital Components in M/S paths”, S. Ozev et al.
Test Rx and Tx paths together (loopback)


Pro:
- low-cost (no?) ATE
- benefit from passive substrate
- test simulation
- easier BIST implementation

Contra:
- need DFT (not a simple short-circuit!)
- correlation with lab measurements
- mgt of yield / test escapes
- diagnosis??

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Loopback starts at the beginning

External loopback

G. Srinivasan, et al.
VTS 2006

Internal loopback

J. Dabrowski, J.G. Bayon
ISDFTVS 2004

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Die Access: SIP Test Access Port

Solution for end-user: SIP-TAP
F. de Jong, A. Biewenga
[ITC 2006]
Exploitation of boundary-scan resources

Specific test strategy for intermediate testing

<table>
<thead>
<tr>
<th>Step</th>
<th>Instruction Die 1</th>
<th>Instruction Die 3</th>
<th>Test vector</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>Reset</td>
<td>Reset</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>PRELOAD</td>
<td>PRELOAD</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>EXTEST</td>
<td>EXTEST</td>
<td>Vector #1</td>
</tr>
<tr>
<td>4</td>
<td>EXTEST</td>
<td>EXTEST</td>
<td>Vector #2</td>
</tr>
<tr>
<td>5</td>
<td>Reset</td>
<td>Reset</td>
<td></td>
</tr>
</tbody>
</table>
Controllable through the SIP-TAP
Transparent mode
Maximum exploitation of boundary-scan resources
Ideally require DFT in each die
MS and RF Dies

- **Challenges:**
  - Cost reduction of the required test equipment
  - Test of embedded dies because of difficulty to access these dies after SIP assembly.
**MS and RF Dies: cost reduction**

Analog Network of Converters:

- DSP-based methods / algorithms, the contribution of the non-linearity of each converter is discriminated.
- The converters may be re-used as embedded instruments in the loop!

*V. Kerzerho, et al. [ETS 2006]*
Compliant digital die with IEEE 1149.1

Compliant MS die with IEEE 1149.4
New challenges because of MEMS packaging

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Source: LIRMM
Test of Embedded MEMS

Testing the cavity sealing

Embedded MEMS

A moisture sensor is added

Cross-section view of a porous Si

Top view of a porous Si

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Concluding Remarks

- SIP offers many solutions for the miniaturization of heterogeneous electronic systems
- Known-good-die and assembly are very critical to achieve high yield and quality levels
- Test of embedded dies is a challenge too
- Many solutions for a cost-effective system test are emerging