Chapter 9

Design for Manufacturability and Yield
What is this chapter about?

- Introduce Design for Manufacturability (DFM) and related concepts
- Focus on:
  - Design for Yield (DFY) and yield models
  - Photolithography
  - Relationship between DFM, DFY, DFT
- Design for Excellence (DFX)
Design for Manufacturability & Yield

- Introduction
- Yield
- Components of Yield
- Lithography
- DFM and DFY
- Variability
- Metrics for DFX
- Concluding remarks
Introduction

- In the 1960s all aspects of IC design and manufacture could be confined to a single organization.
- Through the 1980s specialized fabs were common for individual products.
- Throughout this time technology followed Moore’s law, with ever increasing integration.
- Increased integration came with increasing costs.
Disaggregation

- Rising manufacturing costs led to ecosystem with specialized fabs fed by fabless semiconductor companies
Yield

\[ \text{Yield} = \frac{\text{good chips}}{\text{total chips}} \]

- Difficulty lies in separating good from bad
- Competing definitions of “good”
  - **Ideal**: works in customer’s application
    - Can’t measure this until it’s too late!
  - Example ambiguity: high leakage from defects and/or fast transistors
- Practical definition “passes the tests we apply”

\[ \text{Measured Yield} = \frac{\text{good parts} + \text{test escapes} - \text{false rejects}}{\text{all parts}} \]
Components of Yield

- Systemic problems (foundry)
  - Related to processing, managed by foundry
  - Kinds: spatial across wafer, layer-specific, machine-specific, etc.
  - Example: Oxide problems due to deposition
Components of Yield

- Systemic problems (foundry)
- Parametric variations (foundry, IP vendor)
  - Designs characterized over parametric window (“slow/typ/fast”)
  - Foundry process must remain within this window
  - Example parameters:
    - Channel length/width variation
    - nMOS to pMOS length ratio variation
    - Effective gate oxide thickness variation
    - Doping variation - threshold voltage and diffusion resistance
Components of Yield

- Systemic problems (foundry)
- Parametric variations (foundry, IP vendor)
- Defect-related yield (foundry, IP vendor, design team)
  - Susceptibility to shorts and opens
  - Caused by particles, cracks, voids, scratches, missing vias, etc.
Components of Yield

- Systemic problems (foundry)
- Parametric variations (foundry, IP vendor)
- Defect-related yield (foundry, IP vendor, design team)
- Design-related yield (IP vendor, design team)
  - Increasingly important issue
  - Examples: optical, physical/mechanical, electrical
Components of Yield

- Systemic problems (foundry)
- Parametric variations (foundry, IP vendor)
- Defect-related yield (foundry, IP vendor, design team)
- Design-related yield (IP vendor, design team)
- Test-related yield (test vendor)
  - Examples: overkill from guardbanding, test escapes
Components of Yield

- Systemic problems (foundry)
- Parametric variations (foundry, IP vendor)
- Defect-related yield (foundry, IP vendor, design team)
- Design-related yield (IP vendor, design team)
- Test-related yield (test vendor)
- DFY concerned with all of these
Yield models

Yield = systematic yield
* parametric yield
* defect yield
* design yield
* test yield

Poisson
\[ Y = Y_s \cdot e^{-AD} \]

Negative Binomial
\[ Y = Y_s \frac{1}{\left(1 + \frac{AD}{\alpha}\right)^\alpha} \]

Murphy
\[ Y = Y_s \left(1 - e^{-AD}\right)^2 \]

Bose-Einstein
\[ Y = Y_s \frac{1}{(1 + AD)^n} \]
Origins of Models

- Poisson Model
  - Defects are events from a random process with a uniform defect density

- Murphy Model
  - Defect density is not uniform, approximate Gaussian with a triangle distribution

- Bose-Einstein Model
  - Some layers more susceptible than others to defects, density uniform per layer

- Negative Binomial Model
  - Defects tend to cluster together

\[
Y = Y_s \cdot e^{-AD}
\]

\[
Y = Y_s \left(1 - e^{-AD}\right)^2
\]

\[
Y = Y_s \frac{1}{(1 + AD)^n}
\]

\[
Y = Y_s \frac{1}{\left(1 + \frac{AD}{\alpha}\right)^\alpha}
\]
**Yield and Repair**

- Four classes of yield:
  - Systematic problems (foundry)
    - Mild cases can be helped by repair
  - Parametric variations (foundry, IP vendor)
    - Mainly covered by design margin
    - Local extreme cases (e.g. weak cells) can be helped by repair
  - Defect-related yield (foundry, IP vendor, design team)
    - Most can be fixed with repair
  - Design-related yield (IP vendor, design team)
    - Covered by improved design practice

- Repair mainly addresses #3 (defects) at 90nm and above

- At 65nm and below, variability also important
**Repairable Memory**

\[
\Delta Y = P(\text{repair}) \cdot (1 - \text{base _ yield}) \\
= P(\text{repair}) \cdot (1 - e^{-AD})
\]

\[
\Delta Y_n = \text{repair _ yield}^n - \text{base _ yield}^n \\
= \left( e^{-(A+A_r)D} + P(\text{repair}) \cdot (1 - e^{-AD}) \right)^n - e^{-nAD}
\]

- Memory fails more than logic
- Repairable memory improves yield
Even at high overhead, significant yield improvement is possible.
Photolithography

- Decreasing feature size not accompanied by decreasing wavelength of light used
- 193nm and 157nm wavelengths most common in current technology
- Printing of features at 65nm, 45nm, and below uses off axis illumination, immersion lithography and more
Lithography Basics (Rayleigh Equation)

\[ \sin \theta_m = m \frac{\lambda}{P} \]
\[ P = m \frac{\lambda}{\sin \theta} \]
\[ P_{\text{min}} = 1 \frac{\lambda}{\text{NA}} \]
\[ R_{\text{min}} = 0.5 \frac{\lambda}{\text{NA}} \]
\[ R = k_1 \frac{\lambda}{\text{NA}} \]
\[ k_{1\text{min}} = 0.5 \]

1) resolution is controlled by \( \lambda \) and NA
2) improving resolution by increasing NA hurts DOF
3) \( k = 0.5 \) resolution limit is real physical barrier

Courtesy L. Liebmann

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DRC moving beyond simple distance metrics to shape-based approaches.
Example shape-based problem layout

Feature will be a problem across a wide range of geometries
DFM and DFY

- Uniformity is good for manufacturing
  - Example: arrays of bit cells
- Non-uniformity creates value
  - Example: standard cells with different layout
- DFM Challenge:
  Maintain manufacturability (enough uniformity) while allowing value (enough non-uniformity)
Uniformity in Polysilicon

- Compare SRAM array (left) with pre-DFM standard cell (right)
  - Uniform direction
  - Uniform shapes
  - Uniform spacing
**DFM is Subtle**

- Major problems found early in a process generation
  - Addressed by design rules
- Minor changes in layout cause significant changes in manufacturability and yield
- Examples: moving a wire a few nanometers, adding extra overlap around a contact, doubling a via
Lithography Simulation

- Simulate manufacturing process to identify problem areas ("hot spots")
- Several commercial solutions available
- Sensitive process information can be encrypted
Some DFM Challenges

- Forbidden pitches
  - Caused by inability to place SRAF due to conflict with neighboring shapes
- Shape-based problems, distance-based rule decks
  - Complex rules built out of need to avoid certain shapes combined with need to express constraints in standard DRC terms
DRC Spacing Example

- DRC is yes/no
- Silicon is continuous
- DFM recommendations and waivers attempt to compensate

### DRC Spacing Example

<table>
<thead>
<tr>
<th>Spacing</th>
<th>Relative Defect Probability</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>1.0</td>
</tr>
<tr>
<td>0.15</td>
<td>0.9</td>
</tr>
<tr>
<td>0.2</td>
<td>0.8</td>
</tr>
<tr>
<td>0.25</td>
<td>0.7</td>
</tr>
<tr>
<td>0.3</td>
<td>0.6</td>
</tr>
<tr>
<td>0.35</td>
<td>0.5</td>
</tr>
<tr>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>0.45</td>
<td>0.3</td>
</tr>
<tr>
<td>0.5</td>
<td>0.2</td>
</tr>
</tbody>
</table>

- **Waiver spacing**
- **Minimum spacing**
- **Recommended spacing**
Quantifying DFM: Critical Area

- Critical area measures the area where the center of a fixed size circular defect can land and cause a short or an open.
- Can be weighted by size distribution (typically $1/x^3$).
Weighted Critical Area

- Combine critical area and defect distribution into single value
- Integrate area under yellow curve for total value
Yield variation over time

More open space = Fewer shorts

Double contacts = Fewer opens

At any time, one or the other could be better
- Fab engineers use a Pareto chart to find key problems
- Over time, systematic problems will be fixed, leaving random (defect-related) yield to dominate
Variability

- Historically, test concerned with defects, validation concerned with design variation

- Process variability occupies a middle ground
  - Small variation: expected
  - Medium variation: needs to be tolerated by design (margin)
  - Large variation: needs to be found by test
Sources of variability

- Accounted for by standard device model
  - Lot-to-Lot
  - Wafer-to-Wafer
  - Die-to-Die

- More complex effects, sometimes included in model
  - Within Die examples
    - Length variability
    - Oxide variability
    - Implant variability
Example: Leakage and Gate Length

- Longer gate leads to higher Vt
- Small change in Vt (<100mV) leads to large change in Ioff (10X) with small change in performance (10%)
Finding variability at wafer level

- Reticle based variability
  - 2x2 reticle
  - Patterning issue – likely sources masks, lithography
Variability across a wafer

- Chemical/physical aspects of process optimized for middle distance from center, can cause variability issues at center and edges
  - Examples include etch, polishing
Radial variability

- Starts in one region and works outwards
  - May be related to position in equipment
Variability versus defectivity

- Outliers and discontinuities may be defect related
DFX – Design For Excellence

- DFX = multidimensional optimization
- DFX can be
  - DFT: testability
  - DFM: manufacturability
  - DFY: yield
  - DFR: reliability
- Optimization requires quantification
Quantified Tradeoffs – DFM Metrics

- Simple but effective
- Recommended rule classes
  - No effect on area: implement all
  - Affects area
    - Find intermediate value point
- Example: contact-poly spacing
  - Minimum DRC value: 80nm (0 credit)
  - Recommended DRC value: 120nm (full credit)
  - 80% of yield benefit achieved: 90nm (half credit)
- Sum and score across instances
## Example DFM Rules and Metric

<table>
<thead>
<tr>
<th>Rule</th>
<th>Weight</th>
<th>Scoring</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rule</td>
<td>Weight</td>
<td>Scoring</td>
</tr>
<tr>
<td>1. Increase line end</td>
<td>.4</td>
<td>0.05</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.15</td>
</tr>
<tr>
<td>2. Avoid jogs in poly</td>
<td>.3</td>
<td>Jog &gt; 0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Jog &gt; 0.05</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Jog &lt; 0.05</td>
</tr>
<tr>
<td>3. Reduce critical area for poly gates</td>
<td>.2</td>
<td>0.15 spacing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2 spacing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.25 spacing</td>
</tr>
<tr>
<td>4. Maximize contact overlap</td>
<td>.1</td>
<td>0.05 on 2 sides</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.05 on 3 sides</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.05 on 4 sides</td>
</tr>
</tbody>
</table>

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Metric in practice

- Example rules:
  1. Line ends
  2. Jogs
  3. Spacing
  4. Contact overlap

- Key:
  A=best
  B=partial
Improved Layout

- Metric improves for
  1. Line ends
  2. Jogs
  3. Spacing
  4. Contact overlap

- Some locations cannot be improved ("C") without increasing area
Concluding Remarks

- Yield is a complex function of many variables
- Repair can improve yield for some structures
- Photolithography and related challenges influence DFM rules
- Effective DFM more complicated than design rule checking allows
- Metrics can be developed to improve manufacturability
- Multidimensional optimization is the key to effective Design For Excellence (DFX)