Chapter 10

Design for Debug & Diagnosis
What is this chapter about?

- Introduce the concept of chip debug and diagnosis and show various design features that are needed for successful debug and diagnosis

- Focus on
  - design features at the architectural, logic, circuit, and layout level that are needed to facilitate silicon debug and defect diagnosis of integrated circuits.
  - Circuit editing features so that chips can be repaired and hypothesis validated and confirm root cause fixes

- Provide an overview of the debug and diagnosis process (strategy and flow/methodology)
Design for Debug and Diagnosis

- Introduction
- Logic Design for Debug and Diagnosis (DFD) Structures
- Probing Technologies
- Circuit Editing
- Physical DFD Structures
- Diagnosis and Debug Process
- Summary and Future Challenges
Introduction

- New chip designs are likely to require debug before they can go into manufacturing.
- Manufacturing startup/ramp also may require low yield analysis for yield improvement.
- Chip in use may fail due to infant mortality or other failure/wearout mechanism that may require investigation.

*Debugging must be planned for during the design of chips to ease any of these needs.*
Debug vs. Diagnosis

- Diagnosis: investigation or analysis of the cause or nature of a condition, situation, or problem
- Debug: the process of isolating bugs or errors that causes a design to behave differently from its intended behavior under its specified operating conditions.

To answer:
- What was wrong with this device?
- Which chip was bad on this board?
- Why did this system crash?
- Why did the simulation of the arithmetic logic unit (ALU) show that 2+2=5?
- Why was this signal late?
Where is Diagnosis Used?

- **MCMs, boards, systems**
  - Identification followed by replacement of the faulty subcircuit (a chip on a board or a board in a system)
  - Reconfiguration of the circuit around the failure.

- **Chips**
  - To identify circuit flaws to be fixed due to design issues
  - To improve the manufacturing process
Debug & diagnosis throughout VLSI Life Cycle

- Design
- Production Ramp
- Design revisions
- Production Ramp
- Volume Production
- Debug
- Qualification

Spec
- Logic Error Diagnosis
- Tapeout / Silicon
- Silicon Debug

Requirements
- Time
- End of life

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Silicon Debug versus Defect Diagnosis

- Silicon debug starts with the arrival of first silicon and continues till volume production
  - logic (functional) errors
  - circuit sensitivities or marginalities; timing or critical speed-path issues
  - physical design errors
Silicon Debug versus Defect Diagnosis

- **Defects:** physical imperfections in the manufactured chip
  - Early process development: Use of memory structure due to ease of fault isolation
  - Intermediate & mature phase: actual design due to design/process interactions, hence requiring logic diagnosis

<table>
<thead>
<tr>
<th>Time</th>
<th>Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Early phase</td>
<td>SRAM vehicle; Test chip; monitors</td>
</tr>
<tr>
<td>Intermediate phase</td>
<td>First product(s); Unexpected low yields due to Process-product interaction</td>
</tr>
<tr>
<td>Mature phase</td>
<td>High volume Product(s) – yield vehicles; Excursions</td>
</tr>
</tbody>
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Defect Diagnosis

Yield

Excursion; High fallout

Time

Failure Location

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Design for Debug and Diagnosis

- a high degree of **observability**
  - observe erroneous events close to when they happen
- **controllability** to further validate what the cause of the problem is
  - to narrow down the circuits that manifest the symptoms

*Many DFT features (e.g., scan) can be reused*
**Logic DFD structures**

- to extract logic/timing information
- to manipulate the operation of a chip non-intrusively

**Physical DFD structures**

- to either enable probing or make corrections to the circuit to verify root-cause fixes
Scan

Muxed scan or LSSD OK

1. Stop clock at suspected (functional test) cycle
2. Enable scan mode
3. Shift state content into scan chain
4. Shift scan data out
5. Compare with simulated (RTL or gate level) result
6. Repeat 1-5 with pattern rerun (due to scan shift destroying state content) and stop at later clock(s)
**Observation-Only Scan**

- Observe only -- No controllability
- Can be placed anywhere (not necessarily tied to latch/flops)
  - Capture/Latch with system clock
- Can be tied to any specific nodes of interests
  - Gate, wires, anything...

![Observation-Only Scan Diagram](image-url)
Observation-Only Scan – system view
Observation Points with Multiplexers

- Multiplexers to concatenate individual signals to be mapped out to a test port
- Programmable interface may allow different sets of signals to be observed at different times
- Logically simple, BUT
  - Test/Mux control may be massive
  - Not routing friendly
  - Signals you needed may not be included
Array Dump and Trace Logic Analyzer

- **Array structures are usually not scanned**
  - Need array dump feature
  - Content unloaded onto convenient output interfaces (e.g. buses or TDO)
  - Reversed feature (array load) may be desirable for validation of hypothesis

- **Arrays can be deployed for storing on-chip events**
  - Bus transactions, various signals
  - Aka on-chip Logic Analyzer
  - Original array resized for original purposes
Clock control

- “Where” from scan/scanout
- “When” with clock control
- Starting, stopping, and restarting of internal clocks while keeping them synchronized to specific external and internal events
  - Clock is internally synthesized from PLL
  - Offset counters
    - E.g. 487 clock cycles after an exception event
  - Single stepping
- Clock stop + scan dump
Advanced clock control
Advanced clock control

PLL

Clock regions
+60ps
+120ps
+0ps

Buffers

Main Clock (PLL)
Region 1 (normal)
Region 2 (more skew)
Region 3 (less skew)

+60ps (default)
+120ps
+0ps
Partitioning, Isolation, and De-featuring

- Partitioning: separate/decouple blocks
  - Does problem still exist?
  - E.g. disabling the caches

- Isolation/defeaturing: selective disabling of features to allow identification of specific area
  - E.g. turns off different execution units in turns

- Restricted to logic blocks that are not absolutely needed
Probing Technologies

- Contact probing
  - Mechanical probing
- Non-contact probing
  - Beam injection (laser or e-beam)
  - Emission detection (photon or thermal infrared)
Mechanical probing

Long Working distance microscope objective 10-15mm working distance

Probe manipulator

Sample Holder and fixturing

Probestation base

IC
**E-beam probing**

A line at 0 Volts does not influence the low energy Secondary Electrons. Most electrons escape to the detector and the line appears bright.

A positively biased line attracts low energy Secondary Electrons back to itself. Few electrons escape to the detector and the line appears dark.

- **Primary E-beam**
- **Secondary Electrons collected by detector**

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0 Volts

Vcc Volts
Voltage Contrast

Normal

Low potential (0V) highlighted
Logic state or timing

Logic state map
Timing waveform at any node

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Packaging induced challenges

Wirebonded

C4/flip chip
Backside probe with e-beam

a) Flip Chip MCM with 2 Chips A & B and LICAs. Chip B needs to be probed.

b) First Globally thin Chip B only to a thickness ~100µm - using a fast wet chemical etch.

c) Magnified view of silicon chip B in MCM in the region of the circle. Use Laser Chemical Etch to mill a local trench to within 10 µm of the P-Well and active circuits. The trench walls are sloped to minimize the amount of silicon removed.

d) Magnified view of region in circle in c). Final Probe hole drilled at the base of the LCE generated trench to expose an N+ diffusion (NAC) diode. The E-Beam probes the N+ diffusion directly. The tapered holes improve electron collection through the hole for the E-Beam probing and FIB imaging.
Optical probing

**Backside view using IR**

**Front view (metal blocking much of the area underneath)**

*Silicon is transparent to IR*
Optical probing principle

With NO input electrical signal

With applied electrical signal
**IR prober setup**

Mode Locked Laser
100MHz, 1.064\(\mu\)m, 
\(~30\text{ps} \) pulse width

Laser sampling pulses

Silicon IC

Collimating Lens

Faraday Rotator

Polarizing Beam Splitter

IR Objective Lens

Photodiodes

To Detection Electronics

Output Timing Waveform

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Infrared Emission Microscopy (IREM)

Emission with IREM

Emission mapped to logic states
Picosecond Imaging Circuit Analysis (PICA)

Note: optical energy for N and P transistors are not identical


**Time Resolved Emissions (TRE)**

- Same physics as PICA
- Much sensitive spot sensor
  - More detail timing waveform
Circuit editing

- Micro/Nano-surgery
  - Removal (cross-sectioning) of material (or trenching) for improved e-beam or optical probing
  - Cutting of wires
  - Deposition of material to create new connections

Focused Ion Beam
Focused Ion Beam

Global Thinning from 700µm to 150µm

Local Thinning to 10µm over area of interest

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Layout-Database-Driven Navigation System

FIB or prober
Linking polygons to schematics to RTL
Spare Gates and Spare Wires

Branch A

Branch B

Branch C

Branch D

FIB Deposition
FIB Connect (A)
FIB Cut (C)

Signal X
A1

A3
A4
A5
A7

VCC

Bonus AND Gate

C1
C2
C3
C4
C5

Signal Y

VSS
VCC

A6
A8
Physical DFD

- Layout design to facilitate the probing (contact or non-contact; emission or injection probing)
- Layout design is also needed to put in spare gates and spare wires and plans for patching/blue-wiring
Physical DFD for Pico-Probing

- Placement of pads with plenty of open space
  - Avoid shorting to neighboring wires
- Pads size compatible with probe tip sizes
- Avoid putting active signals underneath probe pads
- Dummy metals may be put underneath for planarization
Physical

DFD for

E-Beam

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Physical DFD for FIB and Probing

- Driven by FIB precision
- Generous spacing planned for cutpoints
- Specifically design cut sites
- Add probe diodes as probe points
Diagnosis and debug process

- Applied Test
- Circuit Model
- Test Results
- Other Data

Diagnosis

Faults

Failure Analysis

Defects/Errors
Fault propagation

fault-

effect propagation path

observed error
(far from the crime scene)

fault

1

stuck-at-0

0/1

0/1

0

1

0
Future challenges

- Voltage scaling
  - Reliability driven (power also reduced)
  - Devices may not be driven to saturation
  - Emission reduced
  - Smaller charge at any nodes

- Heisenberg Uncertainty Principle applies – the very act of observing something changes its nature
Future Challenges

- Dynamic and leakage power
  - Thermal density & heat removal during debug
- Adaptive control of voltage & frequency
  - How to debug under these dynamic situations?
- On-chip DFD to supplement inadequacy of ATE
- Tools to help with identification of sensitive circuits, DFD implementations, test generation for debug, debug automation
Summary

- This chapter presented an overview of the debug/diagnosis process, logical/timing debug, various probing technologies as well as circuit editing technologies.
- Provided unique guidance for logical and physical design for debug.
- Future challenges are identified for audience to pursue.