Chapter 11

Analog and Mixed-Signal Testing
What is this chapter about?

- Introduces AMS circuits, failure modes and fault models.
- Addresses analog testing, including DC and AC parametric testing.
- Discusses mixed-signal circuits, ADC and DAC, and their testing approaches.
- Studies IEEE Std. 1149.4, the standard for mixed-signal test buses.
Chapter 11
Analog and Mixed-Signal Testing

- Introduction
- Analog Circuit Testing
- Mixed-Signal Testing
- IEEE Std. 1149.4 Standard for Mixed-Signal Test Bus
- Concluding Remarks
11.1 Introduction

- Analog Circuit Properties
- Analog Defect Mechanism and Fault Models
Analog, Digital, and Mixed-Signal Signals
Analog Circuit Properties

- Continuous Signal
- Large Range of Circuits
- Nonlinear Characteristics
- Feedback Ambiguity
- Complicated Cause-Effect Relationship
- Absence of Suitable Fault Model
- Accurate Measurements Required
Properties - Continuous Signal

Digital Signal

- Logic 1, Logic 0
- VIH, VIL, VOH, VOL
- Rise Time, Fall Time
- Propagation Delay H-L/L-H
- Noise Margin High/Low

Analog Signal

- Voltage/Current
- Slew Rate
- Overshoot
- Damping Factor
- Frequency
- Bandwidth

VLSI Test Principles and Architectures
Chap. 11 - Analog and Mixed-Signal Testing - P.7
Properties - Large Ranges of Circuits

Digital Circuits
- Operation
  - Static Logic
  - Dynamic Logic
- Structure
  - Gates
  - PLA
  - Memory

Analog Circuits
- Operation
  - Current Mode
  - Voltage Mode
  - Switching Cap
- Structure
  - Amplifier
  - Multiplier
  - Rectifier
  - Resonator
Properties - Nonlinear Characteristics

- Analog circuits are nonlinear in nature
- Nonlinear cause effect

\[ I_D = I_s \cdot e^{V_D / n \times V_T} \]

\[ I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{gs} - V_t)^2 \]
Properties - Feedback Ambiguities

- Feedback puts circuit parameters together
- Difficult to identify fault location
Properties - Complicated Cause-Effect Relationship

- Difficult to determine the cause of error.

\[
A_V = \frac{V_0}{V_i} = -\frac{R_2}{R_1}
\]

\[
A = \frac{V_0}{V_i} = -\left(1 + \frac{A}{R_2}\right)R_1
\]
Properties – Absence of Suitable Fault Models

Digital Faults

- Good Logic Fault Model
- Generally Accepted
  - Stuck-at-1, Stuck-at-0
  - Stuck-Open, Stuck-On
  - Short. Open
  - Memory Faults
  - PLA Faults
Properties - Absence of Suitable Fault Models

Analog Faults

- No Good Fault Model
- Not Generally Accepted
  - Open Short
  - Missing/Extra Devices
  - Parameter Variation
  - Performance Deviation
  - Circuit Structure Related
  - Functional Faults
  - ??????????????
Properties — Accurate Measurements Required

Digital Instrument

- Oscilloscope
- Function Generator
- Logic Analyzer
- Frequency Counter
Properties – Accurate Measurements Required

- Oscilloscope
- Function Gen
- Freq. Counter
- Spectrum Analyzer
- Network Analyzer
- Impedance Analyzer
- Timing Analyzer
- Communication Analyzer
- RF Instrument
- Optical Instrument
- Microwave Instrument
11.1 Introduction

- Analog Circuit Properties
- Analog Defect Mechanism and Fault Models
Defect Mechanisms (1)

- **Material Defects**
  - cracks
  - crystal imperfection
  - surface impurities
  - ion migration

- **Processing Faults**
  - oxide thickness
  - mobility change
  - impurity density
  - diffusion depth
  - dielectric constants
  - metal sheet resistance
  - missing contacts
  - dust
Defect Mechanisms (2)

- **Time-Dependent Failures**
  - dielectric breakdown
  - electron migration

- **Packaging Failures**
  - contact degradation
  - seal leakage
Analog Fault Model

Defects/Failure

Hard Faults

Soft Faults
Analog Faults - Defect

- Defects
  - Extra Defects
  - Etching Defects
- Source
  - Dust
  - Lithography
- Layout Oriented
- Statistical Model
**Analog Faults - Hard Faults**

- **Fault Models**
  - Open
  - Short
  - Missing Device
  - Extra Devices

- **Faulty Effects**
  - Catastrophic Error
  - Module Malfunction
  - System Failure
Analog Faults - Soft Faults

- Parametric Faults
  - $I_o$: 100uA -> 50uA
  - $W$: 20um -> 10um

- Deviation Faults
  - $f_o$: 10MHz -> 5MHz
  - Gain: 10000 -> 2000

- Sources
  - Mobility
  - Oxide Thickness
  - Impurity Density
  - Defusion Depth
  - Dielectric Constants
  - Metal Sheet Resistance
Analog Fault - Model Mapping

- Functional Level
  - Deviation Faults

- Circuit Level
  - Parametric Faults
  - Extra Defects
  - Etching Defects

- Layout Level
**Analog Faults - Model Mapping**

**Layout to Parametric**
- **Defect Statistics**
  - Randomly insert dusts of random size.
- **Parameter Statistics**
  - Simulate the effect of dust on transistor parameters

\[
K = \mu C_{ox} \frac{W}{L}
\]
Analog Faults - Model Mapping

Parametric to Deviation
- Use SPICE simulation and statistics to derive the performance deviation.

\[ K = \mu C_{ox} \frac{W}{L} \]
11.1 Summary

- Studied the analog test properties
  - Nonlinearity, Feedback Ambiguity
  - No good fault model

- Overview the analog test plan
  - Test Code, Binning, Sequence Control
  - Focused Calibrations, DIB Checkers
  - Characterization and Simulation Code

- Analog Fault Model
  - Extra and Etching Defects
  - Parametric and Deviation faults
  - Model Mapping
11.2 Analog Circuit Testing

- Analog Test Approaches
- Analog Test Waveforms
- DC Parametric Testing
- AC Parametric Testing
Analog Testing

Spec Oriented

Waveform Oriented
### Specification Oriented Test

**OP777/OP727/OP747—SPECIFICATIONS**

**ELECTRICAL CHARACTERISTICS** (© $V_o = 5 \text{ V}$, $V_{CM} = 2.5 \text{ V}$, $T_A = 25{\degree} \text{C}$ unless otherwise noted.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Voltage OP777</td>
<td>$V_{OS}$</td>
<td>$+25{\degree} \text{C} &lt; T_A &lt; +85{\degree} \text{C}$</td>
<td>20</td>
<td>100</td>
<td></td>
<td>$\mu$V</td>
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<tr>
<td>Offset Voltage OP727/OP747</td>
<td>$V_{OS}$</td>
<td>$-40{\degree} \text{C} &lt; T_A &lt; +85{\degree} \text{C}$</td>
<td>50</td>
<td>200</td>
<td></td>
<td>$\mu$V</td>
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<td>Input Bias Current</td>
<td>$I_N$</td>
<td>$+25{\degree} \text{C} &lt; T_A &lt; +85{\degree} \text{C}$</td>
<td>30</td>
<td>160</td>
<td></td>
<td>$\mu$A</td>
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<tr>
<td>Input Offset Current</td>
<td>$I_{OS}$</td>
<td>$-40{\degree} \text{C} &lt; T_A &lt; +85{\degree} \text{C}$</td>
<td>60</td>
<td>300</td>
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<td>$\mu$A</td>
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<td>Input Voltage Range</td>
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<td>5.5</td>
<td>11</td>
<td></td>
<td>$n$A</td>
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<td><strong>CMRR</strong></td>
<td></td>
<td></td>
<td>0</td>
<td>4</td>
<td></td>
<td>$V$</td>
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<td><strong>Large Signal Voltage Gain</strong></td>
<td>$A_{VOL}$</td>
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<td>104</td>
<td>110</td>
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<td>$d$B</td>
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<td><strong>Offset Voltage OP777</strong></td>
<td>$V_{OS}/\Delta T$</td>
<td></td>
<td>500</td>
<td>500</td>
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<td>$V/m$V</td>
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<tr>
<td><strong>Offset Voltage OP727/OP747</strong></td>
<td>$V_{OS}/\Delta T$</td>
<td></td>
<td>0.3</td>
<td>1.3</td>
<td></td>
<td>$\mu$V/$^\circ$C</td>
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<tr>
<td><strong>OUTPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td>0.4</td>
<td>1.5</td>
<td></td>
<td>$\mu$V/$^\circ$C</td>
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<td>Output Voltage High</td>
<td>$V_{OH}$</td>
<td></td>
<td>4.88</td>
<td>4.91</td>
<td></td>
<td>$V$</td>
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<tr>
<td>Output Voltage Low</td>
<td>$V_{OL}$</td>
<td>$-40{\degree} \text{C} &lt; T_A &lt; +85{\degree} \text{C}$</td>
<td>120</td>
<td>140</td>
<td></td>
<td>$m$V</td>
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<tr>
<td>Output Circuit</td>
<td>$I_{OUT}$</td>
<td>$V_{DROP} &lt; 1 \text{ V}$</td>
<td>$\pm10$</td>
<td></td>
<td></td>
<td>$m$A</td>
</tr>
<tr>
<td><strong>POWER SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>$PSRR$</td>
<td>$V_{OS} = 3 \text{ V} \text{ to } 30 \text{ V}$</td>
<td>120</td>
<td>130</td>
<td></td>
<td>$d$B</td>
</tr>
<tr>
<td>Supply Current/Amplifier OP777</td>
<td>$I_{SV}$</td>
<td>$V_{OS} = 0 \text{ V}$</td>
<td>220</td>
<td>270</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>Supply Current/Amplifier OP727/OP747</td>
<td>$I_{SV}$</td>
<td>$-40{\degree} \text{C} &lt; T_A &lt; +85{\degree} \text{C}$</td>
<td>270</td>
<td>320</td>
<td></td>
<td>$\mu$A</td>
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<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td>235</td>
<td>290</td>
<td></td>
<td>$\mu$A</td>
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<tr>
<td>Slew Rate</td>
<td>$SR$</td>
<td></td>
<td>290</td>
<td>350</td>
<td></td>
<td>$\mu$A</td>
</tr>
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<td>Gain Bandwidth Product</td>
<td>$GBP$</td>
<td></td>
<td>0.2</td>
<td></td>
<td></td>
<td>$V/\mu$S</td>
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<td><strong>NOISE PERFORMANCE</strong></td>
<td></td>
<td></td>
<td>0.7</td>
<td></td>
<td></td>
<td>$M$Hz</td>
</tr>
<tr>
<td>Voltage Noise</td>
<td>$e_{d\mu}$</td>
<td>$0.1 \text{ Hz} \text{ to } 10 \text{ Hz}$</td>
<td>0.4</td>
<td></td>
<td></td>
<td>$\mu$V/$\sqrt{Hz}$</td>
</tr>
<tr>
<td>Voltage Noise Density</td>
<td>$e_a$</td>
<td>$f = 1 \text{ kHz}$</td>
<td>15</td>
<td></td>
<td></td>
<td>$n$V/$\sqrt{Hz}$</td>
</tr>
<tr>
<td>Current Noise Density</td>
<td>$i_b$</td>
<td>$f = 1 \text{ kHz}$</td>
<td>0.13</td>
<td></td>
<td></td>
<td>$p$A/$\sqrt{Hz}$</td>
</tr>
</tbody>
</table>

**NOTES**

- Typical specifications: >50% of units perform equal to or better than the "typical" value.
- Specifications subject to change without notice.
Specification Oriented Test

- Specification Oriented Test
  - Check whether all the specs are met
  - Tedious and inflexible

- Example: Operational Amplifier

- DC Specifications
  - Input Offset Voltage
  - Input Bias Offset Current
  - Open-Loop Gain
  - Noise
  - Common Rejection Ratio
  - Temperature Drift

- AC Specifications
  - Bandwidth
  - Harmonic Distortion
  - Slew Rate
  - Settling Time
  - Noise
Waveform Oriented Test

- Compare waveform to the simulated ones
Waveform Oriented Test

<table>
<thead>
<tr>
<th>A</th>
<th>DC Bias, Input Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>Slew Rate, Damping Factor</td>
</tr>
<tr>
<td>C</td>
<td>Overshoot, Damping Factor, Bandwidth</td>
</tr>
<tr>
<td>D</td>
<td>Settling Time, DC Gain</td>
</tr>
</tbody>
</table>
Analog Testing - Comparison

- Specification Oriented Test
  - Require more test runs and time
  - Require accurate instrument
  - Specifications are guaranteed
  - *Low defect level*

- Waveform Oriented Test
  - Less test runs and test time
  - More forgiving on instrument
  - Specifications are not guaranteed
  - *Low cost*
11.2 Analog Circuit Testing

- Analog Test Approaches
- **Analog Test Waveforms**
- DC Parametric Testing
- AC Parametric Testing
Analog Test Waveforms

- Sine
- Square (Step)
- Ramp
- Triangular
- Chirp (Sweep Sine)
- Arbitrary
- Modulated
For transient response testing
- Application: Filter, OPs, VCO, etc
- Difficult to generate good steps

\[ \theta = \pm 45^\circ \sim \pm 60^\circ \]

\[ f = \frac{1}{(4 \sim 3)T_r} \]

\[ f = \frac{1}{3.5T_r} \]
Waveform - Step

- Step change in voltage: Transient testing
- Step change in frequency: PLL testing
- Step change in amplitude: AGC testing
Waveform - Ramp

- Triangular Wave Generation

- Sawtooth Wave Generation
Waveform - Chirp

- Also called Sweep Sine
- Generation: Triangular to VCO
- Application: Frequency response plotting
Waveform - Chirp

Application: Frequency response plotting

Diagram showing a VCO connected to a CUT (under test) which is then passed through a filter and a LPF (low-pass filter). The waveform changes are depicted at different stages of the process.
Waveform - Arbitrary

- Synthesized by DACs
- Combinations of all kinds of waveform
Modulated/Synthesized Waveforms

- Communication System Testing
  - GSM, CDMA, 1394, USB2, etc.

- Modulation
  - AM, FM, PCM, PWM, QAM, PSK, QPSK

Generated by dedicated instrument
11.2 Analog Circuit Testing

- Analog Test Approaches
- Analog Test Waveforms
- DC Parametric Testing
- AC Parametric Testing
## DC Parametric Testing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated output current</td>
<td>Rated output voltage</td>
</tr>
<tr>
<td>Open-loop gain</td>
<td>Slewing rate</td>
</tr>
<tr>
<td>Unity gain full power response</td>
<td>Unity gain small signal response</td>
</tr>
<tr>
<td>Overload recovery</td>
<td>Input bias current</td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>Input offset current</td>
</tr>
<tr>
<td>Input noise</td>
<td>Input impedance</td>
</tr>
<tr>
<td>Supply voltage sensitivity</td>
<td>Common mode rejection</td>
</tr>
<tr>
<td>Maximum voltage between inputs</td>
<td>Maximum common mode voltage</td>
</tr>
<tr>
<td>Temperature drift</td>
<td></td>
</tr>
</tbody>
</table>

Source: [Sata 1967]
**DC Test – Open-Loop Gain Measurement**

\[ A_o = 101 \cdot \frac{\Delta V_x}{\Delta V_y} \]
**DC Test** – Unit Gain Bandwidth Measurement

\[ f_t = A_o \cdot f_{3dB} \]

- **Inverting Configuration**
  \[ V_i \leq \frac{SR}{2\pi f_t} \]

- **Noninverting Configuration**
  \[ V_i \leq \frac{SR}{2\pi f_t} \]

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**DC Test – Common Mode Rejection Ratio**

\[ V_{CM,i} = \frac{\Delta V_o}{A_o} = \Delta V_o / \frac{R2}{R1} \]

\[ CMRR = 20\log(A_o / \frac{\Delta V_o}{\Delta V_{CM}}) \]
**DC Test – Power Supply Rejection Ratio**

\[ PSRR = 20 \log(A_o / \frac{\Delta V_o}{\Delta V_{DD}}) \]
11.2 Analog Circuit Testing

- Analog Test Approaches
- Analog Test Waveforms
- DC Parametric Testing
- **AC Parametric Testing**
Analog AC Testing

- Test Types
  - Gain
  - Phase
  - Distortion
  - Signal Rejection
  - Noise

- Test Setup
  - AGW: Arbitrary Waveform Generator (DAC)
  - Digitizer: Sample and convert to digital (ADC)
AC – Maximal Output Amplitude

- Input sine wave (1KHz) with fixed amplitude
- Digitize the output waveform
- DSP (FFT) to eliminate distortion and noise.
- Check the fundamental amplitude.
- Detect first order defects in a circuit.
- Voltage in dBV or dBm
AC - Frequency Response

- **LPF**: Low Pass Filter
- **HPF**: High Pass Filter
- **BPF**: Band Pass Filter
- **BRF**: Band Reject Filter
AC - Frequency Response

Bode Plot

\[ A(jw) = \frac{10^2 \left(1 + \frac{jw}{10^6}\right)}{(1 + \frac{jw}{10^2})(1 + \frac{jw}{10^4})} \]

- Open Loop Gain: \(10^2\)
- Pole 1: \(10^2\)
- Pole 2: \(10^4\)
- Zero: \(10^6\)

VLSI Test Principles and Architectures
AC - Frequency Response

- Pass Band Ripple
- Stop Band Rejection
- Stop Band
- Pass Band
- Stop Band
AC - Frequency Response
Frequencies of special interests
AC - Frequency Response

- Multi-tone Test Waveform

$$A(t) = \sum_{i=1}^{i=k} A_i \sin(\omega_i t + \phi_i)$$
AC - Frequency Response

- Multi-tone Test Waveform

\[ A(t) = \sum_{i=1}^{i=k} A_i \sin(\omega_i t + \phi_i) \]
AC – Noise and Distortion

• Distortion
  • Harmonic Distortion
  • Intermodulation Distortion
  • Crossover

• Cause
  • Nonlinearity of the circuit
  • Clip (saturation)
  • Mismatch of the devices
AC – Noise and Distortion

- Apply sinusoidal waveform
- Do Fourier transform on response waveform
- Obtain F domain properties mathematically.
**AC – Noise and Distortion**

\[
THD = 10 \log \frac{F^2}{\sum H_i^2} = 100 \times \frac{F^2}{\sum H_i^2} \%
\]

\[
SNR = 10 \log \frac{F^2}{\sum N_i^2}
\]

\[
SNDR = 10 \log \frac{F^2}{\sum H_i^2 + \sum N_i^2}
\]
\[ v(t) = A_1 \sin 2\pi f_1 t + A_2 \sin 2\pi f_2 t \]
11.2 Summary

- Studied the analog test approaches
  - Specification oriented testing
  - Waveform oriented testing
-Outlined the analog test waveforms
  - Sine, step, triangular, chirp, arbitrary, modulated
- Discussed DC parametric testing
  - Open-loop gain, unit gain bandwidth
  - CMRR, PSRR
- Discussed AC parametric testing
  - Use AWG, Digitizer, and DSP
  - Frequency response, Noise, and Distortion
11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
- ADC and DAC Circuit Structure
- ADC/DAC Specification and Fault Models
- IEEE Std. 1057
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing
AD Model - Quantization

\[ X_{\text{out}} \text{ LSBs} \]

\[ X_{\text{in}} \]

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Quantization error is sawtooth-like.
Uniform distribute between \((-q/2, q/2)\) (\(q=\text{LSB}\)).

Quantization Noise Model

\[ x(t) \quad \text{Original signal} \quad \text{Quantized signal} \]

\[ n_q(t) \quad \text{Quantization error} \]
Quantization – Noise Model

- The error contains a lot of jumps.
- Error spectral is much wider than the original signal.
- The bandwidth of the quantization is proportional to the slope of the signal and inversely proportional to the quantum size $q$.

$$n_q(t)$$

Quantization error

$$q/2$$

$$-q/2$$

$t$
A sine wave is quantized by a B-bit ADC. How large is the SNR.

\[ 2V_p = 2^n q \]

\[ P_S = \frac{V_p^2}{2} \]

\[ P_N = \left( \frac{q/2}{\sqrt{3}} \right)^2 = \frac{q^2}{12} \]
Quantization - Noise Model

\[ SNR = 10 \log \frac{P_s}{P_N} = 10 \log \left( \frac{\frac{V_p^2}{2}}{\frac{q^2}{12}} \right) = 10 \log (6 \cdot 4^{n-1}) \]

\[ SNR = (1.76 + 6n) \text{dB} \]

For \( n=10 \), \( SNR = 61.8 \text{dB} \)
11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
- ADC and DAC Circuit Structure
- ADC/DAC Specification and Fault Models
- IEEE Std. 1057
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing
**ADC Architecture - Gain Stage**

- **Gain:** Provide offset and full scale conversion
- **Filter:** Reject off-band noise (anti-aliasing filter)
- **MUX:** Provide multiple channel access
- **S/H:** Provide steady signal for A-to-D conversion
- **ADC:** Actual analog to digital conversion
**ADC Architecture - Gain Stage**

- **Function:** Provides gain and offset
- **Achieve the maximal A/D resolution by scaling the input signal to match the full A/D input range.**
- **Drawbacks:**
  - Introduces noise, nonlinearity, drift
  - Expense of tight-tolerance
  - Require calibration
ADC Architecture - Filter Stage

- Function: Attenuate the out-of-band noise to prevent aliasing
- Filter Position
  - Before the MUX (1 per channel): maximize speed in switching channels.
  - After the MUX: minimize mismatching among channels.
ADC Architecture - Filter Stage

- Anti-Aliasing Filter

\[ A(w) \quad \text{Anti Aliasing Filter} \]

Signal Spectrum

Nyquist Rate Sampling

4X Over Sampling
Function: Provides multiple access

Crosstalk:
- The most severe problem
- Frequency dependent
- Can be minimized by placing amplifier before the MUX.

Load Issues
- Avoid too many fanins.
- Use hierarchical structure.
ADC Architecture - S/H Stage

- **Function:**
  - Provides steady signal
  - Provides signal synchronization,

- **S/H position:**
  - After the MUX for cost reason
  - Before MUX for synchronization and crosstalk reduction.
ADC Architecture - S/H Check List

- **Aperture Time**: The time aperture \((t3)\)
- **Acquisition Time**: The total time for the S/H to acquire a full-scale step input signal. \((t3 - t1)\)
- **Aperture Jitter**: The uncertainty of aperture time due to noise or jitter in clock. \((t4-t2)\)

\[
\begin{align*}
V_{\text{droop}} &= \frac{I_{\text{leak}}}{C_H} \\
\Delta V_c &\leq X\% \cdot \text{LSB}
\end{align*}
\]
ADC Architecture - ADC Stage

- ADC

- Gain
- Filter
- MUX
- S/H

Executes analog to digital conversion

Check List:

- Bit length
- Accuracy
- Conversion Rate
- System Error Budget
- Input Signal Range
- Total System Cost Target
- Input Impedance
- AC or DC Inputs BW

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**DAC Example - R-2R Ladder**

\[
V_o = S_5 \cdot \frac{V_{ref}}{2^1} + S_4 \cdot \frac{V_{ref}}{2^2} + S_3 \cdot \frac{V_{ref}}{2^3} + S_2 \cdot \frac{V_{ref}}{2^4} + S_1 \cdot \frac{V_{ref}}{2^5} + S_0 \cdot \frac{V_{ref}}{2^6}
\]

\[
= (S_5 \cdot 2^5 + S_4 \cdot 2^4 + S_3 \cdot 2^3 + S_2 \cdot 2^2 + S_1 \cdot 2^1 + S_0 \cdot 2^0) \cdot \frac{V_{ref}}{2^6}
\]
ADC Example – Pipelined ADC

S/H → X 4 → S/H → X 4 → S/H → X 4 → S/H

ADC 3 bits → DAC 3 bits → ADC 3 bits → DAC 3 bits → ADC 2 bits

Calibration and Correction Circuit

d0 → d7
## ADC – Bits v.s. Throughput

<table>
<thead>
<tr>
<th>ADC</th>
<th>Bit-Length</th>
<th>Throughput</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash</td>
<td>~ 6 bits</td>
<td>100 M ~</td>
</tr>
<tr>
<td>Pipelined</td>
<td>8 ~ 16 bits</td>
<td>10 ~ 100 MHz</td>
</tr>
<tr>
<td>Sigma-Delta</td>
<td>14 ~ bits</td>
<td>~ 10 M</td>
</tr>
</tbody>
</table>
### ADC – Selection Matrix

<table>
<thead>
<tr>
<th>Bits</th>
<th>&lt;10kbps</th>
<th>10Kbps to 100Kbps</th>
<th>100Kbps to 1Mbps</th>
<th>1Mbps to 10Mbps</th>
<th>10 to 100Mbps</th>
<th>100Mbps +</th>
</tr>
</thead>
<tbody>
<tr>
<td>17+</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td></td>
<td>●</td>
</tr>
<tr>
<td>14-16</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>12-13</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>10-11</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>8-9</td>
<td></td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>&lt;8</td>
<td></td>
<td></td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
</tbody>
</table>

*From Analog Devices Inc.*
# AD775 – Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>AD775J (Typ)</th>
<th>AD775J (Max)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RESOLUTION</strong></td>
<td>8</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td><strong>DC ACCURACY</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integral Nonlinearity (INL)</td>
<td>+0.5</td>
<td>1.3</td>
<td>LSB</td>
</tr>
<tr>
<td>Differential Nonlinearity (DNL)</td>
<td>+0.3</td>
<td>+0.5</td>
<td>LSB</td>
</tr>
<tr>
<td>No Missing Codes</td>
<td>GUARANTEED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset</td>
<td>-10</td>
<td>-35</td>
<td>mV</td>
</tr>
<tr>
<td>To Top of Ladder VREF</td>
<td>0</td>
<td>+15</td>
<td>mV</td>
</tr>
<tr>
<td>To Bottom of Ladder VREF</td>
<td></td>
<td>445</td>
<td></td>
</tr>
<tr>
<td><strong>VIDEO ACCURACY</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Gain Error</td>
<td>1.0</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Differential Phase Error</td>
<td>0.5</td>
<td></td>
<td>Degrees</td>
</tr>
<tr>
<td><strong>ANALOG INPUT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Range (VREF – VSS)</td>
<td>2.0</td>
<td></td>
<td>V p-p</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>11</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td><strong>AC SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal-to-Noise and Distortion (S/N + D)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fN = 1 MHz</td>
<td>47</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>fN = 5 MHz</td>
<td>41</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Total Harmonic Distortion (THD)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fN = 1 MHz</td>
<td>-51</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>fN = 5 MHz</td>
<td>-42</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td><strong>REFERENCE INPUT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Input Resistance (RREF)</td>
<td>230</td>
<td>300</td>
<td>450</td>
</tr>
<tr>
<td>Case 1: VREF = VMAX, VSS = VMIN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Bottom Voltage (VSS)</td>
<td>0.60</td>
<td>0.64</td>
<td>0.68</td>
</tr>
<tr>
<td>Reference Span (VREF – VSS)</td>
<td>1.96</td>
<td>2.09</td>
<td>2.21</td>
</tr>
<tr>
<td>Reference Ladder Current (IREF)</td>
<td>4.4</td>
<td>7.0</td>
<td>9.6</td>
</tr>
<tr>
<td>Case 2: VREF = VMIN, VSS = AVSS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Span (VREF – VSS)</td>
<td>2.25</td>
<td>2.39</td>
<td>2.53</td>
</tr>
<tr>
<td>Reference Ladder Current (IREF)</td>
<td>5</td>
<td>8</td>
<td>11</td>
</tr>
<tr>
<td><strong>POWER SUPPLIES</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Voltages</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AVDD</td>
<td>+4.75</td>
<td>+5.25</td>
<td>Volts</td>
</tr>
<tr>
<td>DVDD</td>
<td>+4.75</td>
<td>+5.25</td>
<td>Volts</td>
</tr>
<tr>
<td>Operating Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IAVDD</td>
<td>9.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IDVDD</td>
<td>2.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IAVDD + IDVDD</td>
<td>12</td>
<td>17</td>
<td>mA</td>
</tr>
<tr>
<td><strong>POWER CONSUMPTION</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating</td>
<td>60</td>
<td>85</td>
<td>mW</td>
</tr>
<tr>
<td><strong>TEMPERATURE RANGE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating</td>
<td>-20</td>
<td>+75</td>
<td>°C</td>
</tr>
</tbody>
</table>

**NOTES**

1. NTSC 40 IRE modulation ramp. CLOCK = 14.3 MSPS.
2. fN amplitude = 0.3 dB full scale.
3. Specifications subject to change without notice. See Definition of Specifications for additional information.
11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
- ADC and DAC Circuit Structure
- **ADC/DAC Specification and Fault Models**
- IEEE Std. 1057
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing
ADC – Offset Error

• **Offset**: constant component of the error that is independent of the inputs

![Graph showing Offset Error](image)
**ADC – Gain Error**

- **Gain Error**: difference between the actual transfer ratio and the ideal ratio
- Also called Calibration Error

![Graph showing the difference between actual and ideal gain transfer](image)
**ADC – Nonlinearity Error**

**Nonlinearity error**: The deviation of the output quantity from a specified linear reference.
ADC – Nonlinearity Error

- **Integral Nonlinearity:**
  Worst-case deviation from the ideal transfer characteristic curve

- **Differential Nonlinearity:**
  Difference between the actual transfer ratio and the ideal ratio

IN = 2 LSB
DN = 0.5 LSB
**ADC – Temperature-Dependent Error**

- **Temperature-Dependent Error:** Due to the change in ambient temperature or temperature variation due to self-heating (temperature stability, temperature coefficient)

![Graph showing temperature-variant ADC responses](image)

\[ X_{out} \quad X_{in} \]

- Temperature-variant response \( T_1, T_2, T_3 \)
**Load Error**: Loading error is due to the effect of a load impedance upon the converter or signal source driving it.
**ADC – Hysteresis Error**

**Hysteresis Error**: The difference between the increasing and decreasing input values that produce the same output.
**ADC – Resolution Error**

- **Resolution Error**: The error due to the inability to respond to change of a variable smaller than a given increment.
ADC – Missing Code Error

Ideal Input Waveform

Quantized with missing Code

Quantization Error

Missing Codes
11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
- ADC and DAC Circuit Structure
- ADC/DAC Specification and Fault Models
- **IEEE Std. 1057**
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing
IEEE 1057 Standard

Scope

- Covers electronic digitizing waveform recorders, waveform analyzers and digitizing oscilloscopes with digital outputs.
- Applies to, but is not restricted to, general-purpose waveform recorders and analyzers.
IEEE 1057 Standard

Purpose

- Provides common methods for testing and terminology for describing the performance of waveform recorders.
- Benefits users and manufacturers of such devices.
- Presents many performance features, sources of error, and test methods.
### IEEE 1057 – General Information

<table>
<thead>
<tr>
<th>Model Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimensions and weight</td>
</tr>
<tr>
<td>Power Requirement</td>
</tr>
<tr>
<td>Environmental conditions (tem., humidity, EMC/EMI, etc.)</td>
</tr>
<tr>
<td>Any special or peculiar characteristics</td>
</tr>
<tr>
<td>Available options and accessories</td>
</tr>
<tr>
<td>Exception to the above parameters where applicable</td>
</tr>
<tr>
<td>Calibration interval</td>
</tr>
</tbody>
</table>
### IEEE 1057 – Minimum Specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of digitizing bits</td>
<td>Input impedance</td>
</tr>
<tr>
<td>Sample rates</td>
<td>Analog bandwidth</td>
</tr>
<tr>
<td>Memory length</td>
<td>Input signal ranges</td>
</tr>
</tbody>
</table>
### IEEE 1057 – Additional Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>Fixed error in sample time</td>
</tr>
<tr>
<td>Offset</td>
<td>Trigger delay and jitter</td>
</tr>
<tr>
<td>Differential nonlinearity</td>
<td>Trigger sensitivity</td>
</tr>
<tr>
<td>Integral nonlinearity</td>
<td>Trigger minimum rate of change</td>
</tr>
<tr>
<td>Harmonic distortion</td>
<td>Trigger hysteresis band</td>
</tr>
<tr>
<td>Spurious response</td>
<td>Trigger coupling to signal</td>
</tr>
<tr>
<td>Maximal static error</td>
<td>Crosstalk</td>
</tr>
<tr>
<td>Signal to noise ratio</td>
<td>Monotonicity</td>
</tr>
<tr>
<td>Effective bits</td>
<td>Hysteresis</td>
</tr>
<tr>
<td>Peak error</td>
<td>Over voltage recovery</td>
</tr>
<tr>
<td>Random noise</td>
<td>Word error rate</td>
</tr>
<tr>
<td>Frequency response</td>
<td>Cycle time</td>
</tr>
<tr>
<td>Settling time</td>
<td>Common mode rejection ratio</td>
</tr>
<tr>
<td>Slew limit</td>
<td>Differential input impedance</td>
</tr>
<tr>
<td>Overshoot and precursors</td>
<td>Maximum operating common</td>
</tr>
<tr>
<td>Aperture uncertainty</td>
<td>Mode signal level</td>
</tr>
<tr>
<td>Long-term stability</td>
<td>Transition duration of step response</td>
</tr>
<tr>
<td>Maximum common mode signal level</td>
<td></td>
</tr>
</tbody>
</table>
# IEEE 1057 – Test Methods

<table>
<thead>
<tr>
<th>General methods</th>
<th>Triggering</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input impedance</td>
<td>Crosstalk</td>
</tr>
<tr>
<td>Gain and offset</td>
<td>Monotonicity</td>
</tr>
<tr>
<td>Noise</td>
<td>Hysteresis</td>
</tr>
<tr>
<td>Analog bandwidth</td>
<td>Overvoltage Recovery</td>
</tr>
<tr>
<td>Frequency response</td>
<td>Word Error Rate</td>
</tr>
<tr>
<td>Step Response parameters</td>
<td>Cycle Time</td>
</tr>
<tr>
<td>Time base errors</td>
<td>Differential Input Specification</td>
</tr>
<tr>
<td>Linearity, harmonic distortion, and spurious responses</td>
<td></td>
</tr>
</tbody>
</table>
11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
- ADC and DAC Circuit Structure
- ADC/DAC Specification and Fault Models
- IEEE Std. 1057
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing
Histogram – Code Bins

Code Bin

<table>
<thead>
<tr>
<th>Code Level</th>
<th>Bin Count $H[k]$</th>
<th>Code Width $W[k]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T[1]$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T[2]$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T[3]$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T[4]$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T[5]$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T[6]$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>302</td>
<td>529</td>
<td>472</td>
<td>345</td>
<td>372</td>
<td>456</td>
<td>543</td>
<td>245</td>
</tr>
</tbody>
</table>

**Test Methods - Code Transition Level**

**Static Test Method**
- Start from 2% below the transition level.
- Take a number of samples.
- Adjust the input level until the 50% codes are greater than k.

![Diagram showing code transition levels and precision percentages](image)

<table>
<thead>
<tr>
<th>Code Bin</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>T[6]</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T[6]</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T[5]</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T[4]</td>
<td>45</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T[3]</td>
<td>443</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T[2]</td>
<td>454</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T[1]</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Samples</th>
<th>64</th>
<th>256</th>
<th>1024</th>
<th>4096</th>
</tr>
</thead>
<tbody>
<tr>
<td>Precision</td>
<td>45%</td>
<td>23%</td>
<td>12%</td>
<td>6%</td>
</tr>
</tbody>
</table>

% of rms noise
**Test Methods - Code Transition Level**

**Dynamic Test Method**
- Apply full range sine wave
- Calculate the transition level from the bin counts

\[
T[k] = C - A \cos \left( \frac{\pi \cdot H_c[k - 1]}{M} \right)
\]

- **A**: Amplitude  
- **C**: Offset
- **\(H_c[j]\)**: The code count of bin j.
- **M**: Total number of samples
- **Record Length M and Number of Cycles Mc must not have common term.**

<table>
<thead>
<tr>
<th>[H_c[j]]</th>
<th>(T[k])</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>245</td>
</tr>
<tr>
<td>6</td>
<td>543</td>
</tr>
<tr>
<td>5</td>
<td>456</td>
</tr>
<tr>
<td>4</td>
<td>372</td>
</tr>
<tr>
<td>3</td>
<td>345</td>
</tr>
<tr>
<td>2</td>
<td>472</td>
</tr>
<tr>
<td>1</td>
<td>529</td>
</tr>
<tr>
<td>0</td>
<td>302</td>
</tr>
</tbody>
</table>
Test Methods - Gain and Offset

- Apply a slow ramp signal
- Construct the code bin table

\[ G \cdot T[k] + V_{os} + \varepsilon[k] = Q \cdot (k - 1) + T_1 \]

\[ V_{os} = T_1 + Q \left(2^N - 1\right) - \frac{G}{2^{N-1}} \sum_{k=1}^{2^{N-1}} T[k] \]

\[ G = Q \frac{\left(2^N - 1\right)^2 \sum_{k=1}^{2^{N-1}} kT[k]}{\left(2^N - 1\right)^2 \sum_{k=1}^{2^{N-1}} T^2[k] - \left(\sum_{k=1}^{2^{N-1}} T[k]\right)^2} - Q \frac{\left(2^N - 1\right) \sum_{k=1}^{2^{N-1}} T[k]}{\left(2^N - 1\right) \sum_{k=1}^{2^{N-1}} T^2[k] - \left(\sum_{k=1}^{2^{N-1}} T[k]\right)^2} \]
Test Methods - Gain and Offset (Example)

Transfer Curves

Histograms

Ideal  Gain Error  Offset Error  Game/Offset

128  128  128  128
**Test Methods - Nonlinearity**

**Differential Nonlinearity**

\[
DNL \[k\] = \frac{G \cdot W[k] - Q}{Q}
\]

**Integral Nonlinearity**

\[
INL = 100 \max \left| \frac{\varepsilon[k]}{Q \cdot 2^N} \right|
\]

**Maximal Static Error**

\[
MSE = 100 \max \left| \frac{T[k] - Q(k - 1) - T_1}{Q \cdot 2^N} \right|
\]
Test Methods - Sine Wave Fitting

- Try to fit the sine wave to find the gain $A'$, offset $C_0$, and phase shift $\theta$.
- There are matrix based and nonmatrix methods.

\[
\begin{align*}
(y_1, y_2, \cdots y_m) &= \left( t_1, t_2, \cdots t_m \right) \\
y_i &= A \sin \omega t_i + C_0 \\
y_i' &= A' \sin(\omega t_i + \theta) + C \\
y_i' &= A \sin(\omega t_i) + B \cos(\omega t_i) + C \\
\min \left[ \sum_{i=1}^{m} (y_i - A \cos(\omega t_i) - B \cos(\omega t_i) - C)^2 \right]
\end{align*}
\]
**Test Methods - Sine Wave Fitting**

**Original Signal:**  
\[ y(t) = A_o \sin(\omega_o t) + C_o \]

**Curve Fitted:**  
\[ y'(t) = A \sin(\omega t) + B \cos(\omega t) + C \]

**Gain Error:**  
\[ \frac{\sqrt{A^2 + B^2} - A_o}{A_o} \]

**Offset Error:**  
\[ C - C_o \]

**Phase Error:**  
\[ \theta = \tan^{-1}\left(-\frac{B}{A}\right) \]

**Frequency Error:**  
\[ \frac{\omega - \omega_o}{\omega_o} \]
11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
- ADC and DAC Circuit Structure
- ADC/DAC Specification and Fault Models
- IEEE Std. 1057
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing
ADC – Frequency Domain Testing

• Similar to Analog AC Testing
• Apply sinusoidal waveform
• Do Fourier transform on response waveform
• Obtain F domain properties mathematically.
**ADC – Frequency Domain Testing**

\[
THD = 10 \log \left( \frac{F^2}{\sum H_i^2} \right) = 100 \times \frac{F^2}{\sum H_i^2} \% 
\]

\[
SNR = 10 \log \frac{F^2}{\sum N_i^2} 
\]

\[
SNDR = 10 \log \frac{F^2}{\sum H_i^2 + \sum N_i^2} 
\]
11.4 IEEE Std. 1149.4 Standard for a Mixed-Signal Test Bus

- IEEE Std. 1149.4 Overview
- IEEE Std. 1149.4 Circuit Structures
- IEEE Std. 1149.4 Instructions
- IEEE Std. 1149.4 Test Modes
IEEE 1149.4 - Overview

- Target mixed signal Printed Circuit Assembles (PCA).
- Components:
  - Mixed Signal
  - Digital
  - Analog
  - Discrete

M: Mixed-signal Component
A: Analog Component
D: Digital Component

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IEEE 1149.4 - Scope

- Provide standardized approaches to
  - Interconnect Test
  - Parametric Test
  - Internal Test
IEEE 1149.4 - Interconnect Test

Open Defects

Short Defects
IEEE 1149.4 - Parametric Test

Simple Interconnect

Extended Interconnect

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11.4 IEEE Std. 1149.4 Standard for a Mixed-Signal Test Bus

- IEEE Std. 1149.4 Overview
- **IEEE Std. 1149.4 Circuit Structures**
- IEEE Std. 1149.4 Instructions
- IEEE Std. 1149.4 Test Modes
IEEE 1149.4 - ABM

Test Control Circuitry
TAP Controller

CUT

VTH VH VL VG

CD

AB1 AB2

AT1 AT2

TBIC

Core Circuit

AB1 AB2

IEEE 1149.4

ABM

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1149.4 – Mixed-Signal Architecture

- Digital Inputs
- Analog Inputs
- TDI
- ABM
- Digital Outputs
- DBM
- Analog Outputs
- TDO

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11.4 IEEE Std. 1149.4 Standard for a Mixed-Signal Test Bus

- IEEE Std. 1149.4 Overview
- IEEE Std. 1149.4 Circuit Structures
- **IEEE Std. 1149.4 Instructions**
- IEEE Std. 1149.4 Test Modes
IEEE 1149.4 - Instructions

- Mandatory Instructions
  - BYPASS
  - SAMPLE/PRELOAD
  - EXTEST
  - PROBE

- Same as IEEE 1149.1
IEEE 1149.4 - Instructions

- Optional Instructions
  - INTEST
  - IDC/USERCODE
  - RUNBISt
  - CLAMP
  - HIGHZ

- Same as IEEE 1149.1
11.4 IEEE Std. 1149.4 Standard for a Mixed-Signal Test Bus

- IEEE Std. 1149.4 Overview
- IEEE Std. 1149.4 Circuit Structures
- IEEE Std. 1149.4 Instructions
- IEEE Std. 1149.4 Test Modes
1149.4 – Open/Short Interconnect Test

Chip 1

AB1

AB2

VH

VL

Chip 2

AB1

AB2

VTH

0

1
1149.4 — Extended Interconnect Test

- Grounded Impedance Measurement
- Apply current and measure voltage
1149.4 — Extended Interconnect Test

- Equivalent Circuit Model.

\[ I_{DUT}(t) = I_s(t) \cdot \frac{R_{SIO}}{R_{SIO} + Z_{P1} + Z_{DUT}} \]

\[ V_M(t) = V_{DUT}(t) \cdot \frac{R_{SVI}}{R_{SVI} + Z_{P2} + Z_{DUT}} \]
1149.4 – Extended Interconnect Test

- Floating Impedance Zd Measurement
1149.4 — Extended Interconnect Test

- Floating Impedance $Z_D$ with optional $V_g$
1149.4 – Extended Interconnect Test

- Apply voltage and measure current
1149.4 – Extended Interconnect Test

• Equivalent Circuit Model

\[
V_{\text{DUT}}(t) = V_s(t) \cdot \frac{Z_{\text{DUT}}}{R_{\text{SVO}} + Z_{P1} + Z_{\text{DUT}} + Z_{P2} + R_{\text{SII}}}
\]

\[
I_m(t) = \frac{V_s(t)}{R_{\text{SVO}} + Z_{P1} + Z_{\text{DUT}} + Z_{P2} + R_{\text{SII}}}
\]

With Ideal Voltage Source and Current Meter

\[
V_{\text{DUT}}(t) = V_s(t) \cdot \frac{Z_{\text{DUT}}}{Z_{P1} + Z_{\text{DUT}} + Z_{P2}}
\]

\[
I_m(t) = \frac{V_s(t)}{Z_{P1} + Z_{\text{DUT}} + Z_{P2}}
\]
1149.4 – Extended Interconnect Test

• Measure complex interconnect network
### 1149.4 – Extended Interconnect Test

![Diagram of an interconnect test circuit](image)

#### Notations
- **Vs**: Apply Voltage
- **Vm**: Measure Voltage
- **Is**: Apply Current
- **Im**: Measure Current

#### Formulas
- \( h_{11} = \frac{V_1}{I_1} \bigg|_{V_2 = 0} \)
- \( h_{21} = \frac{I_2}{I_1} \bigg|_{V_2 = 0} \)
- \( h_{12} = \frac{V_1}{V_2} \bigg|_{I_1 = 0} \)
- \( h_{22} = \frac{I_2}{V_2} \bigg|_{I_1 = 0} \)

#### Table of Test Conditions

<table>
<thead>
<tr>
<th>H</th>
<th>P1</th>
<th>P2</th>
<th>P3</th>
<th>P4</th>
</tr>
</thead>
<tbody>
<tr>
<td>h11</td>
<td>Is/Vm</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>h12</td>
<td>Vm</td>
<td>GND</td>
<td>Vs</td>
<td>GND</td>
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<tr>
<td>h21</td>
<td>Is</td>
<td>GND</td>
<td>Im</td>
<td>GND</td>
</tr>
<tr>
<td>h22</td>
<td>Open</td>
<td>GND</td>
<td>Vs/Im</td>
<td>GND</td>
</tr>
</tbody>
</table>

- **Notations**
  - Is: Apply Current
  - Vm: Measure Voltage
  - Vs: Apply Voltage
  - Im: Measure Current
1149.4 - High Speed Applications

- Use buffers for better frequency response

- Current Buffer
- Voltage Buffer

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11.5 Concluding Remarks

- AMS testing requires specialized approaches and experienced engineers because of the large varieties of signals, functions and circuits.
- DSP approaches are so pervasive that even basic analog test items can be accomplished.
- IEEE 1057 with formal terminologies and standardized test methods provides a solid theoretical background for ADC/DAC testing.
- IEEE 1149.4 is one solution to extending and incorporating the digital counterpart.