Chapter 11

Analog and Mixed-Signal Testing

What is this chapter about?

- Introduces AMS circuits, failure modes and fault models.
- Addresses analog testing, including DC and AC parametric testing.
- Discusses mixed-signal circuits, ADC and DAC, and their testing approaches.
- Studies IEEE Std. 1149.4, the standard for mixed-signal test buses

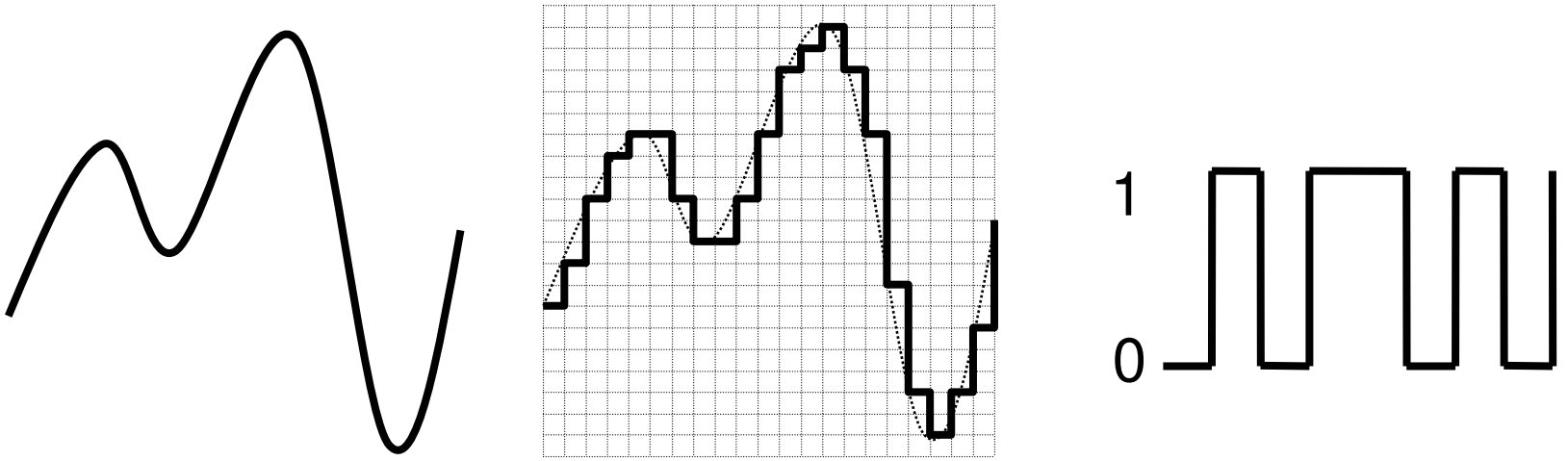
Chapter 11
Analog and Mixed-Signal Testing

- Introduction
- Analog Circuit Testing
- Mixed-Signal Testing
- IEEE Std. 1149.4 Standard for Mixed-Signal Test Bus
- Concluding Remarks

11.1 Introduction

- **Analog Circuit Properties**
- Analog Defect Mechanism and Fault Models

Analog, Digital, and Mixed-Signal Signals



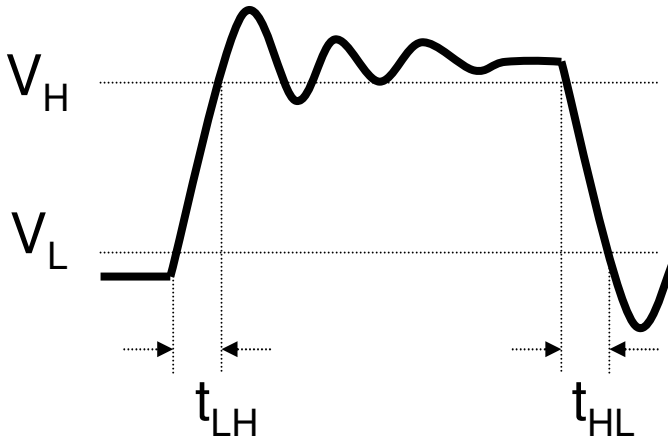
Analog Mixed-Signal Digital

Analog Circuit Properties

- Continuous Signal
- Large Range of Circuits
- Nonlinear Characteristics
- Feedback Ambiguity
- Complicated Cause-Effect Relationship
- Absence of Suitable Fault Model
- Accurate Measurements Required

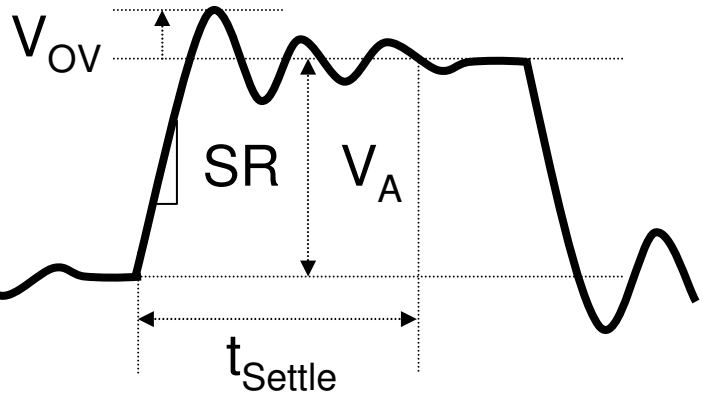
Properties - Continuous Signal

Digital Signal



- Logic 1, Logic 0
- VIH, VIL, VOH, VOL
- Rise Time, Fall Time
- Propagation Delay H-L/L-H
- Noise Margin High/Low

Analog Signal



- Voltage/Current
- Slew Rate
- Overshoot
- Damping Factor
- Frequency
- Bandwidth

Properties - Large Ranges of Circuits

Digital Circuits

- Operation
  - Static Logic
  - Dynamic Logic
- Structure
  - Gates
  - PLA
  - Memory

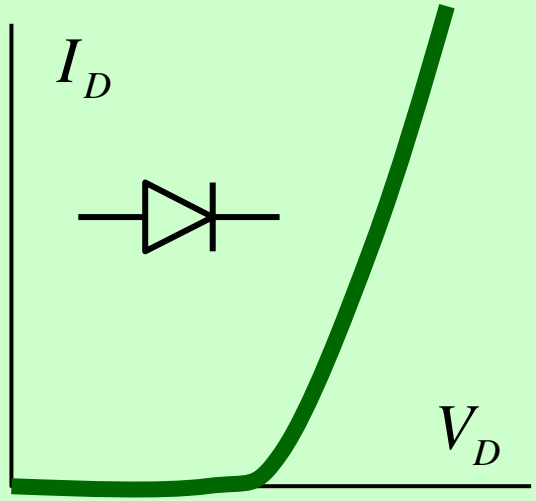
Analog Circuits

- Operation
  - Current Mode
  - Voltage Mode
  - Switching Cap
- Structure
  - Amplifier
  - Multiplier
  - Rectifier
  - Resonator

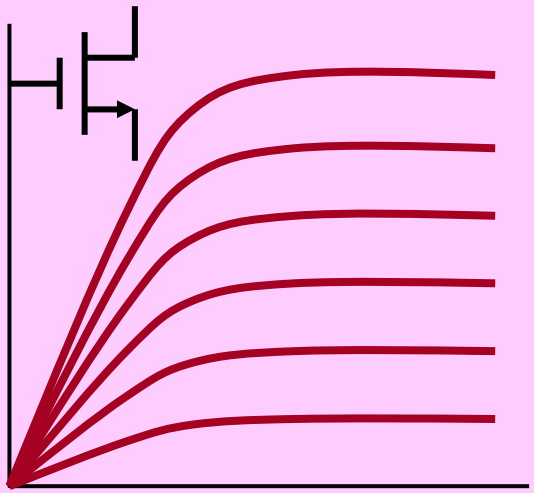
Properties- Nonlinear Characteristics

- Analog circuits are nonlinear in nature
- Nonlinear cause effect

$$I_D = I_s \cdot e^{V_D / n \times V_T}$$

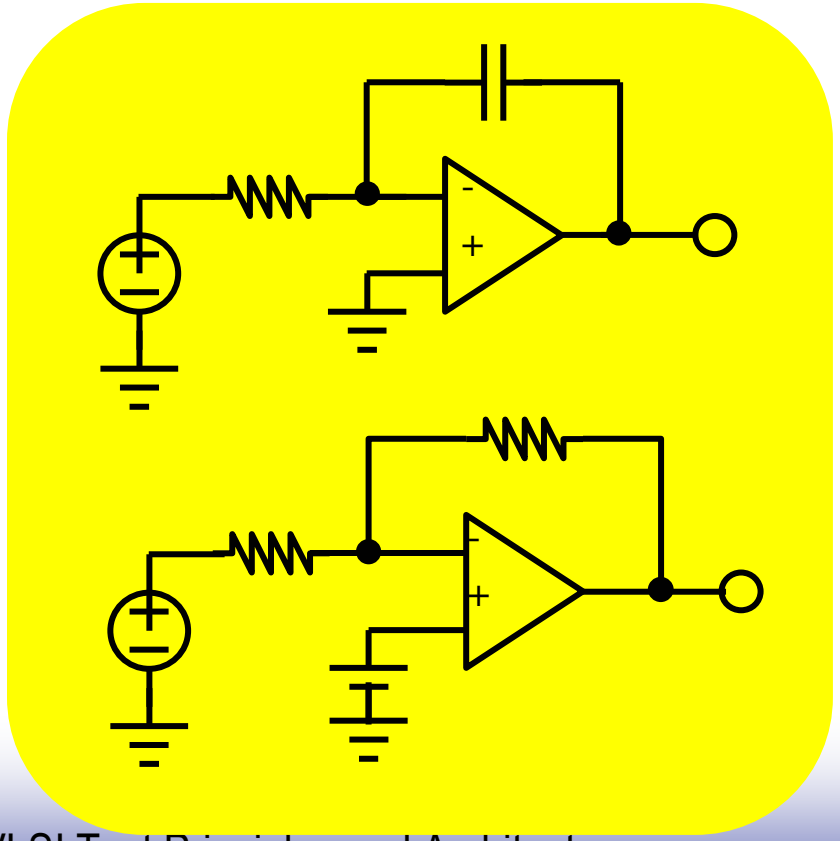


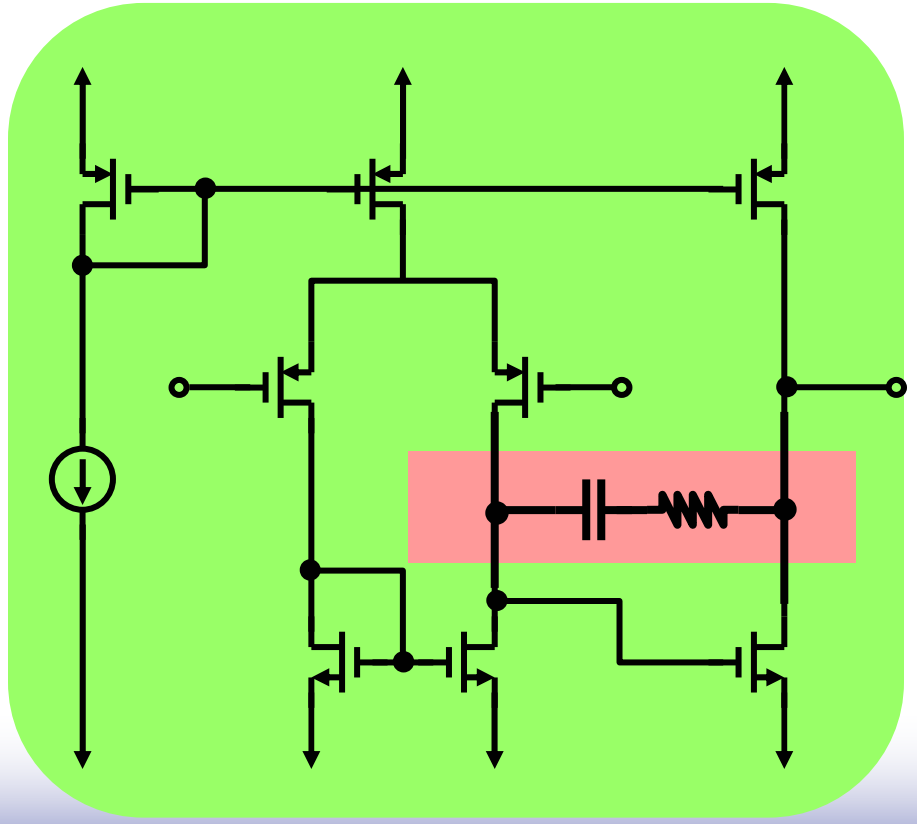
$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_t)^2$$



Properties- Feedback Ambiguities

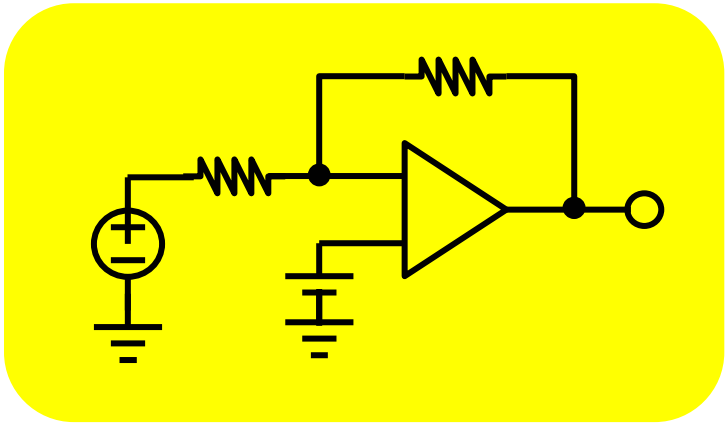
- Feedback puts circuit parameters together
- Difficult to identify fault location



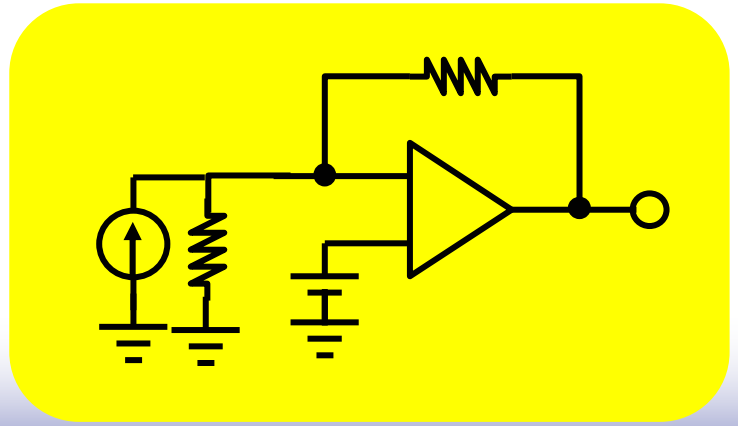


Properties- Complicated Cause-Effect Relationship

- Difficult to determine the cause of error.



$$A_V = \frac{V_0}{V_i} = -\frac{R_2}{R_1}$$



$$A = \frac{V_0}{V_i} = -\frac{A}{(1+\frac{A}{R_2})R_1}$$

Properties – Absence of Suitable Fault Models

Digital Faults

- Good Logic Fault Model
- Generally Accepted
  - Stuck-at-1, Stuck-at-0
  - Stuck-Open, Stuck-On
  - Short. Open
  - Memory Faults
  - PLA Faults

Properties - Absence of Suitable Fault Models

Analog Faults

- No Good Fault Model
- Not Generally Accepted
  - Open Short
  - Missing/Extra Devices
  - Parameter Variation
  - Performance Deviation
  - Circuit Structure Related
  - Functional Faults
  - ??????????

Properties – Accurate Measurements Required

Digital Instrument

- Oscilloscope
- Function Generator
- Logic Analyzer
- Frequency Counter

Properties – Accurate Measurements Required

Analog Instrument

- Oscilloscope
- Function Gen
- Freq. Counter
- Spectrum Analyzer
- Network Analyzer
- Impedance Analyzer
- Timing Analyzer
- Communication Analyzer
- RF Instrument
- Optical Instrument
- Microwave Instrument

11.1 Introduction

- Analog Circuit Properties
- **Analog Defect Mechanism and Fault Models**

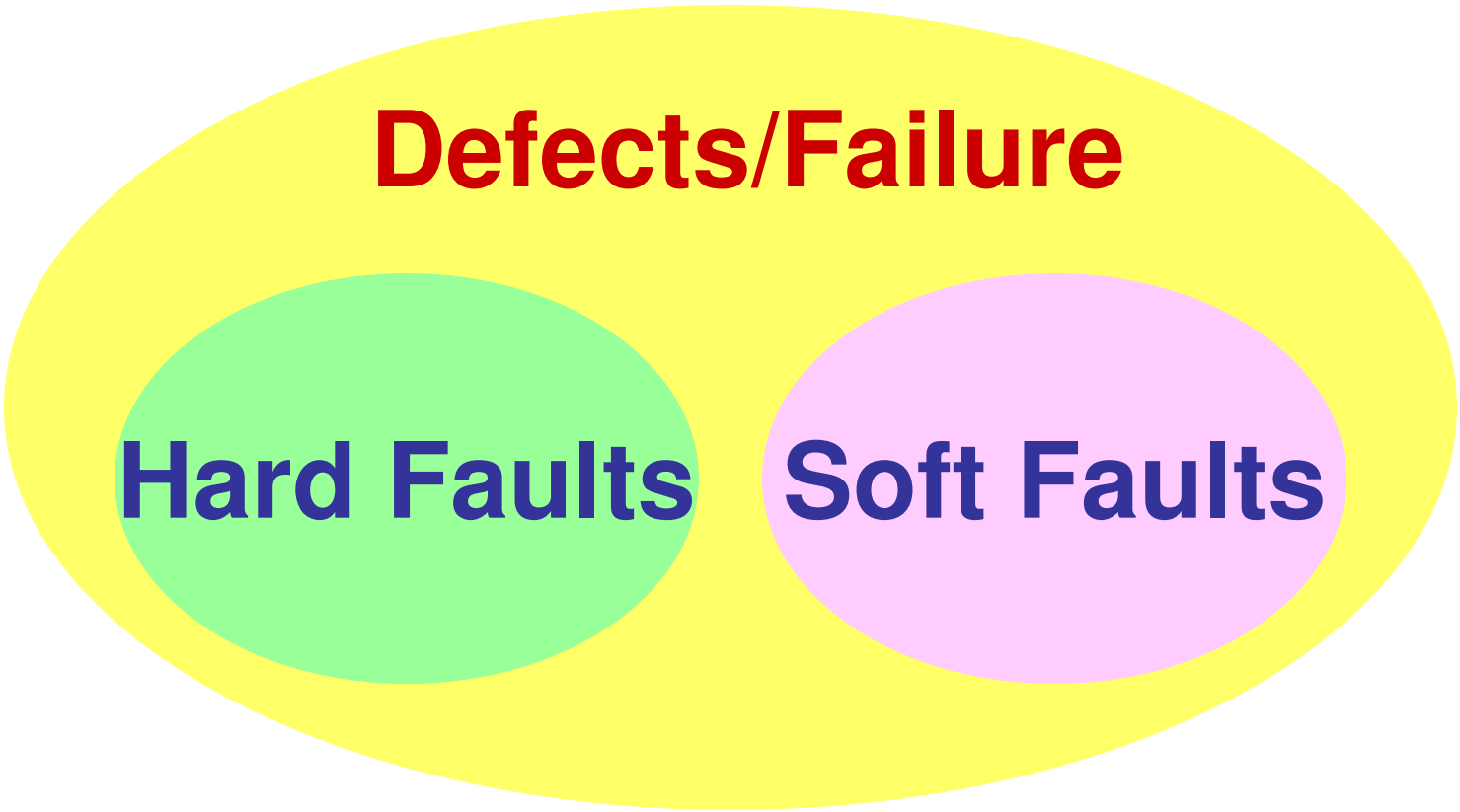
Defect Mechanisms (1)

- **Material Defects**
  - cracks
  - crystal imperfection
  - surface impurities
  - ion migration
- **Processing Faults**
  - oxide thickness
  - mobility change
  - impurity density
  - diffusion depth
  - dielectric constants
  - metal sheet resistance
  - missing contacts
  - dust

Defect Mechanisms (2)

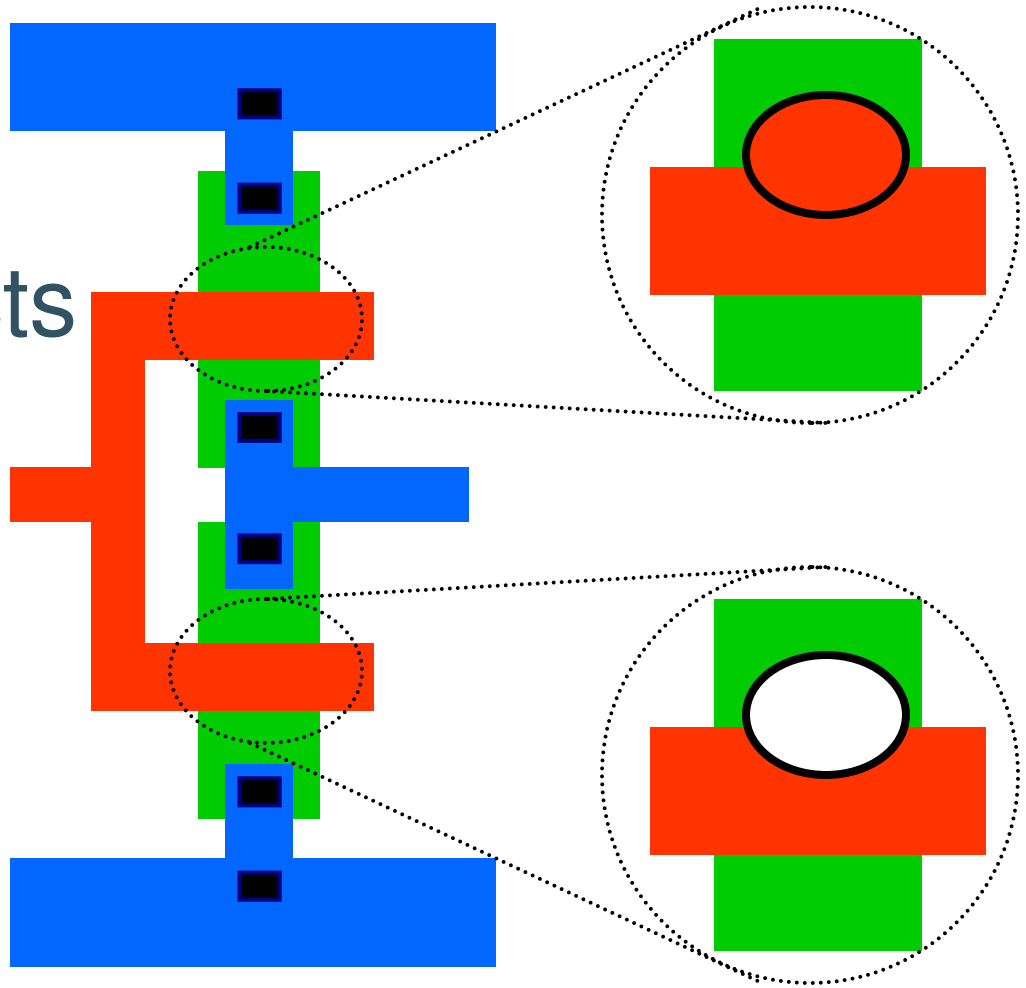
- **Time-Dependent Failures**
  - dielectric breakdown
  - electron migration
- **Packaging Failures**
  - contact degradation
  - seal leakage

Analog Fault Model



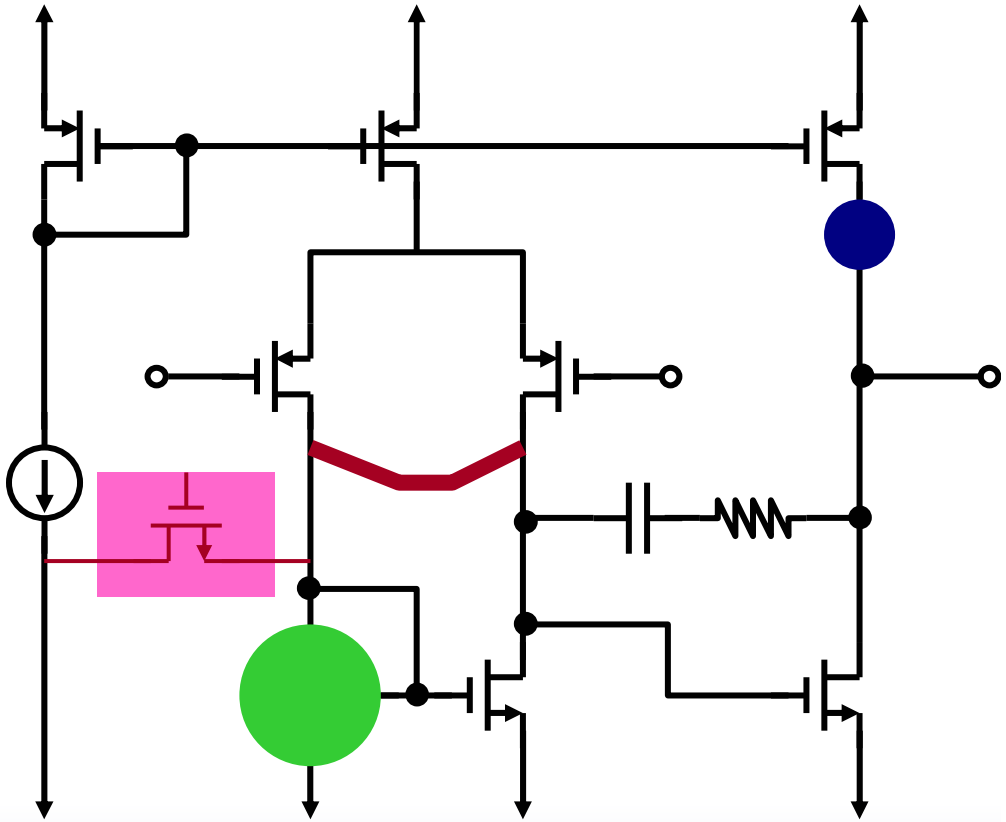
Analog Faults - Defect

- Defects
  - Extra Defects
  - Etching Defects
- Source
  - Dust
  - Lithography
- Layout Oriented
- Statistical Model



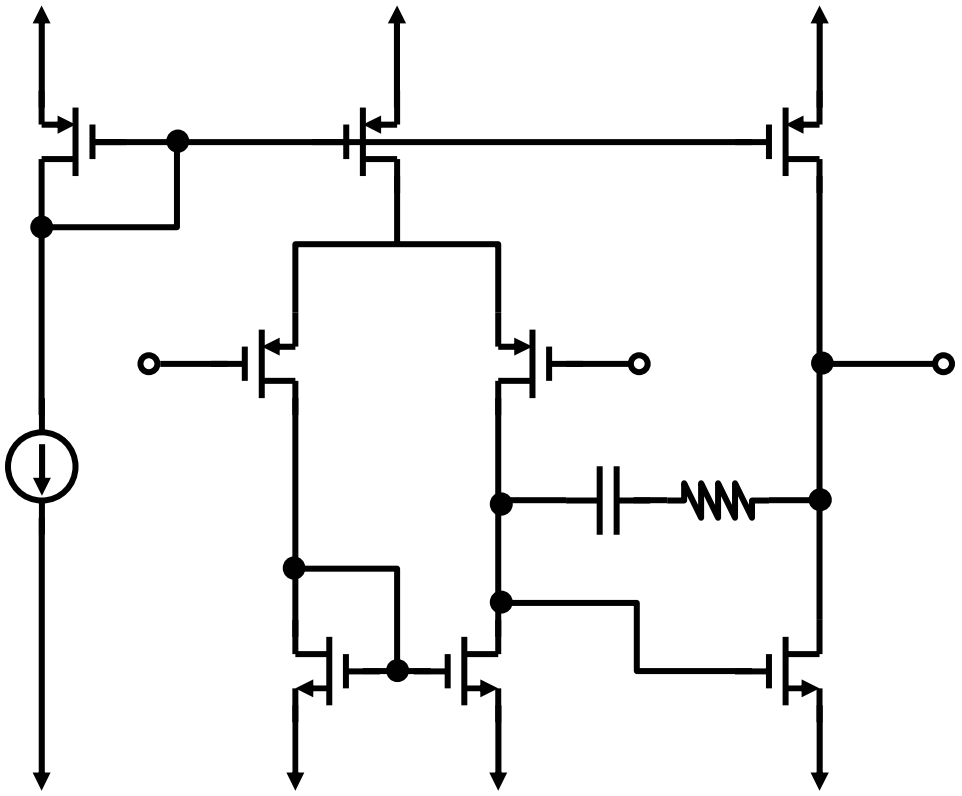
Analog Faults - Hard Faults

- Fault Models
  - Open
  - Short
  - Missing Device
  - Extra Devices
- Faulty Effects
  - Catastrophic Error
  - Module Malfunction
  - System Failure

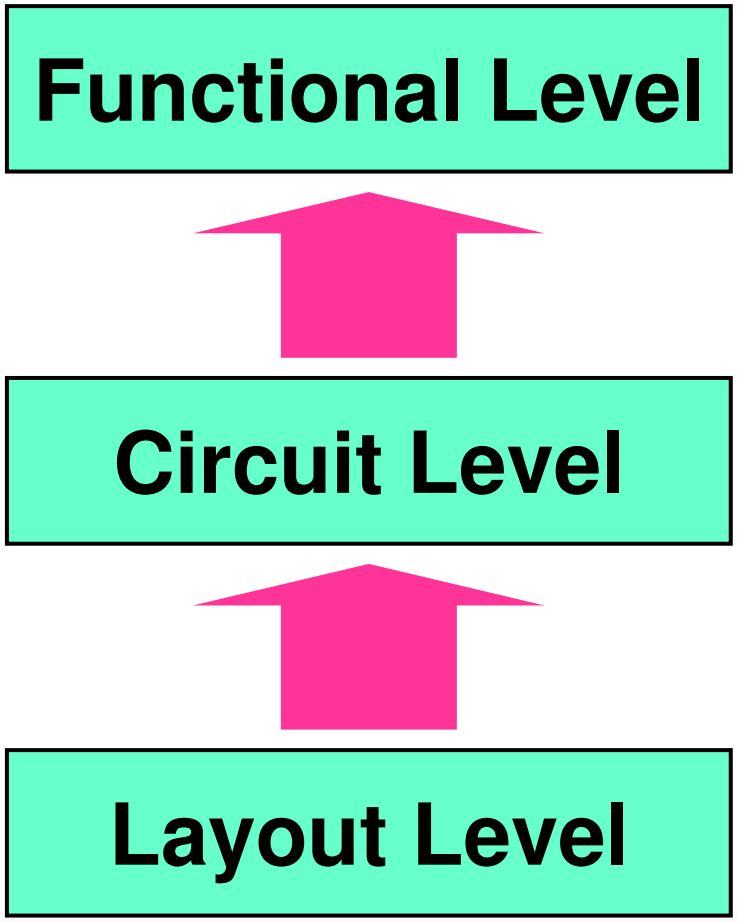


Analog Faults - Soft Faults

- Parametric Faults
  - *Io: 100uA -> 50uA*
  - *W: 20um -> 10um*
- Deviation Faults
  - *fo: 10MHz -> 5MHz*
  - *Gain: 10000 -> 2000*
- Sources
  - Mobility
  - Oxide Thickness
  - Impurity Density
  - Defusion Depth
  - Dielectric Constants
  - Metal Sheet Resistance

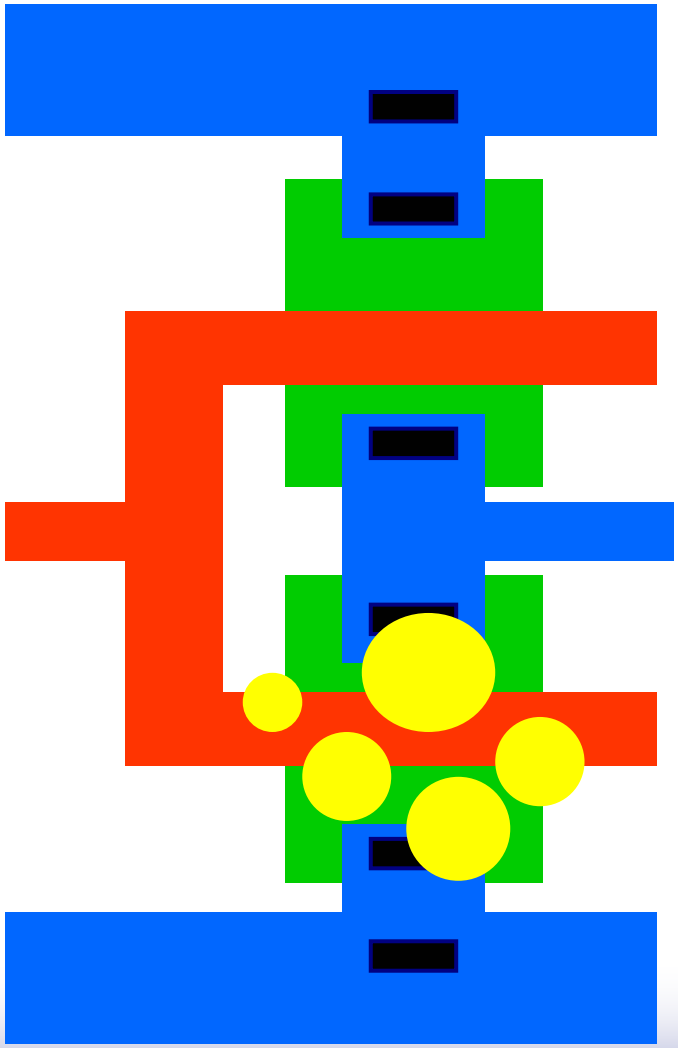


Analog Fault - Model Mapping



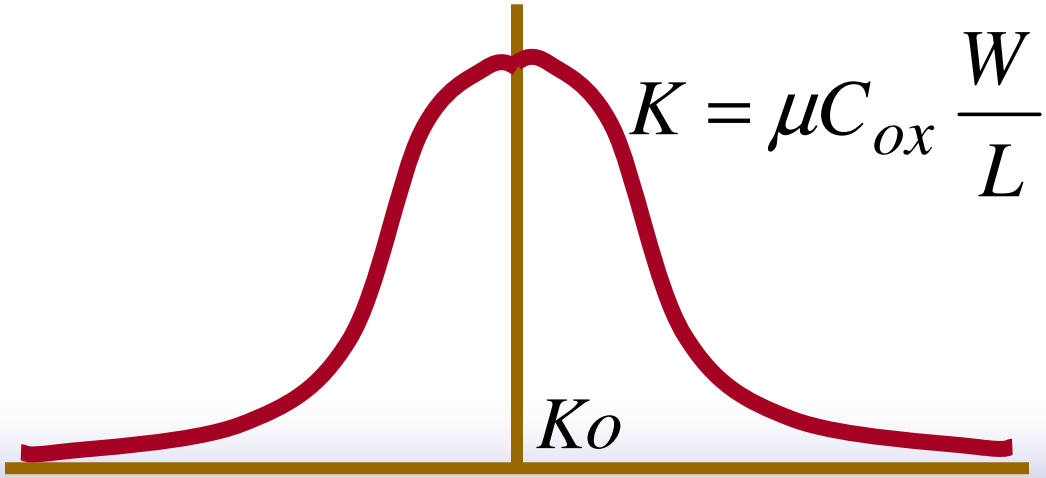
- Deviation Faults
- Parametric Faults
- Extra Defects
- Etching Defects

Analog Faults - Model Mapping



Layout to Parametric

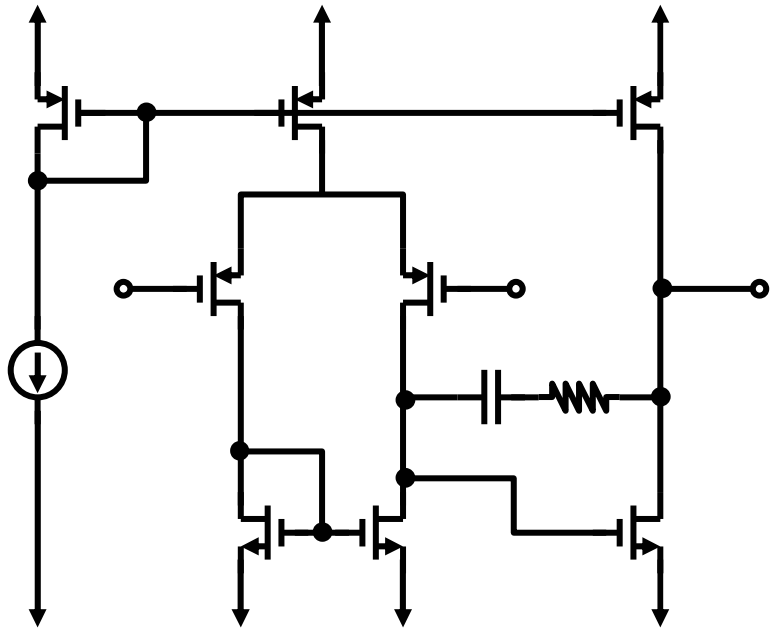
- Defect Statistics
  - Randomly insert dusts of random size.
- Parameter Statistics
  - Simulate the effect of dust on transistor parameters



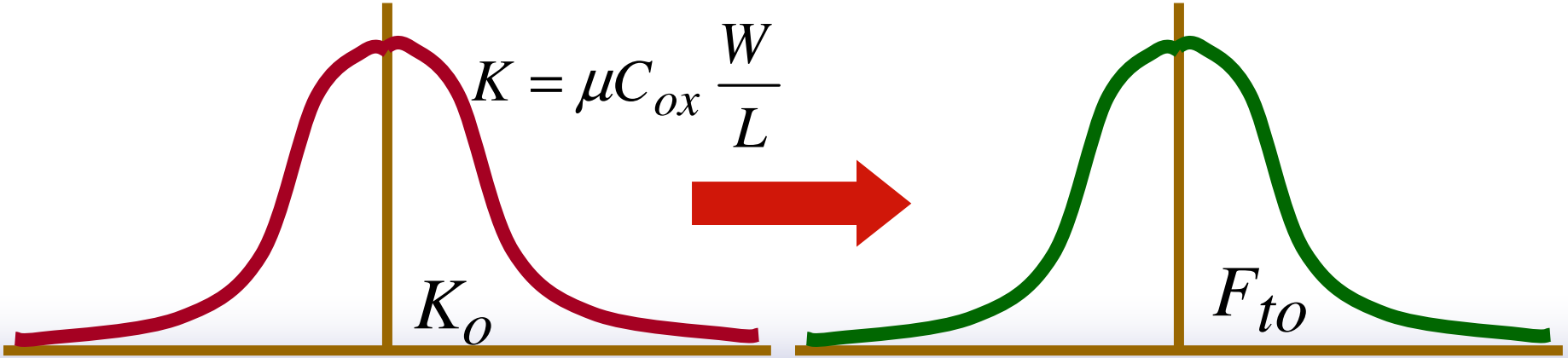
Analog Faults - Model Mapping

Parametric to Deviation

- Use SPICE simulation and statistics to derive the performance deviation.



$$K = \mu C_{ox} \frac{W}{L}$$



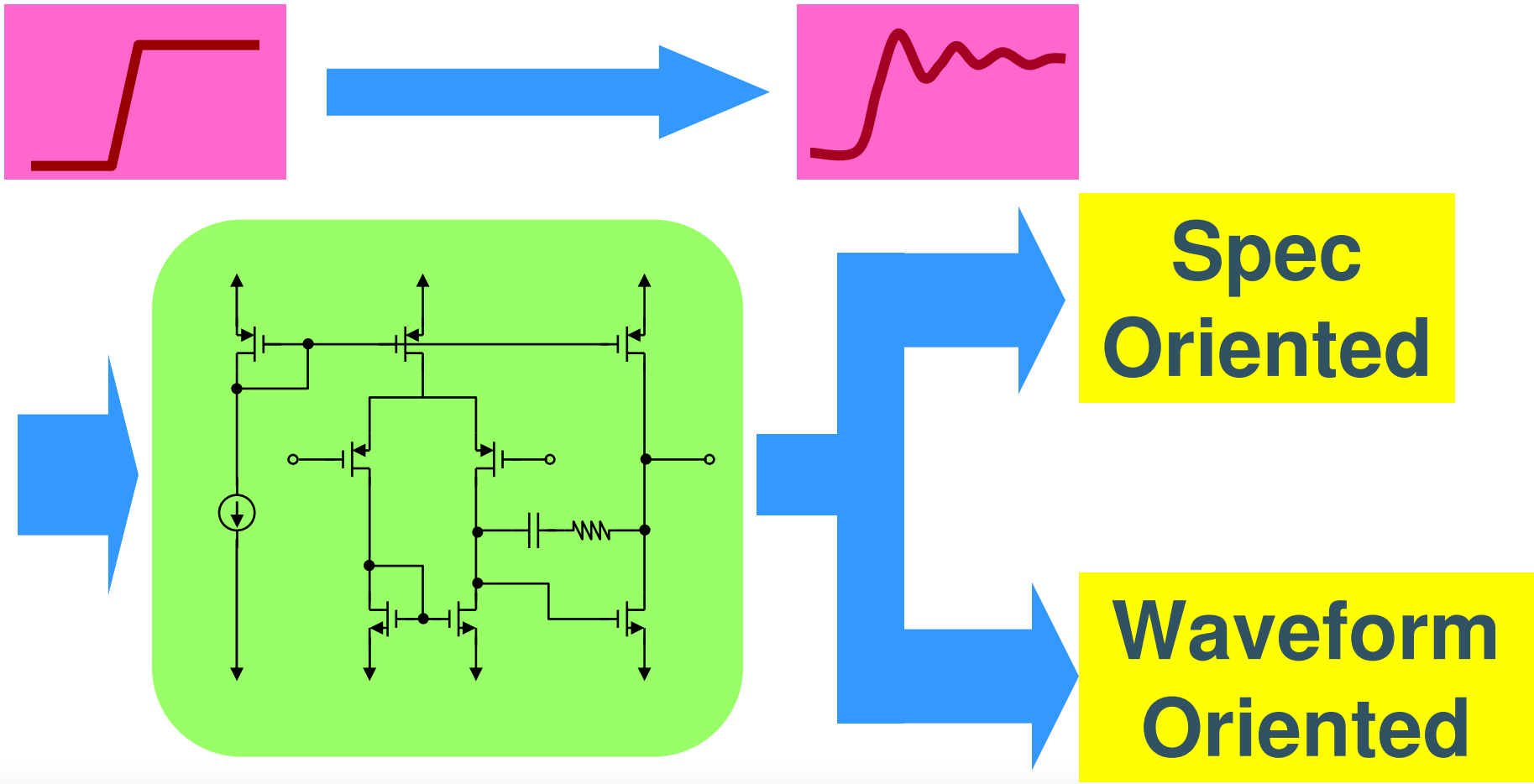
11.1 Summary

- Studied the analog test properties
  - Nonlinearity, Feedback Ambiguity
  - No good fault model
- Overview the analog test plan
  - Test Code, Binning, Sequence Control
  - Focused Calibrations, DIB Checkers
  - Characterization and Simulation Code
- Analog Fault Model
  - Extra and Etching Defects
  - Parametric and Deviation faults
  - Model Mapping

11.2 Analog Circuit Testing

- **Analog Test Approaches**
- Analog Test Waveforms
- DC Parametric Testing
- AC Parametric Testing

Analog Testing



Specification Oriented Test

OP777/OP727/OP747–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C unless otherwise noted.)

Analog Devices, Inc.™

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage OP777	V_{OS}	+25°C < T_A < +85°C		20	100	µV
		–40°C < T_A < +85°C		50	200	µV
Offset Voltage OP727/OP747		+25°C < T_A < +85°C		30	160	µV
		–40°C < T_A < +85°C		60	300	µV
Input Bias Current	I_B	–40°C < T_A < +85°C		5.5	11	nA
Input Offset Current	I_{OS}	–40°C < T_A < +85°C		0.1	2	nA
Input Voltage Range			0		4	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4 V	104	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to 4.5 V	300	500		V/mV
Offset Voltage Drift OP777	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +85°C		0.3	1.3	µV/°C
Offset Voltage Drift OP727/OP747	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +85°C		0.4	1.5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA, –40 °C to +85 °C	4.88	4.91		V
Output Voltage Low	V_{OL}	I_L = 1 mA, –40 °C to +85 °C		126	140	mV
Output Circuit	I_{OUT}	$V_{DROPOUT}$ < 1 V		±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 30 V	120	130		dB
Supply Current/Amplifier OP777	I_{SY}	V_O = 0 V		220	270	µA
		–40°C < T_A < +85°C		270	320	µA
Supply Current/Amplifier OP727/OP747		V_O = 0 V		235	290	µA
		–40°C < T_A < +85°C		290	350	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.2		V/µs
Gain Bandwidth Product	GBP			0.7		MHz
NOISE PERFORMANCE						
Voltage Noise	e_nP-p	0.1 Hz to 10 Hz		0.4		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.13		pA/√Hz

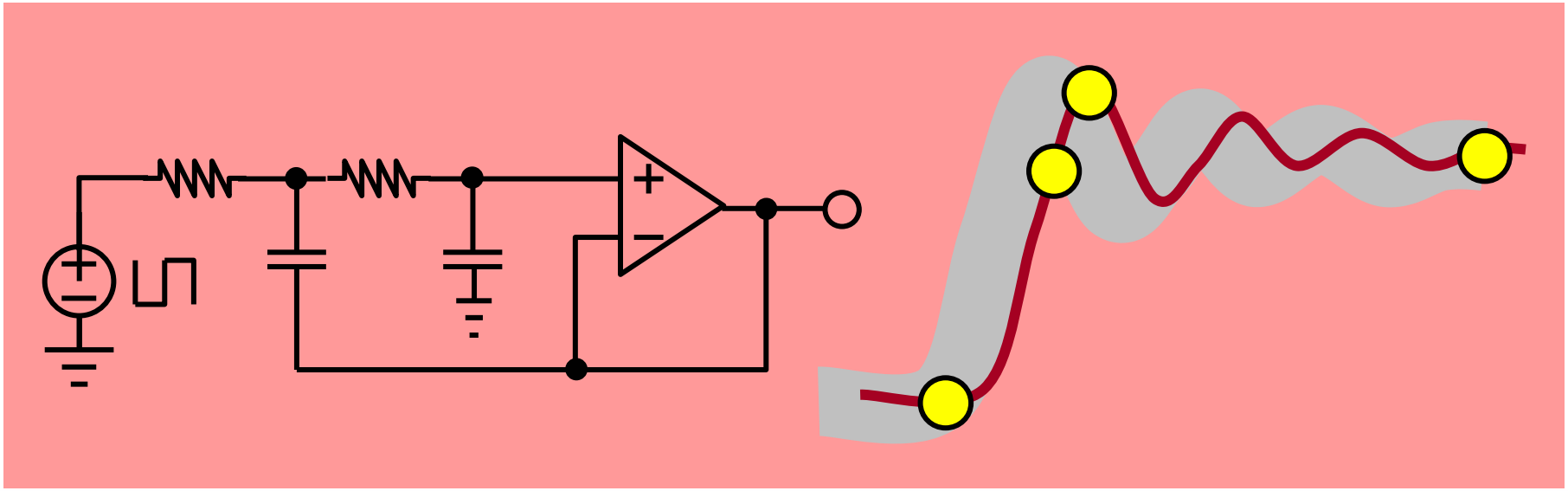
NOTES
Typical specifications: >50% of units perform equal to or better than the "typical" value.
Specifications subject to change without notice.

Specification Oriented Test

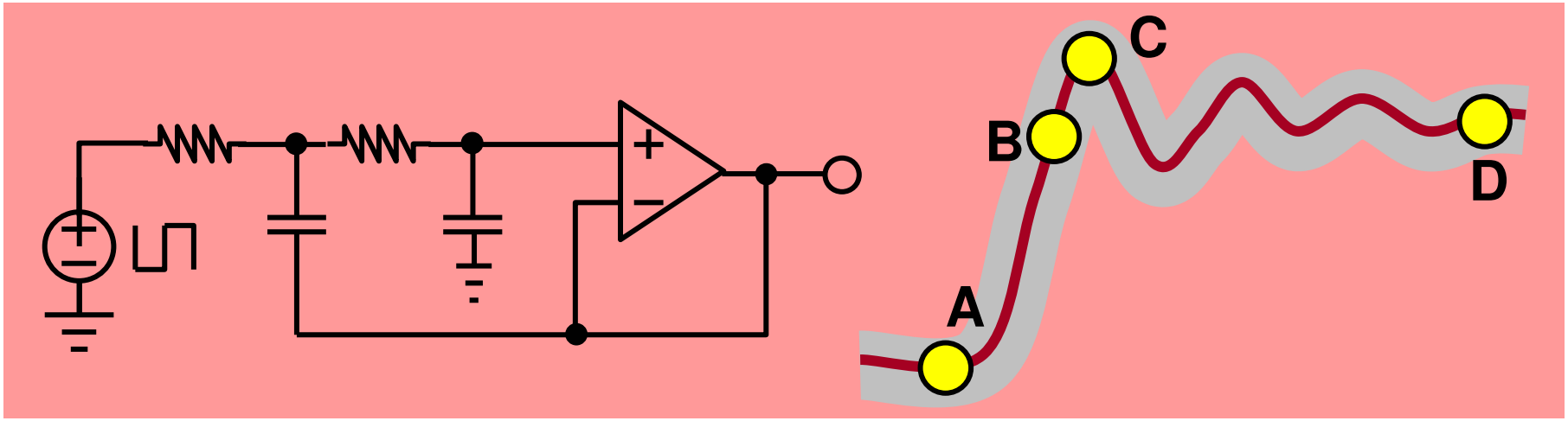
- Specification Oriented Test
  - Check whether all the specs are met
  - Tedious and inflexible
- Example: Operational Amplifier
  - DC Specifications
    - Input Offset Voltage
    - Input Bias Offset Current
    - Open-Loop Gain
    - Noise
    - Common Rejection Ratio
    - Temperature Drift
  - AC Specifications
    - Bandwidth
    - Harmonic Distortion
    - Slew Rate
    - Settling Time
    - Noise

Waveform Oriented Test

- Waveform Oriented Test
  - Compare waveform to the simulated ones



Waveform Oriented Test



A	DC Bias, Input Offset
B	Slew Rate, Damping Factor
C	Overshoot, Damping Factor, Bandwidth
D	Settling Time, DC Gain

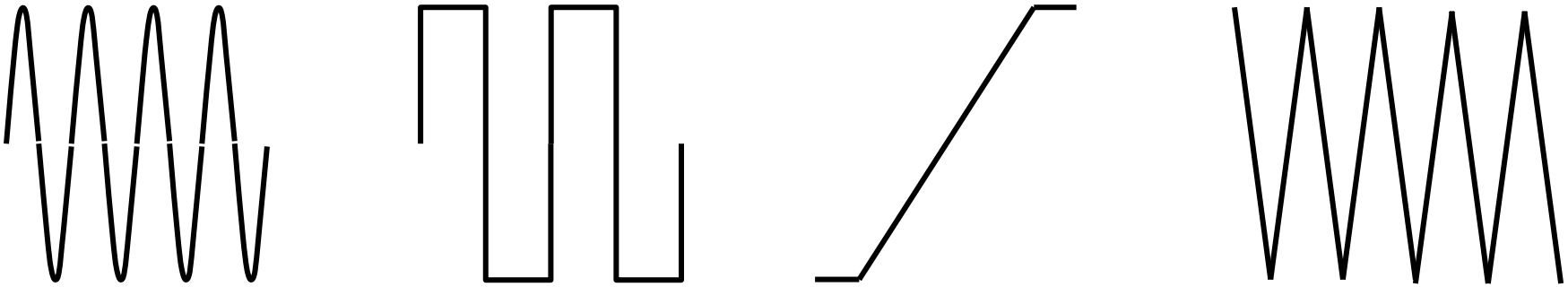
Analog Testing - Comparison

- Specification Oriented Test
  - Require more test runs and time
  - Require accurate instrument
  - Specifications are guaranteed
  - ***Low defect level***
- Waveform Oriented Test
  - Less test runs and test time
  - More forgiving on instrument
  - Specifications are not guaranteed
  - ***Low cost***

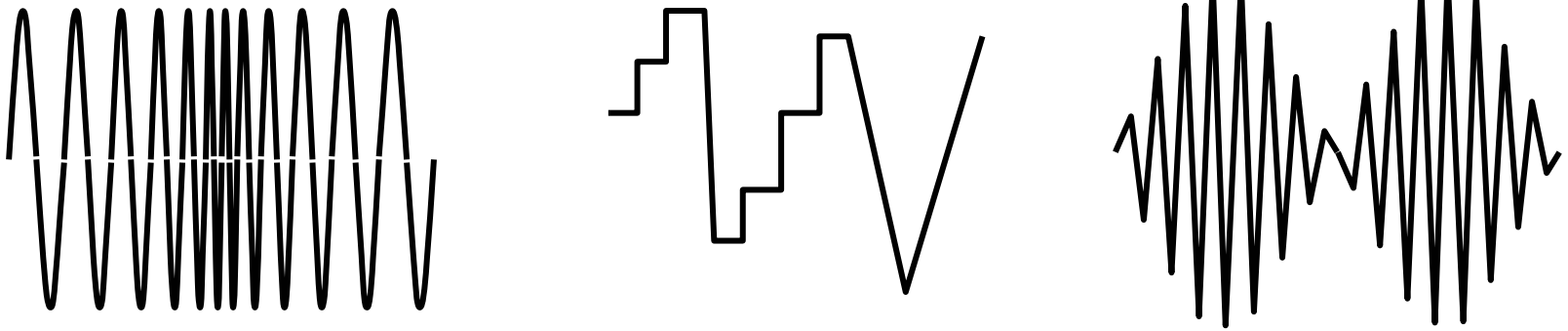
11.2 Analog Circuit Testing

- Analog Test Approaches
- **Analog Test Waveforms**
- DC Parametric Testing
- AC Parametric Testing

Analog Test Waveforms



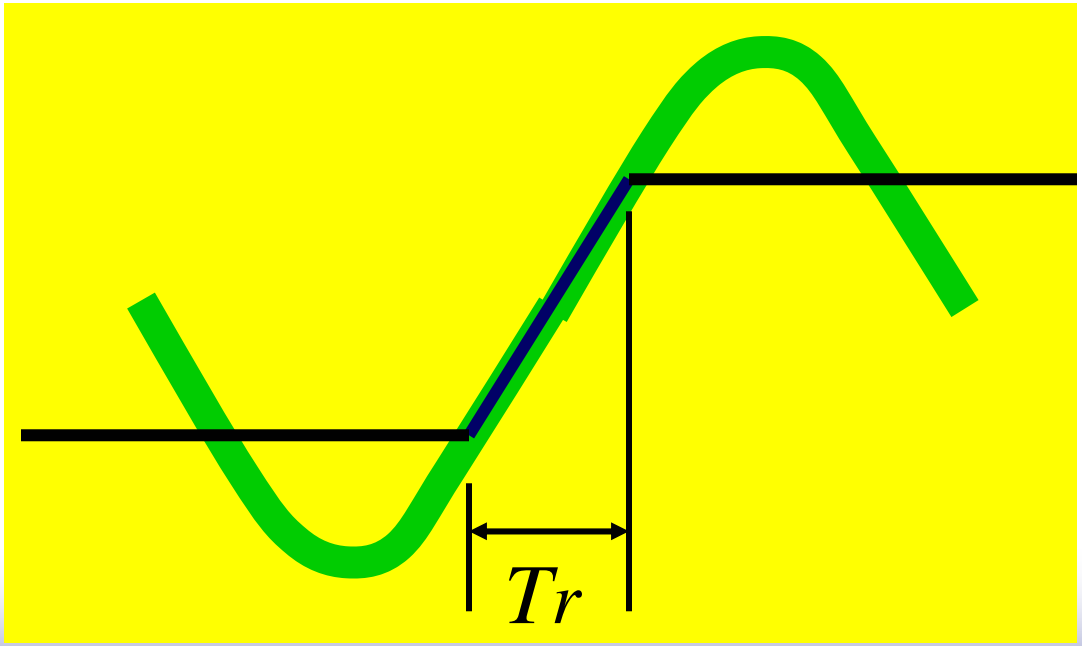
Sine Square (Step) Ramp Triangular



Chirp (Sweep Sine) Arbitrary Modulated

Waveform - Step

- For transient response testing
- Application: Filter, OPs, VCO, etc
- Difficult to generate good steps



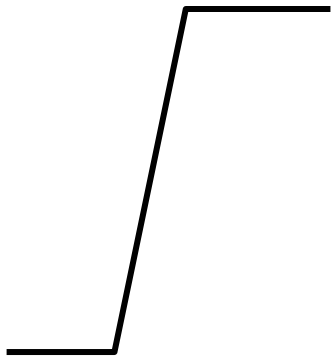
$$\theta = \pm 45^{o} \sim \pm 60^{o}$$

$$f = \frac{1}{(4 \sim 3)T_r}$$

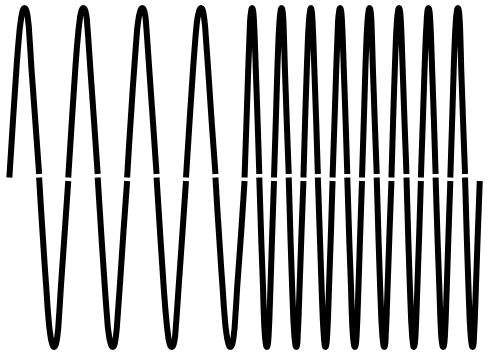
$$f = \frac{1}{3.5T_r}$$

Waveform - Step

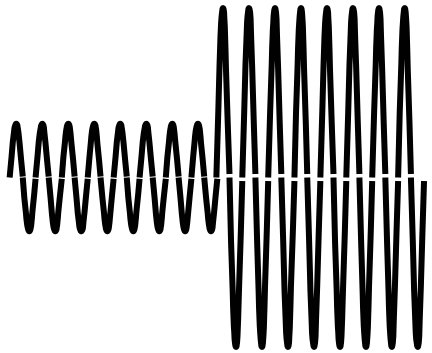
- Step change in voltage: Transient testing
- Step change in frequency: PLL testing
- Step change in amplitude: AGC testing



Voltage Step



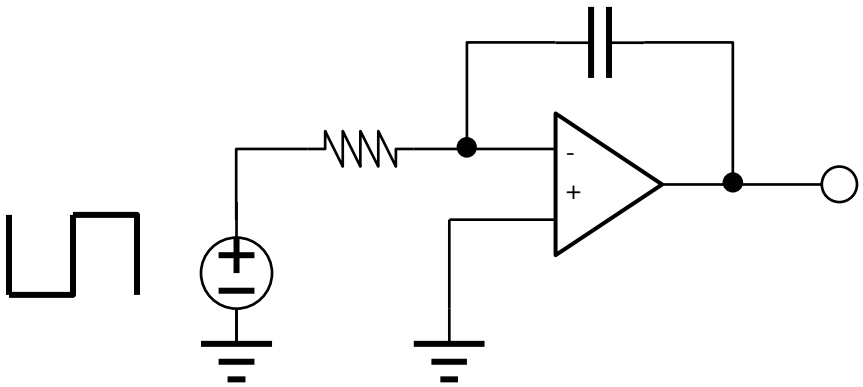
Frequency Step

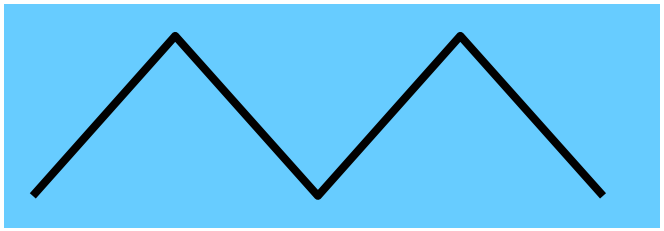


Amplitude Step

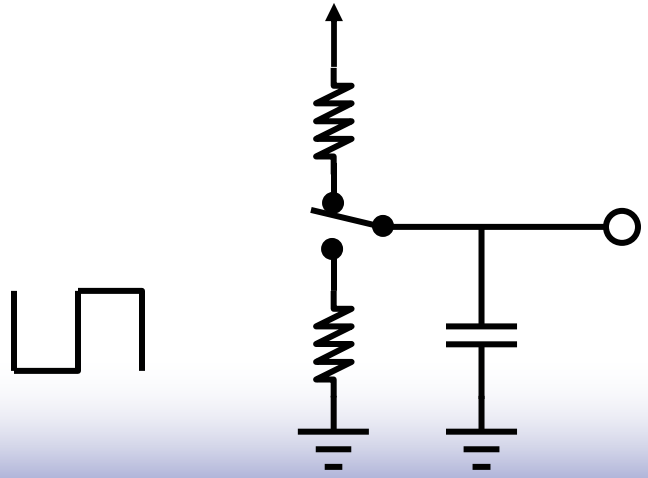
Waveform - Ramp

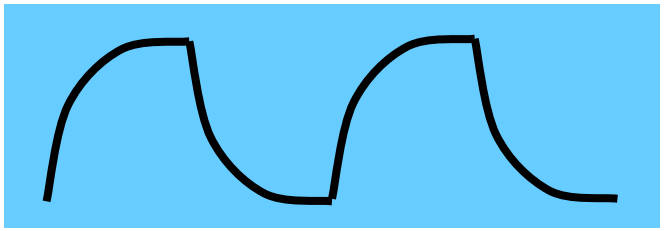
- Triangular Wave Generation





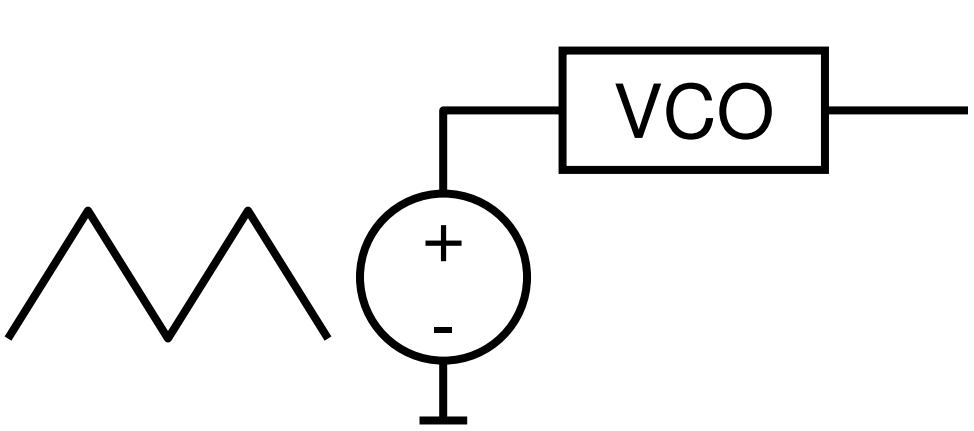
- Sawtooth Wave Generation

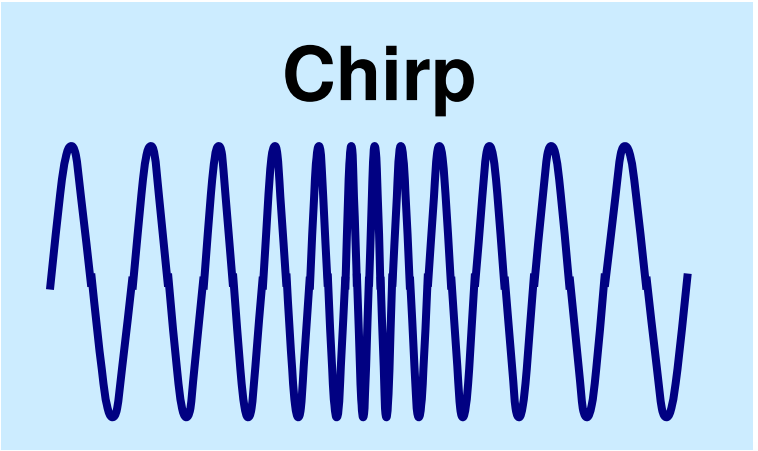




Waveform - Chirp

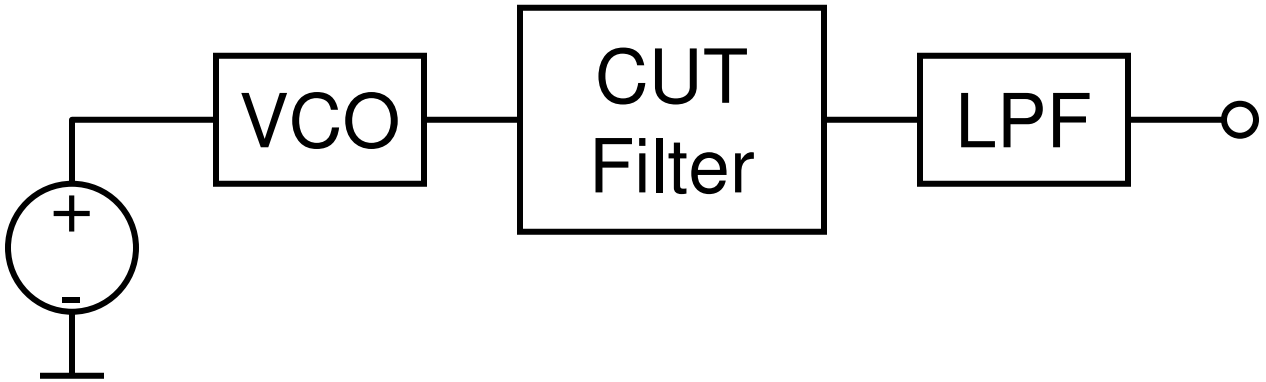
- Also called Sweep Sine
- Generation: Triangular to VCO
- Application: Frequency response plotting

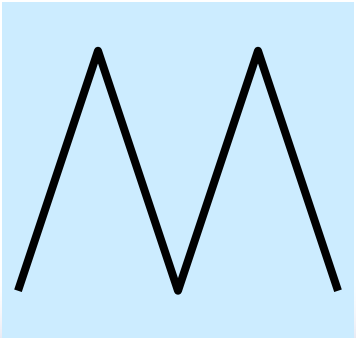


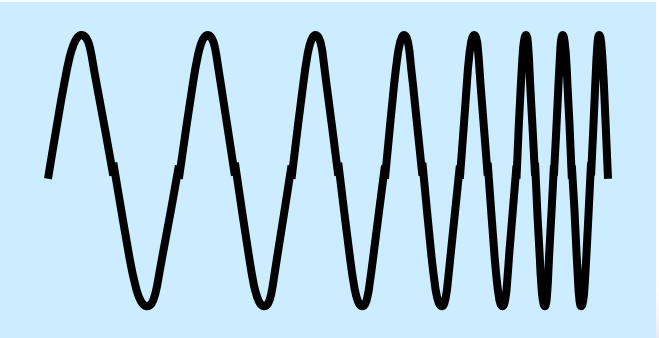


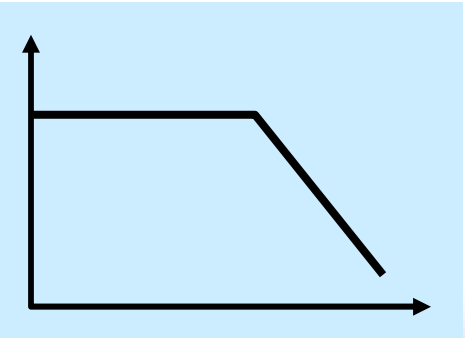
Waveform - Chirp

- Application: Frequency response plotting



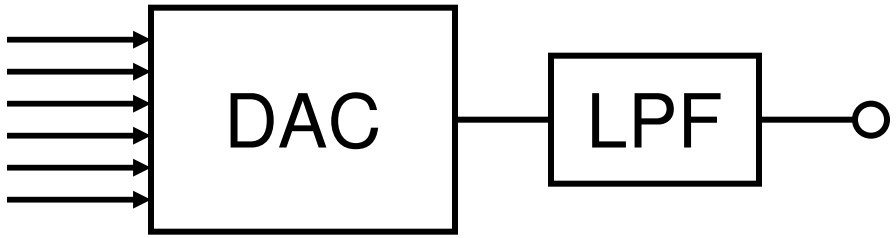


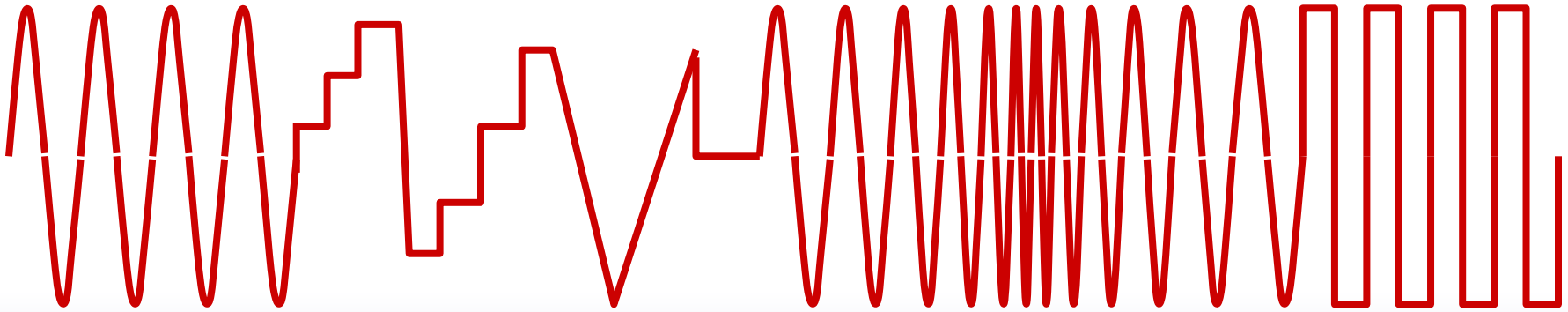




Waveform - Arbitrary

- Synthesized by DACs
- Combinations of all kinds of waveform





Waveform - Modulated/Synthesized

- Modulated/Synthesized Waveforms
  - Communication System Testing
    - GSM, CDMA, 1394, USB2, etc.
  - Modulation
    - AM, FM, PCM, PWM, QAM, PSK, QPSK
- Generated by dedicated instrument

11.2 Analog Circuit Testing

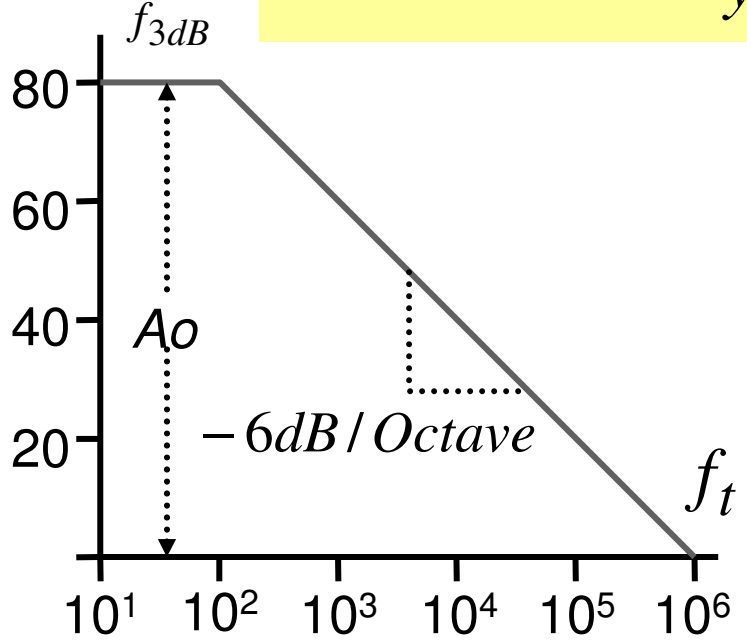
- Analog Test Approaches
- Analog Test Waveforms
- DC Parametric Testing
- AC Parametric Testing

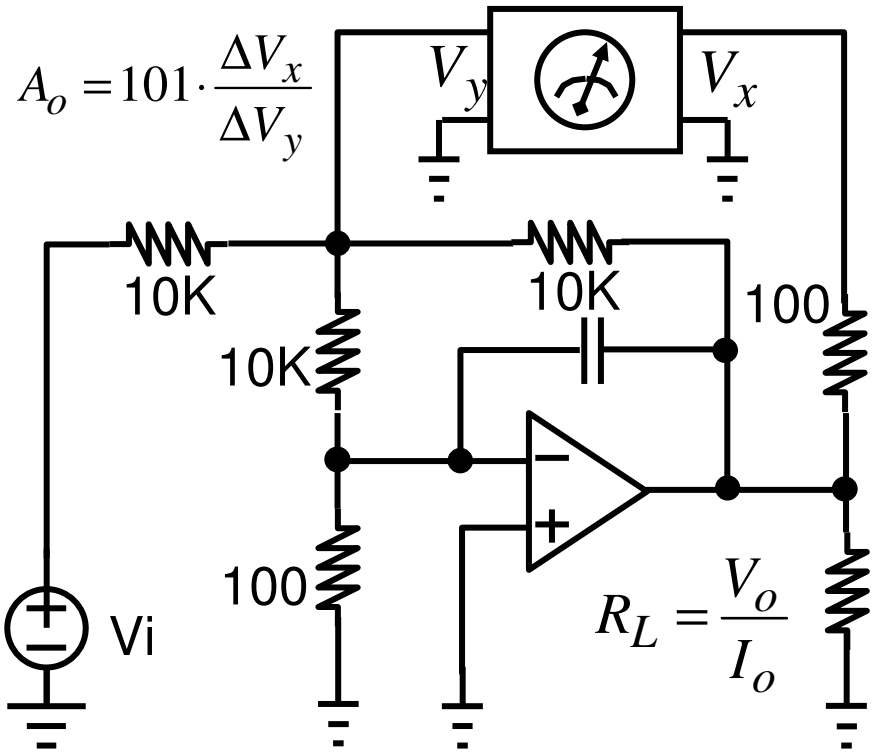
DC Parametric Testing

Rated output current	Rated output voltage
Open-loop gain	Slewing rate
Unity gain full power response	Unity gain small signal response
Overload recovery	Input bias current
Input offset voltage	Input offset current
Input noise	Input impedance
Supply voltage sensitivity	Common mode rejection
Maximum voltage between inputs	Maximum common mode voltage
Temperature drift	Source: [Sata 1967]

DC Test – Open-Loop Gain Measurement

$$A_o = 101 \cdot \frac{\Delta V_x}{\Delta V_y}$$

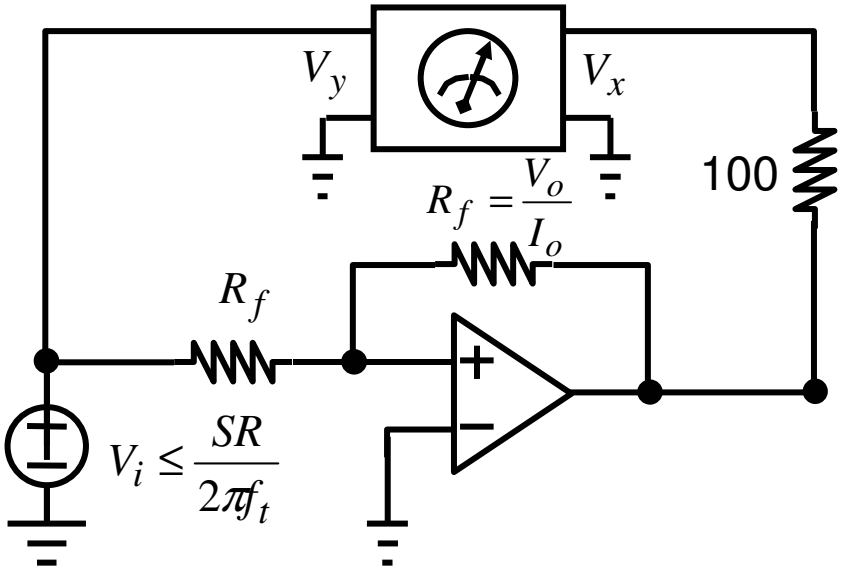




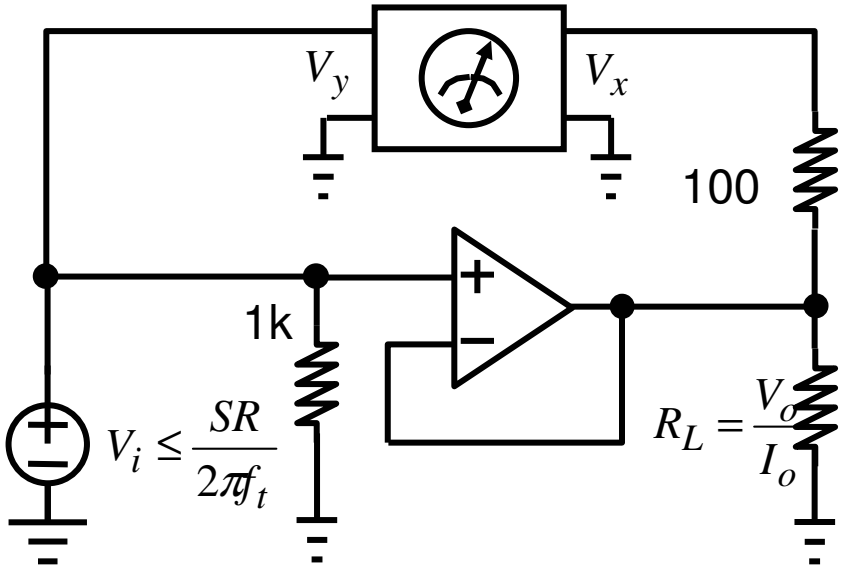
DC Test – Unit Gain Bandwidth Measurement

$$f_t = A_o \cdot f_{3dB}$$

$$V_i \le \frac{SR}{2\pi f_t}$$

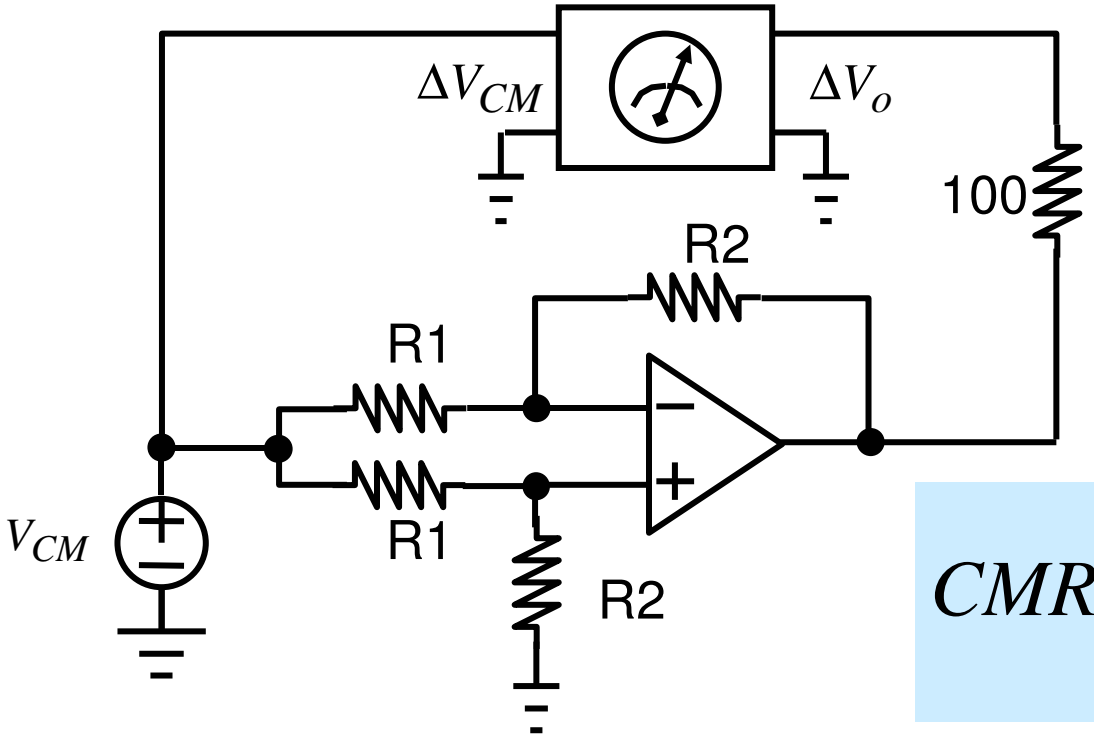


Inverting Configuration



Noninverting Configuration

DC Test – Common Mode Rejection Ratio

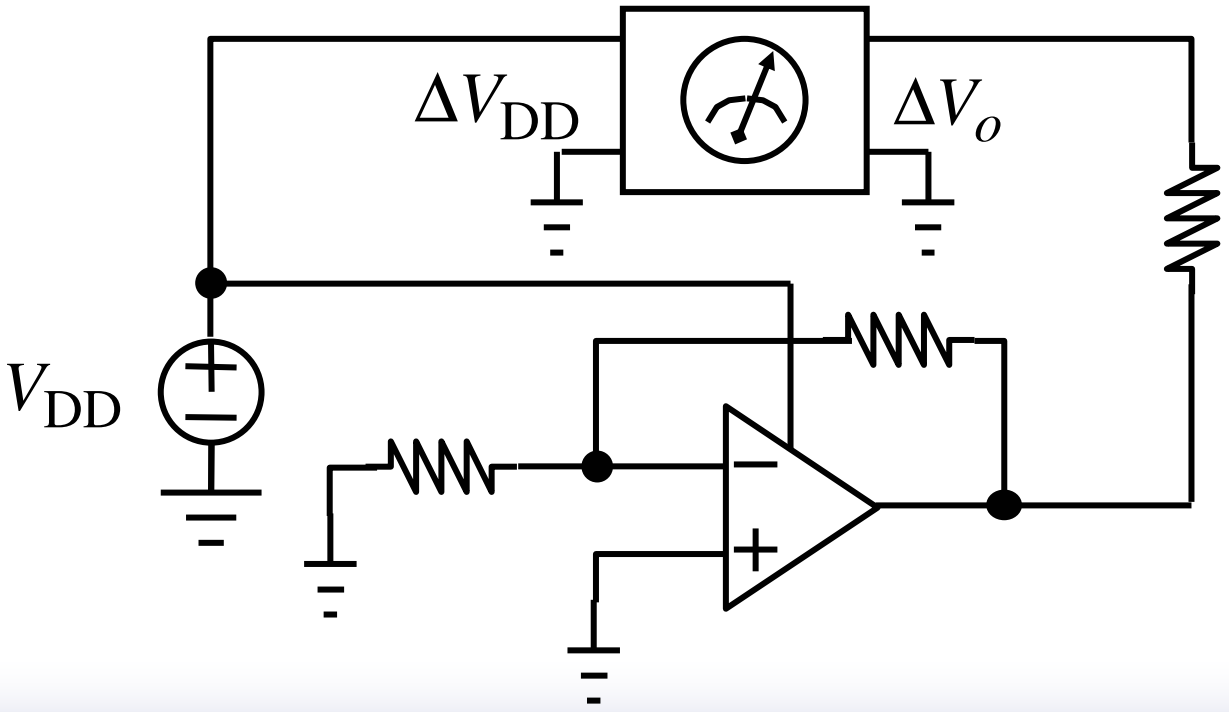


$$V_{CM \cdot i} = \frac{\Delta V_o}{A_o} = \Delta V_o / \frac{R2}{R1}$$

$$CMRR = 20\log(A_o / \frac{\Delta V_o}{\Delta V_{CM}})$$

DC Test – Power Supply Rejection Ratio

$$PSRR = 20\log(A_o / \frac{\Delta V_o}{\Delta V_{DD}})$$

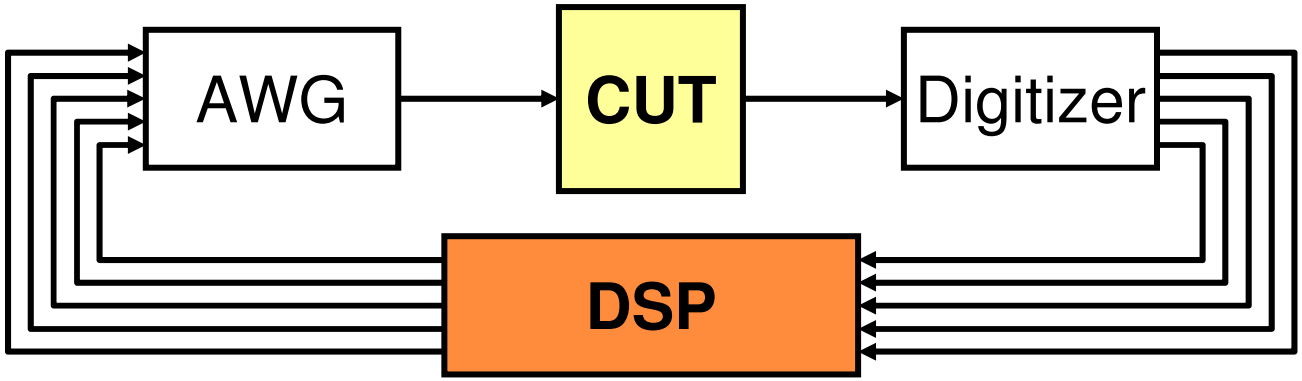


11.2 Analog Circuit Testing

- Analog Test Approaches
- Analog Test Waveforms
- DC Parametric Testing
- **AC Parametric Testing**

Analog AC Testing

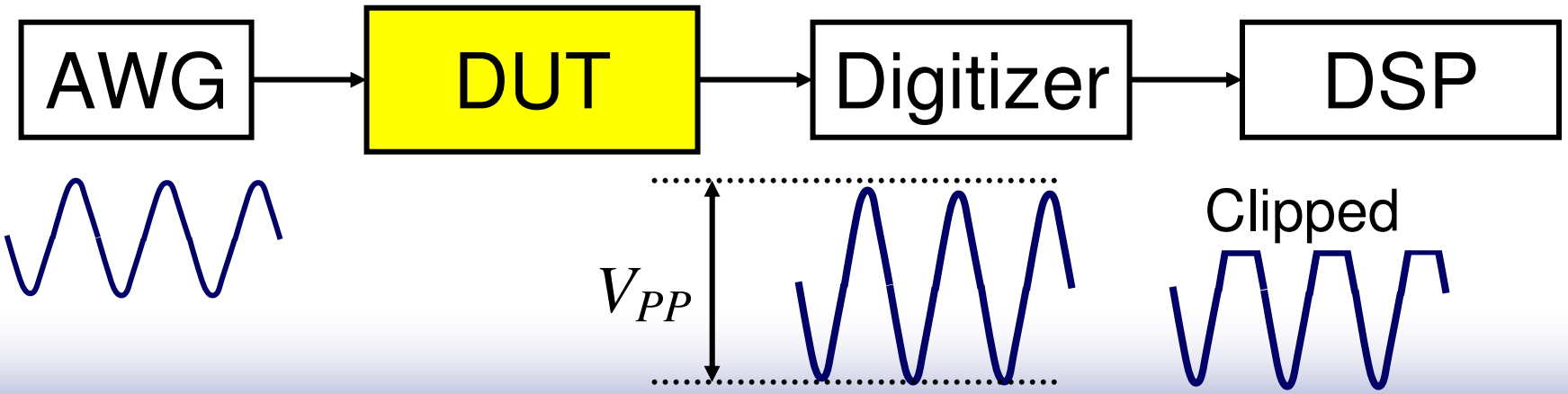
- Test Types
  - Gain
  - Phase
  - Distortion
  - Signal Rejection
  - Noise



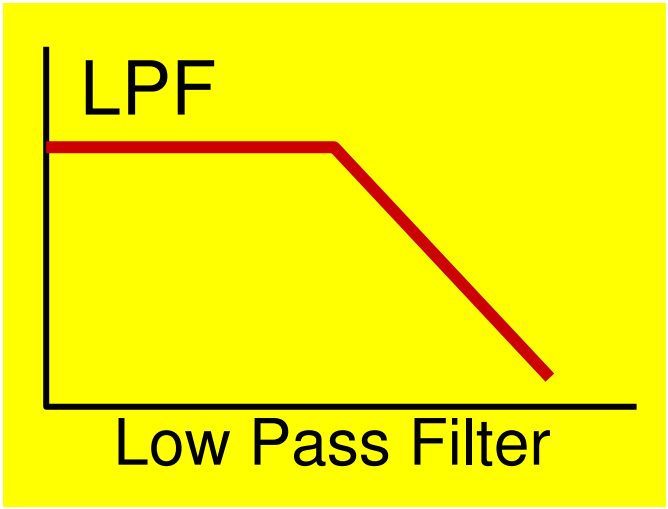
- Test Setup
  - AGW: Arbitrary Waveform Generator (DAC)
  - Digitizer: Sample and convert to digital (ADC)

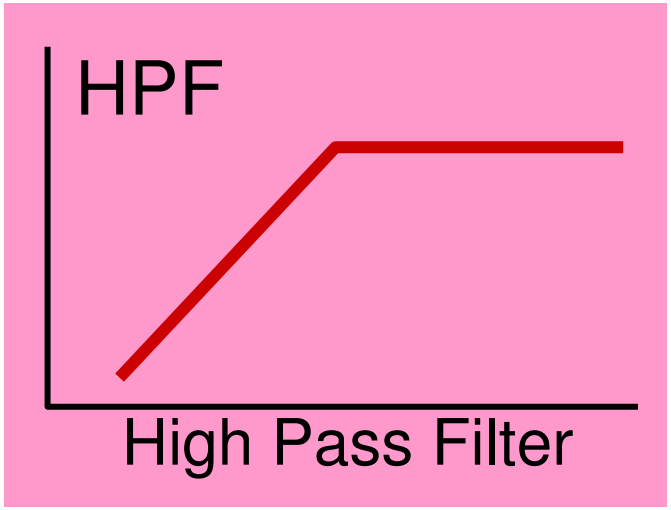
AC – Maximal Output Amplitude

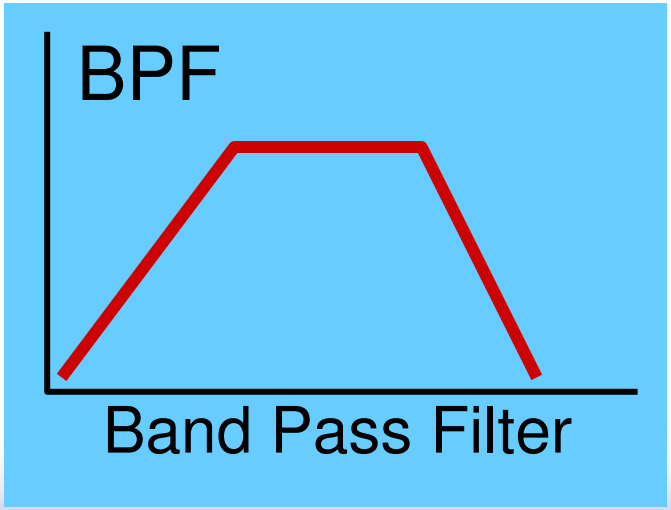
- Input sine wave (1KHz) with fixed amplitude
- Digitize the output waveform
- DSP (FFT) to eliminate distortion and noise.
- Check the fundamental amplitude.
- Detect first order defects in a circuit.
- Voltage in dBV or dBm

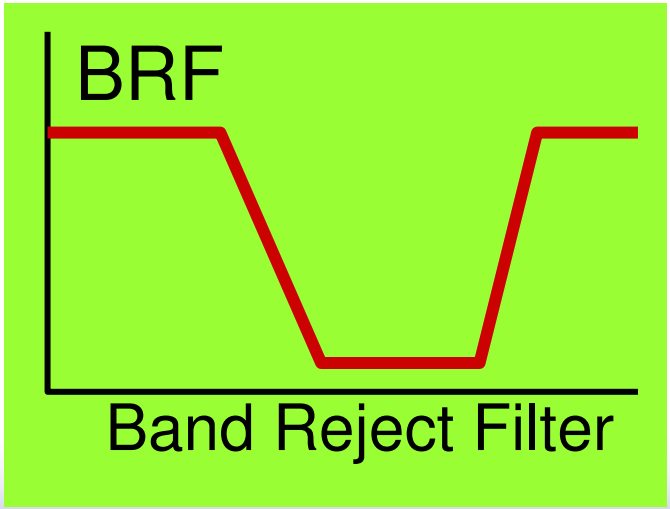


AC - Frequency Response







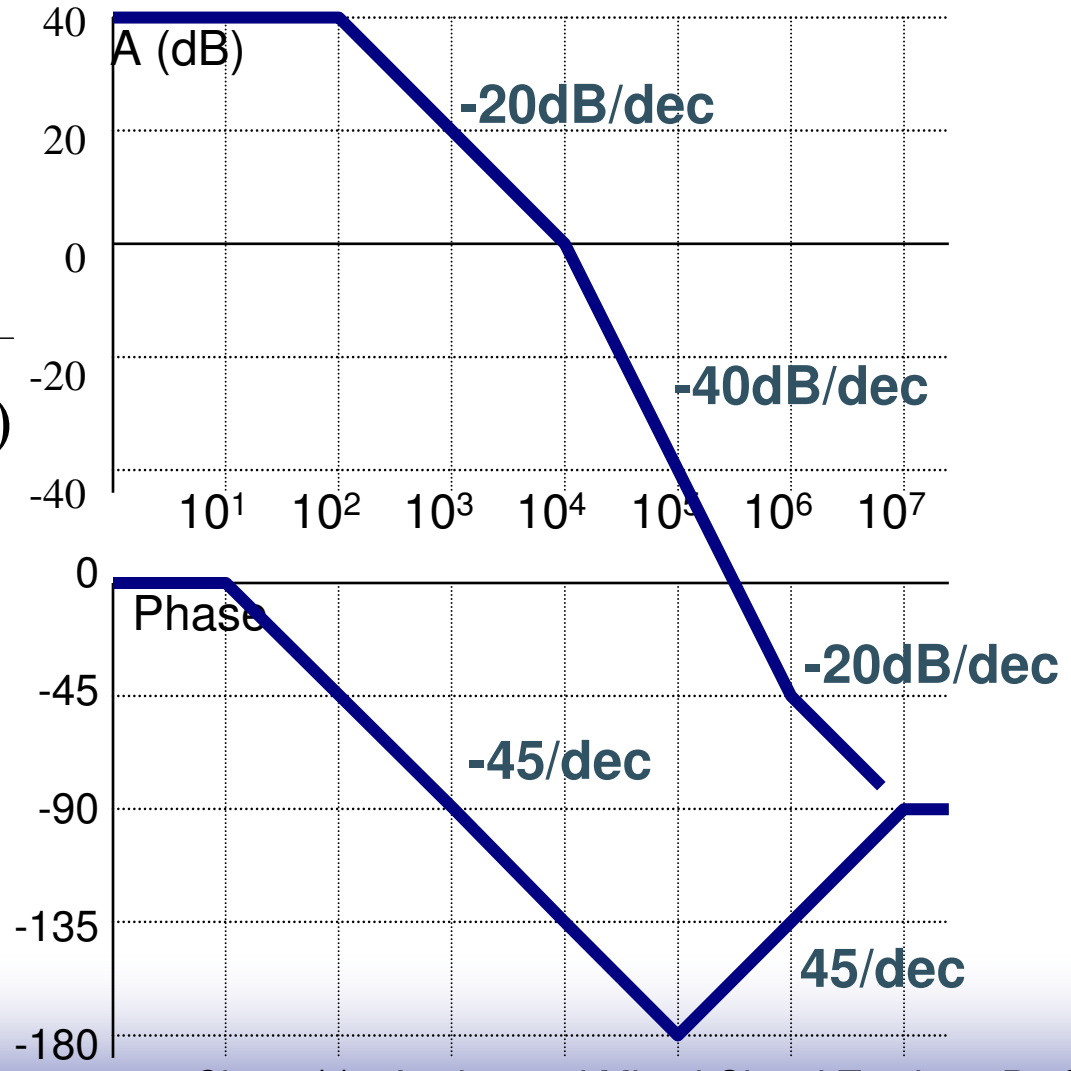


AC - Frequency Response

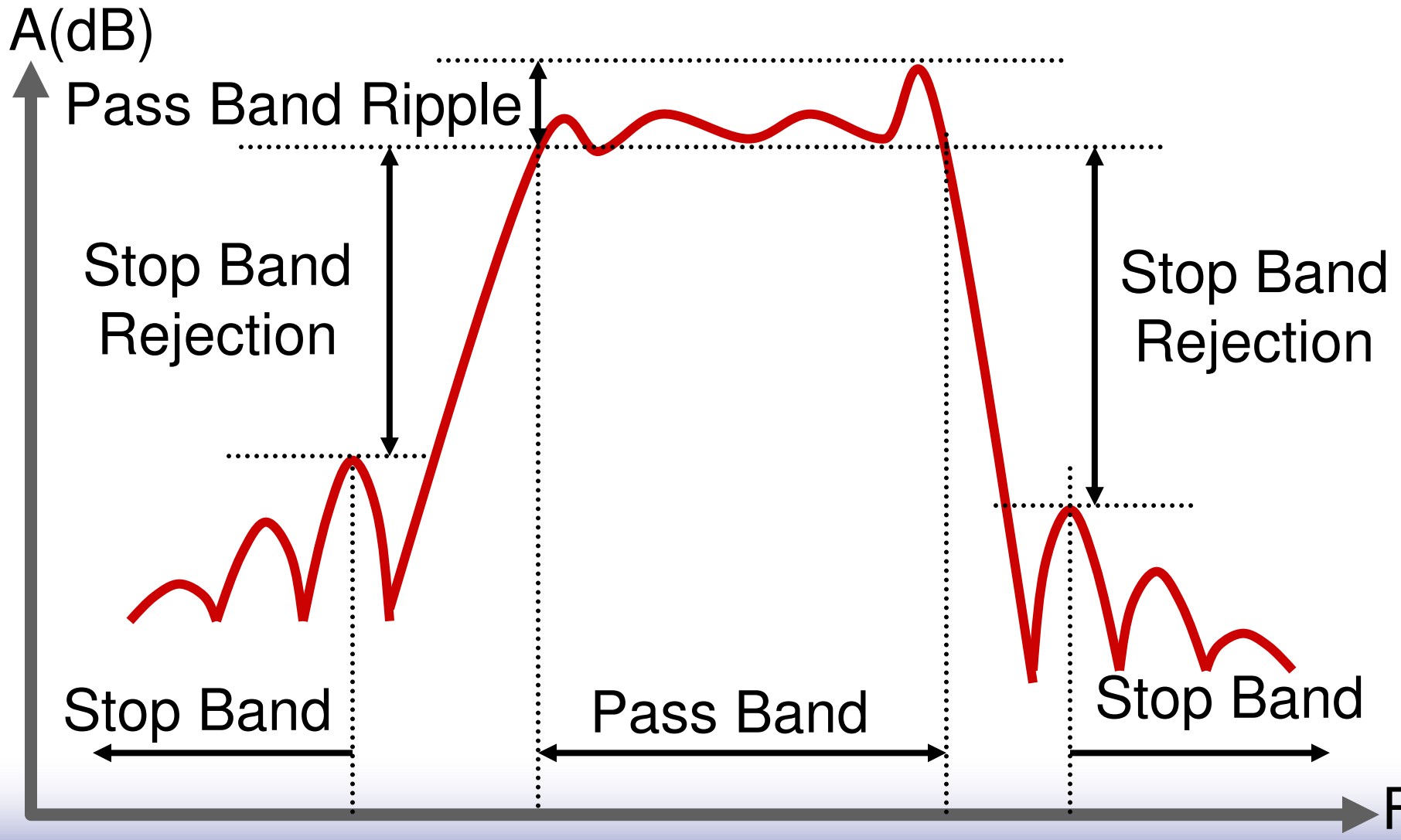
Bode Plot

$$A(jw) = \frac{10^2 (1 + \frac{jw}{10^6})}{(1 + \frac{jw}{10^2})(1 + \frac{jw}{10^4})}$$

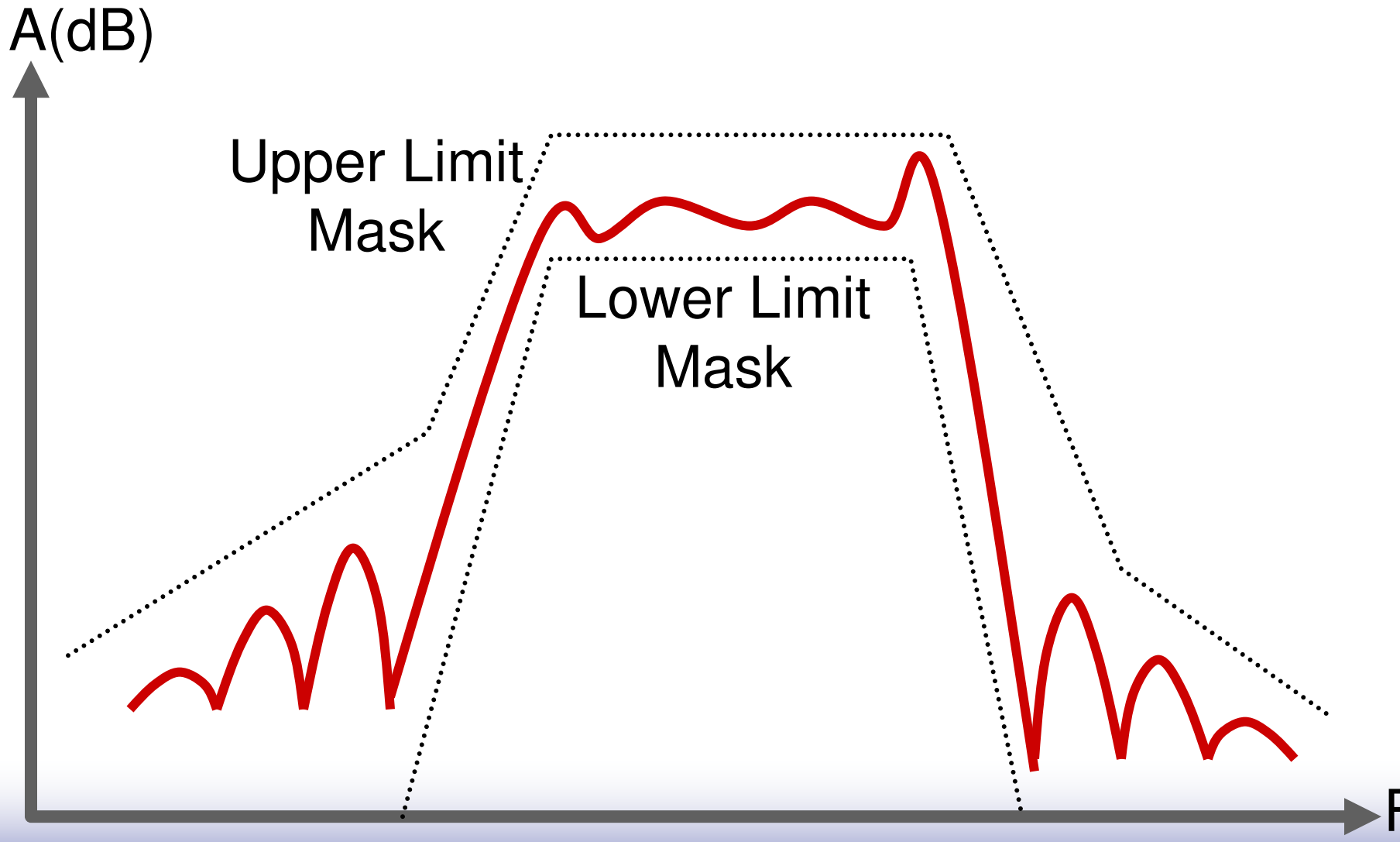
- Open Loop Gain 10^2
- Pole 1: 10^2
- Pole 2: 10^4
- Zero: 10^6



AC - Frequency Response

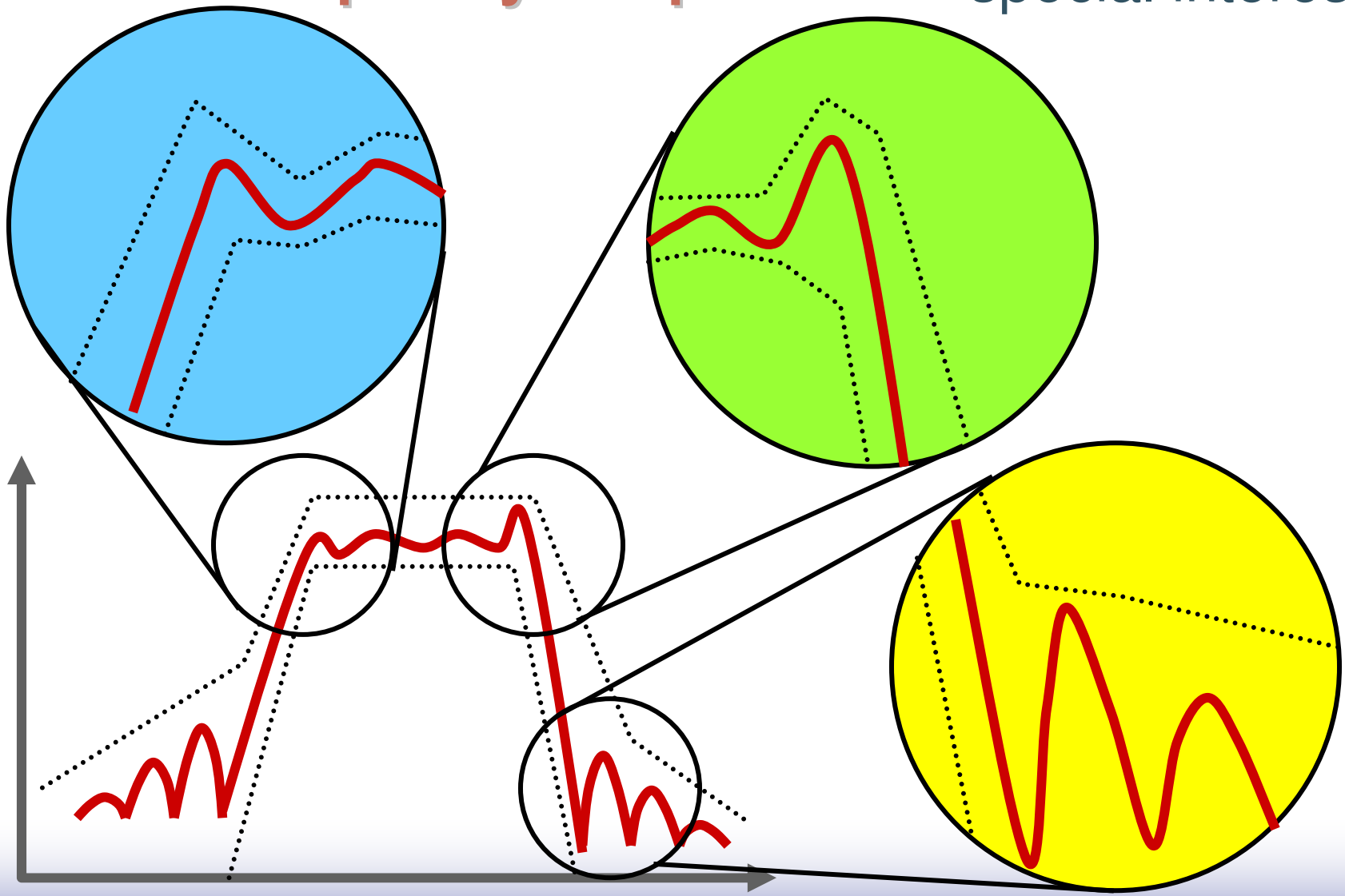


AC - Frequency Response



AC - Frequency Response

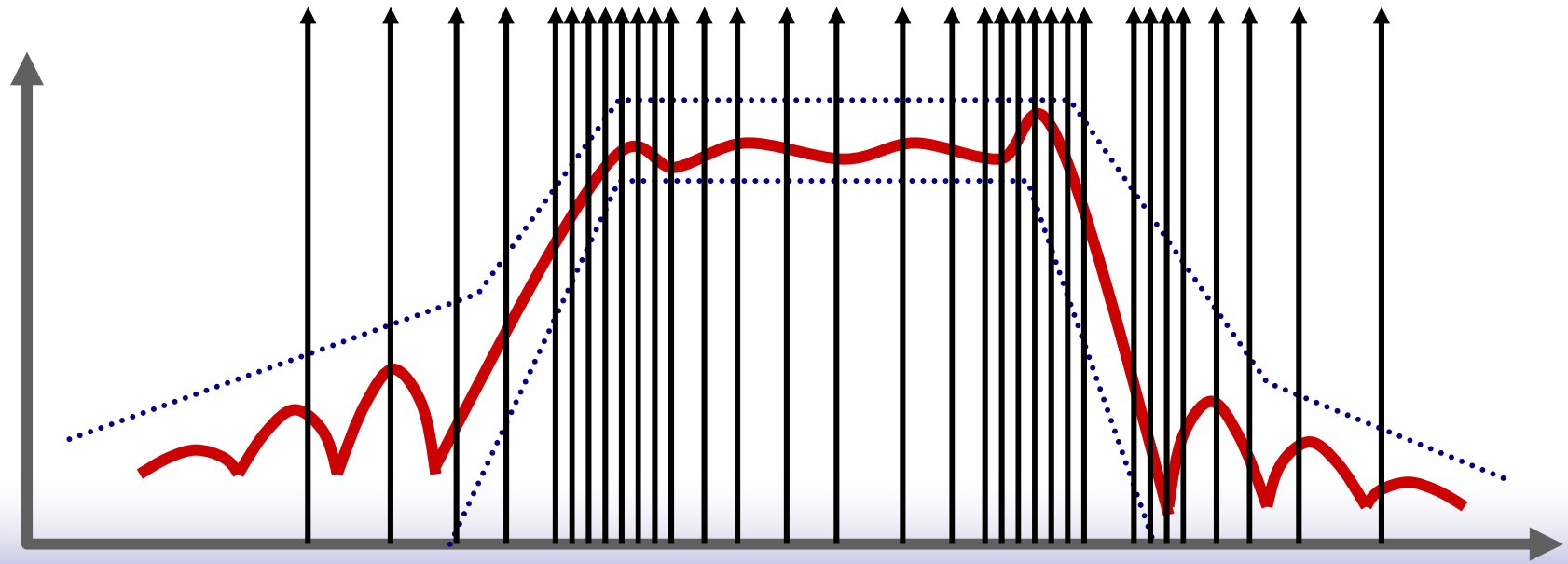
Frequencies of special interests



AC - Frequency Response

- Multi-tone Test Waveform

$$A(t) = \sum_{i=1}^{i=k} A_i \sin(\varpi_i t + \varphi_i)$$



AC - Frequency Response

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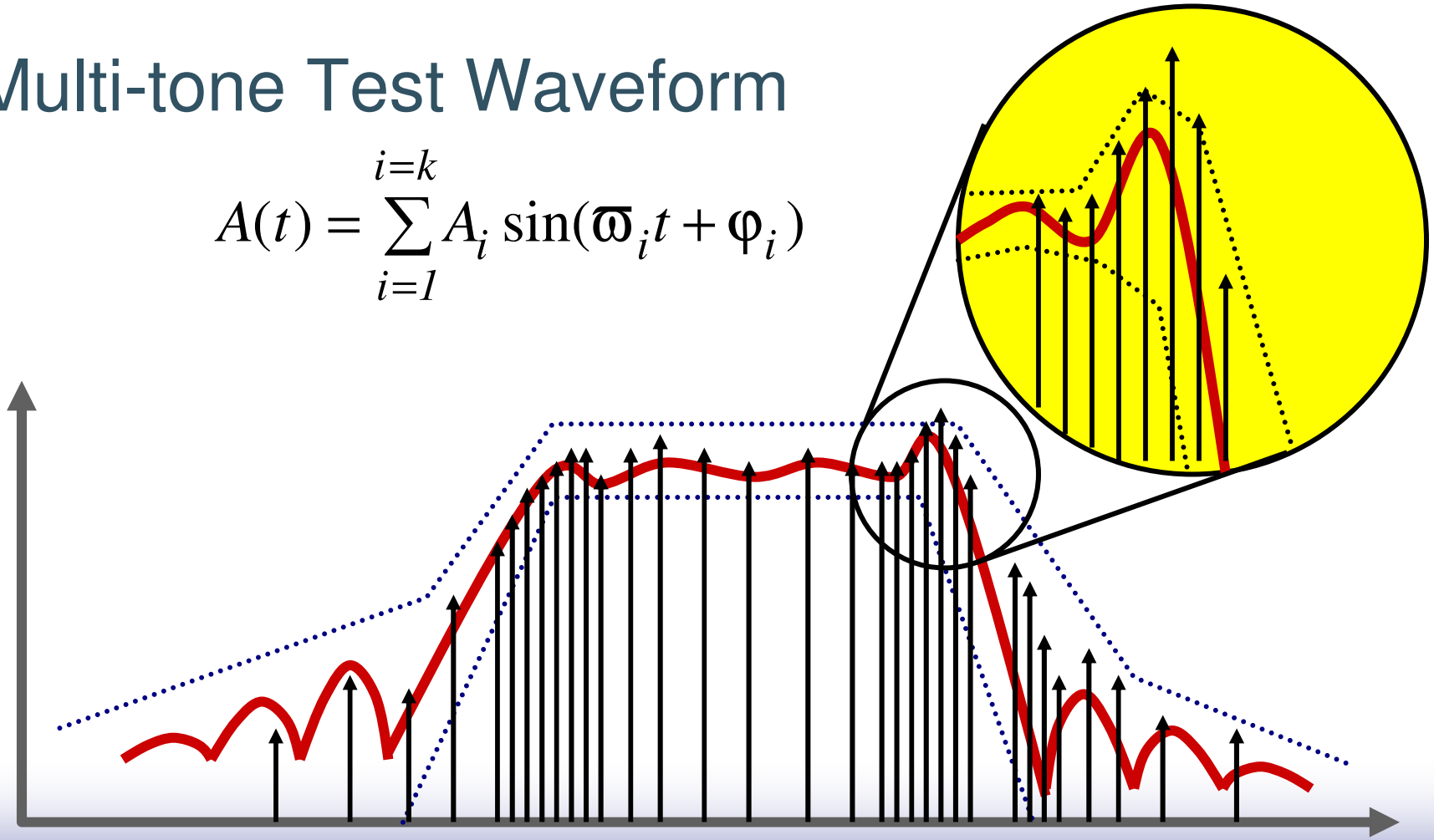
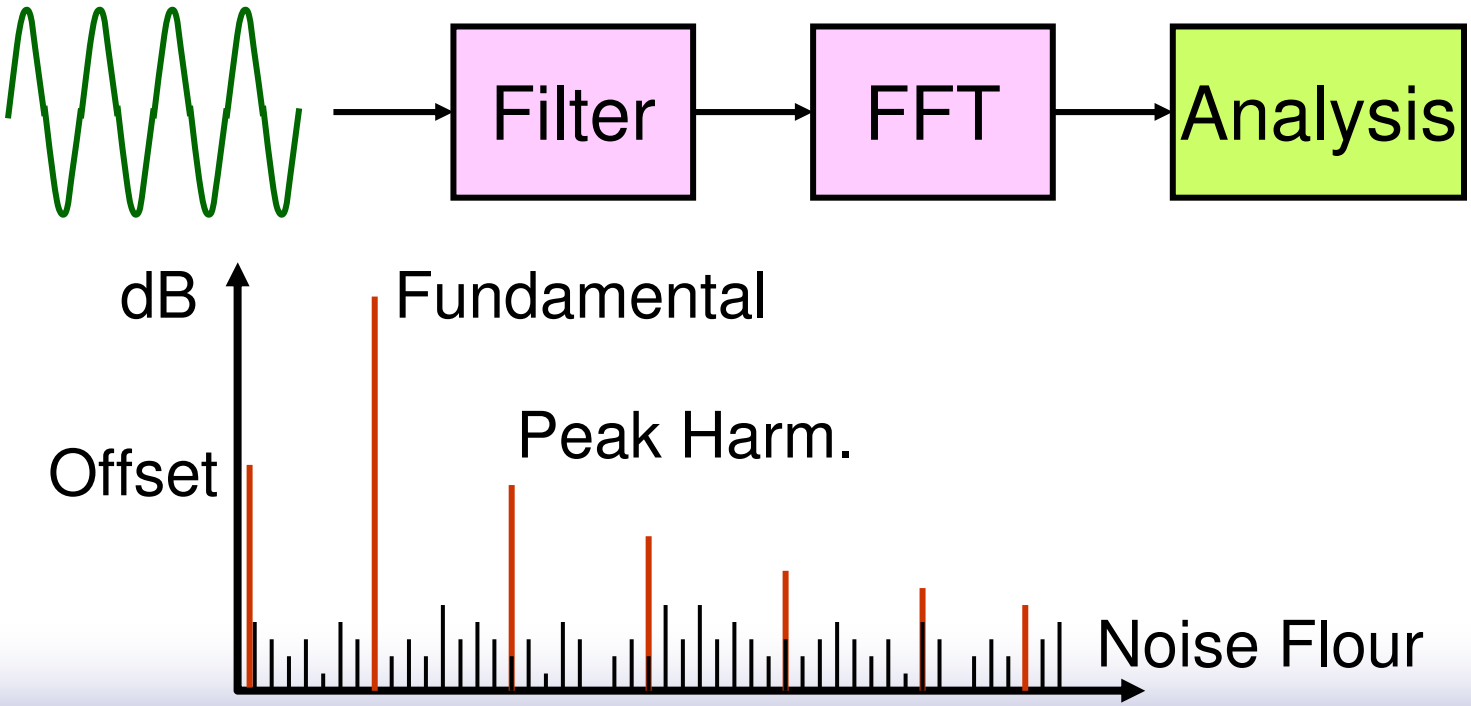


AC – Noise and Distortion

- **Distortion**
  - Harmonic Distortion
  - Intermodulation Distortion
  - Crossover
- **Cause**
  - Nonlinearity of the circuit
  - Clip (saturation)
  - Mismatch of the devices

AC – Noise and Distortion

- Apply sinusoidal waveform
- Do Fourier transform on response waveform
- Obtain F domain properties mathematically.

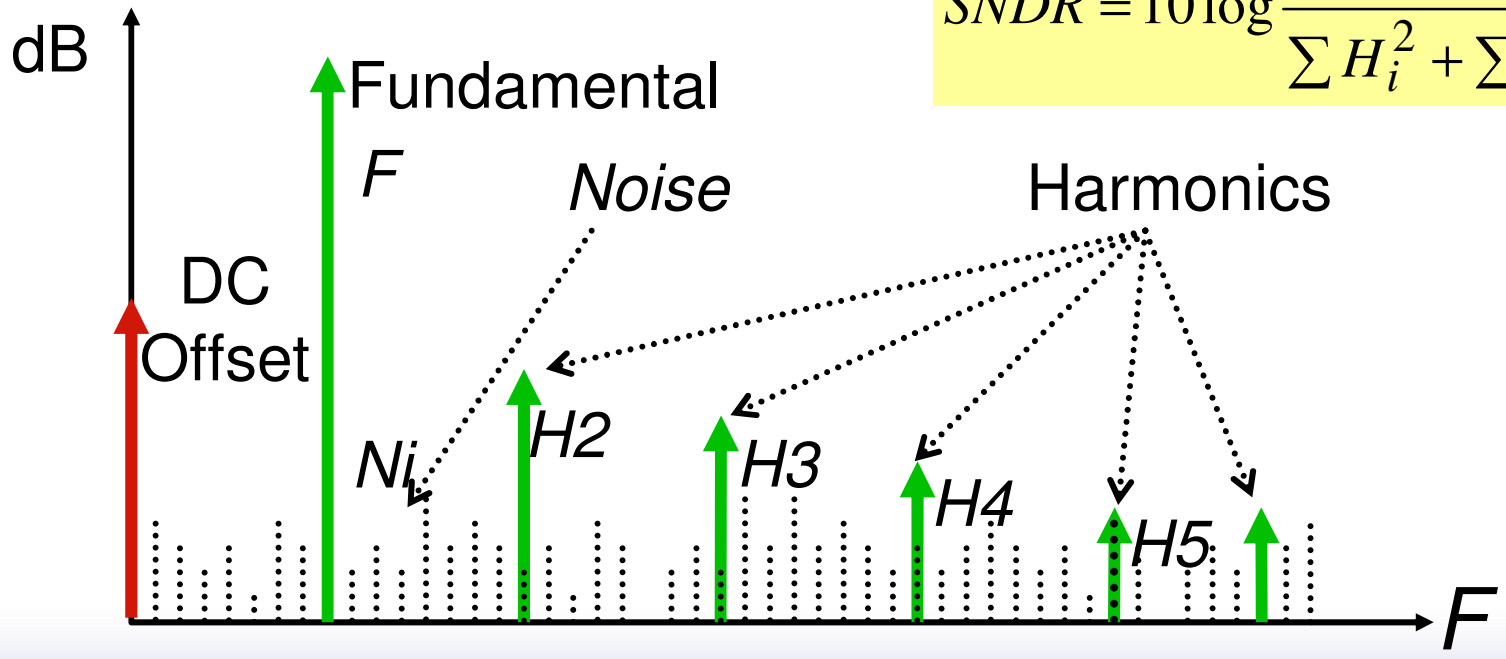


AC – Noise and Distortion

$$THD = 10\log\frac{F^2}{\sum H_i^2} = 100\times\frac{F^2}{\sum H_i^2}\%$$

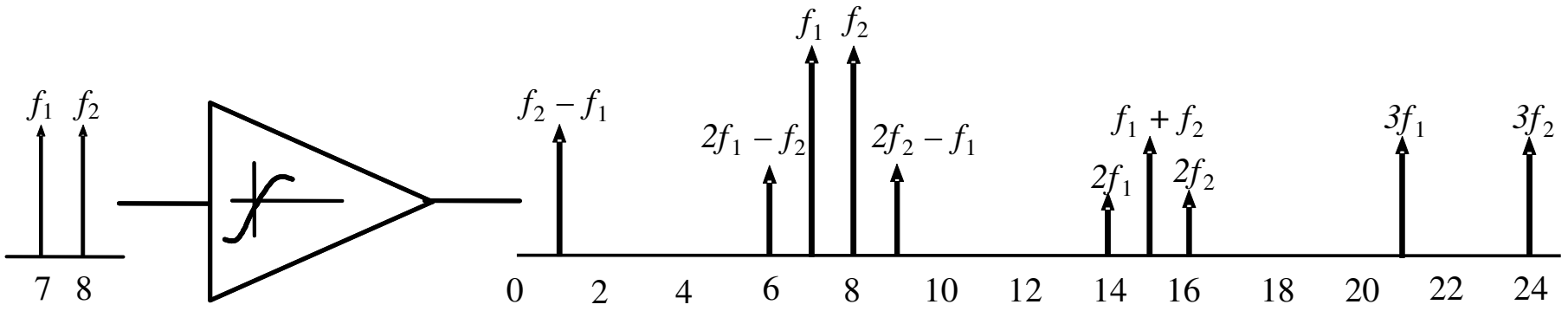
$$SNR = 10\log\frac{F^2}{\sum N_i^2}$$

$$SNDR = 10\log\frac{F^2}{\sum H_i^2 + \sum N_i^2}$$



AC – Intermodulation Distortion

$$v(t) = A_1 \sin 2\pi f_1 t + A_2 \sin 2\pi f_2 t$$



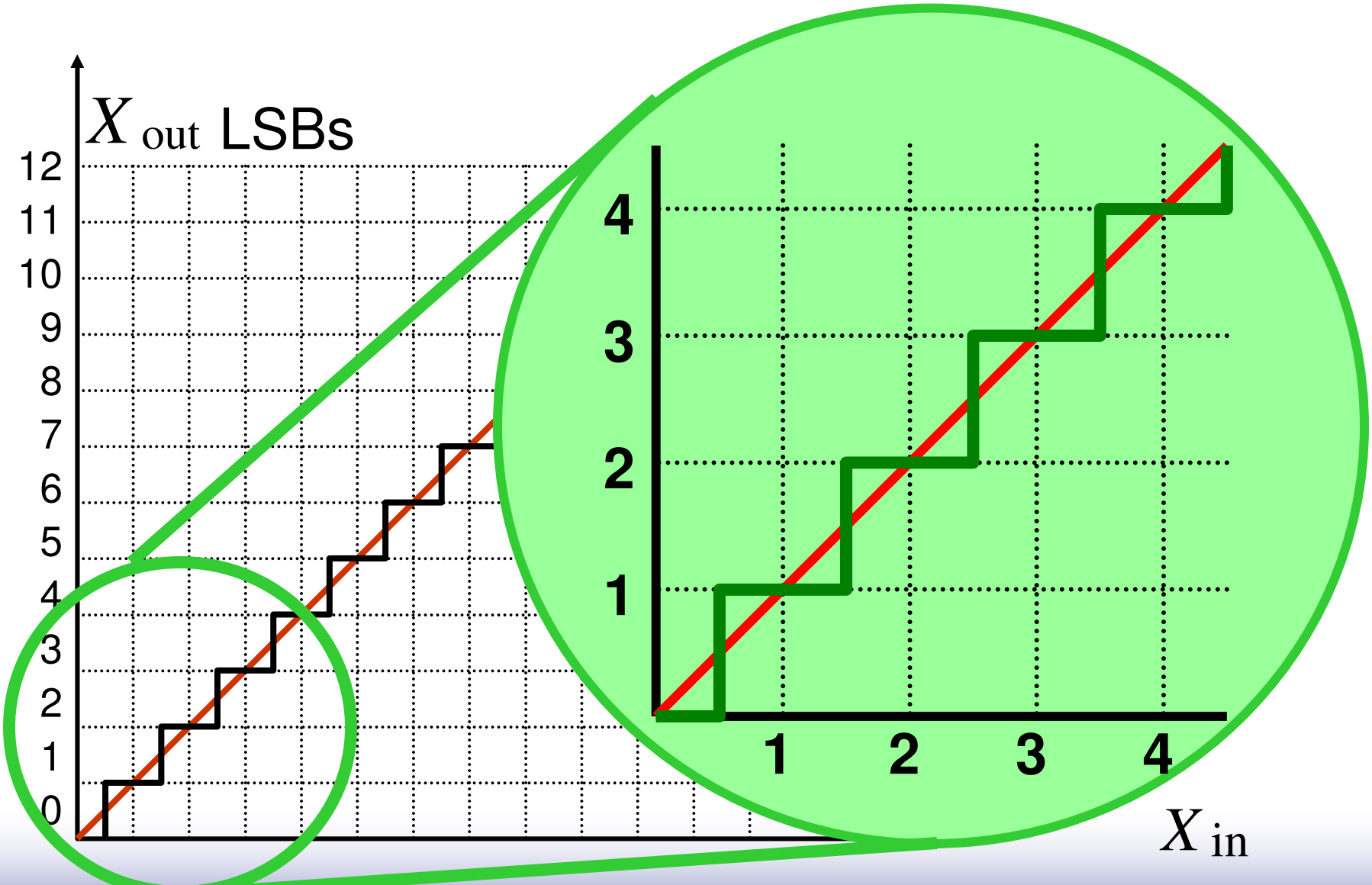
11.2 Summary

- Studied the analog test approaches
  - Specification oriented testing
  - Waveform oriented testing
- Outlined the analog test waveforms
  - Sine, step, triangular, chirp, arbitrary, modulated
- Discussed DC parametric testing
  - Open-loop gain, unit gain bandwidth
  - CMRR, PSRR
- Discussed AC parametric testing
  - Use AWG, Digitizer, and DSP
  - Frequency response, Noise, and Distortion

11.3 Mixed-Signal Testing

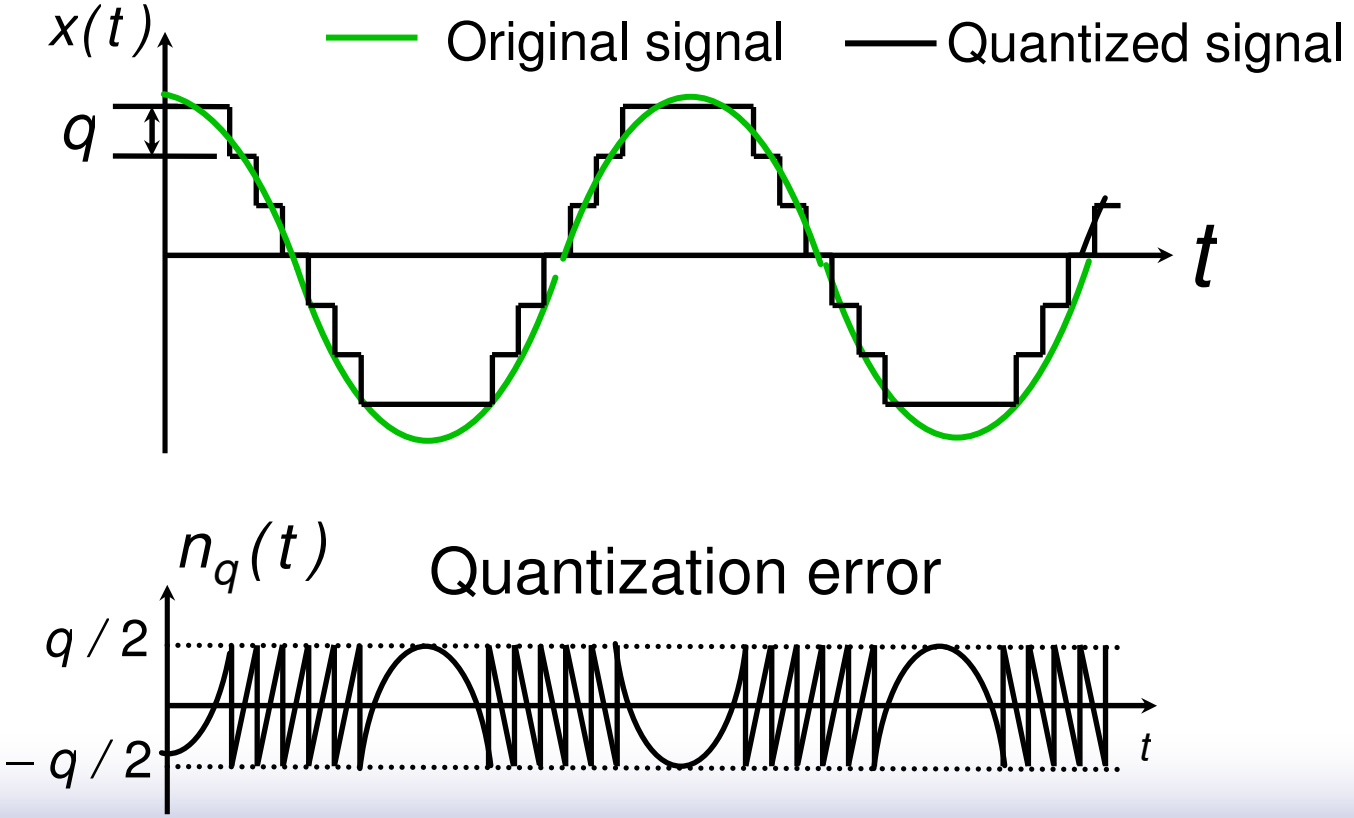
- **Introduction to Analog-Digital Conversion**
- ADC and DAC Circuit Structure
- ADC/DAC Specification and Fault Models
- IEEE Std. 1057
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing

AD Model - Quantization



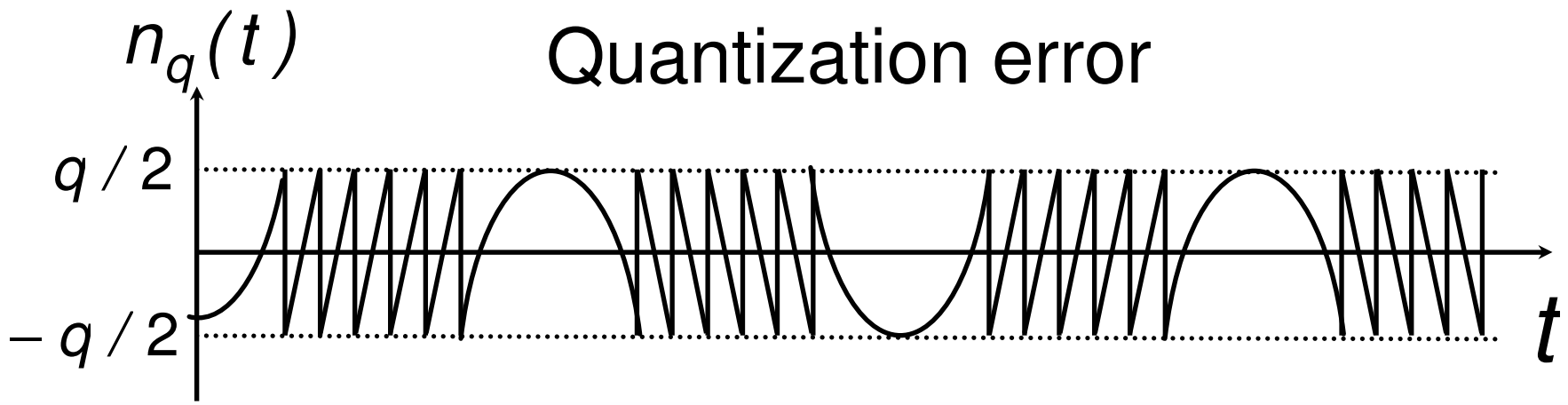
Quantizatoin – Noise Model

- Quantization error is sawtooth-like.
- Uniform distribute between *(-q/2, q/2) (q=LSB).*



Quantizatoin – Noise Model

- The error contains a lot of jumps.
- Error spectral is much wider than the original signal.
- The bandwidth of the quantization is proportional to the slop of the signal and inversely proportional to the quantum size q.



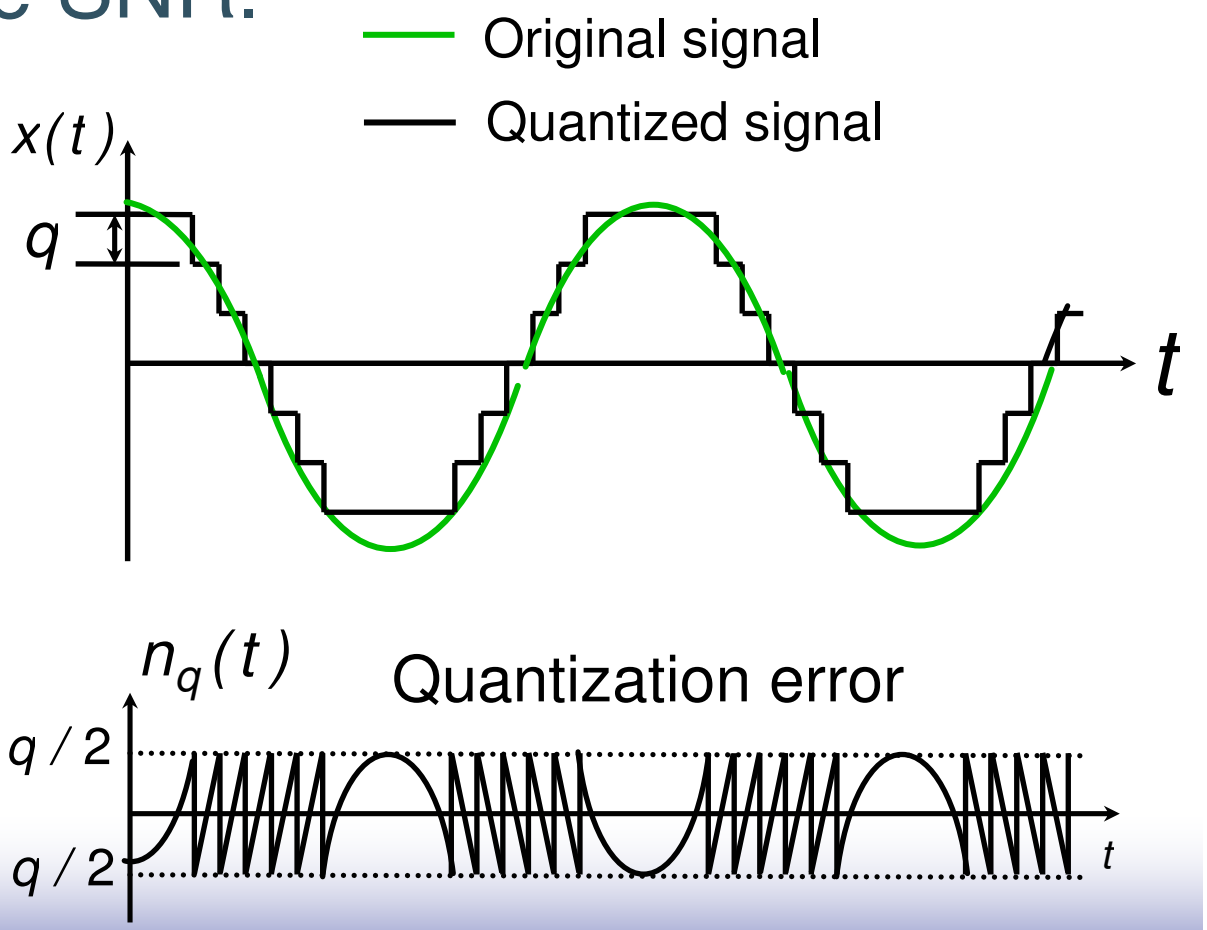
Quantization - Noise Model

- A sine wave is quantized by a B-bit ADC. How large is the SNR.

$$2V_p = 2^n q$$

$$P_S = \frac{V_p^2}{2}$$

$$P_N = \left(\frac{q/2}{\sqrt{3}}\right)^2 = \frac{q^2}{12}$$



Quantization - Noise Model

$$SNR = 10\log\frac{P_s}{P_N} = 10\log\left(\frac{\frac{V_p^2}{2}}{\frac{q^2}{12}}\right) = 10\log(6\cdot 4^{n-1})$$

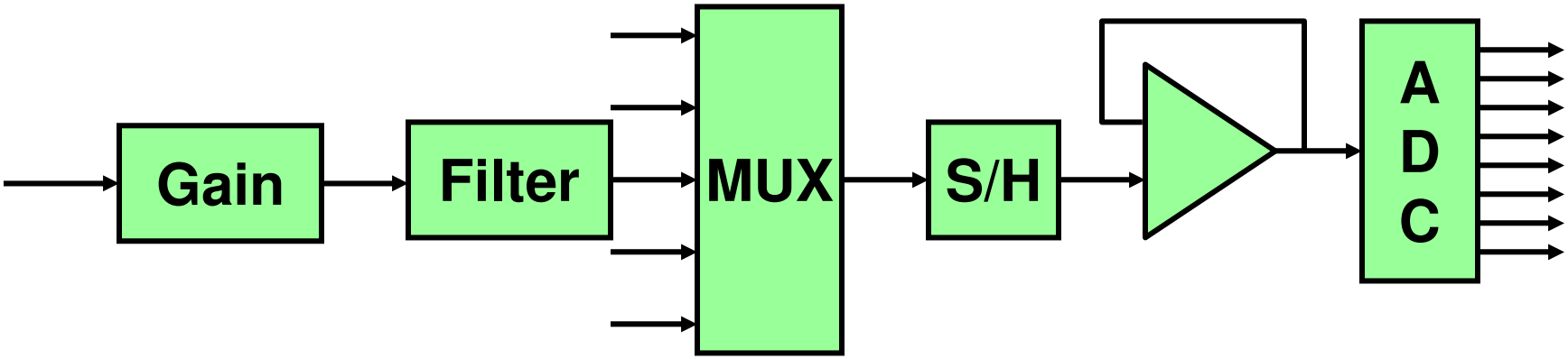
$$SNR == (1.76 + 6n)dB$$

For n=10, $SNR = 61.8dB$

11.3 Mixed-Signal Testing

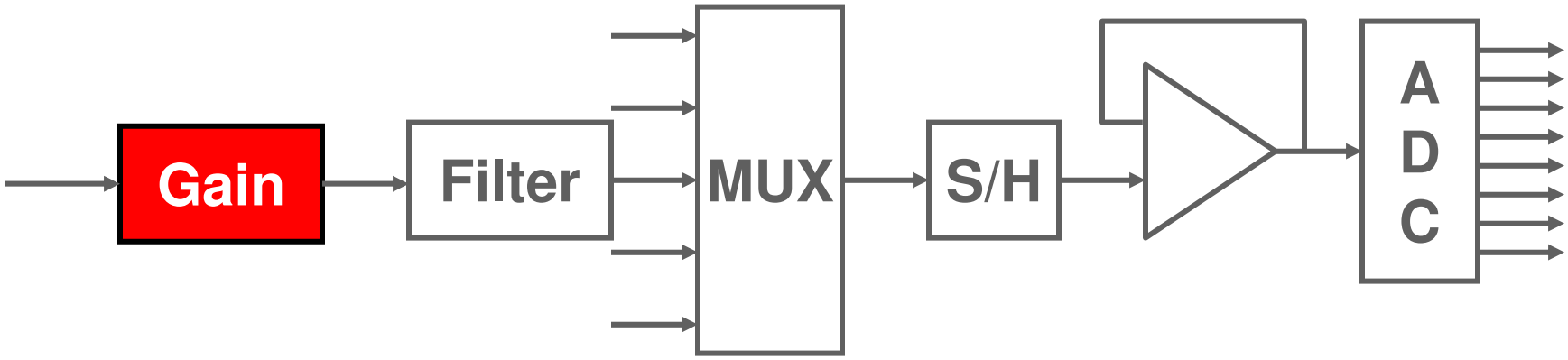
- Introduction to Analog-Digital Conversion
- **ADC and DAC Circuit Structure**
- ADC/DAC Specification and Fault Models
- IEEE Std. 1057
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing

ADC Architecture - Gain Stage



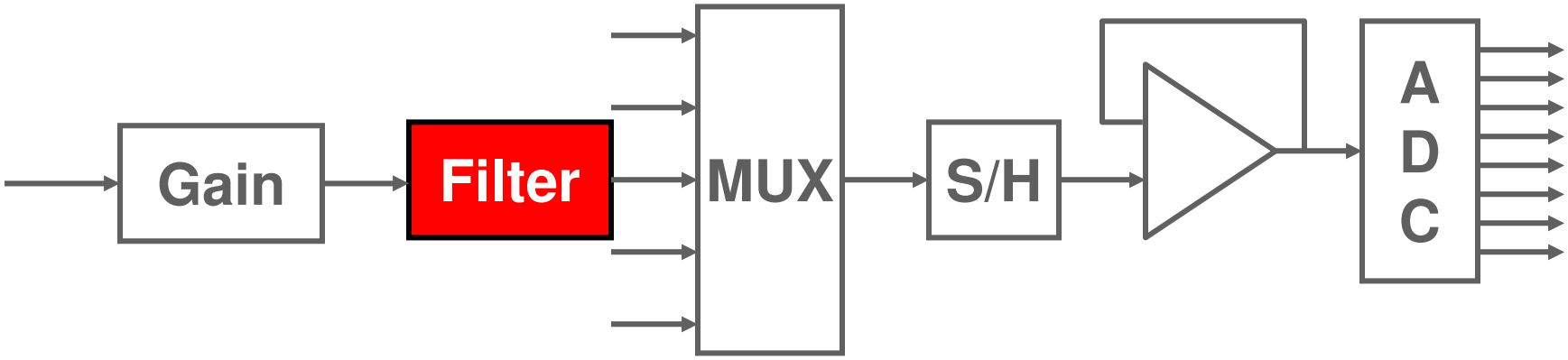
- **Gain:** Provide offset and full scale conversion
- **Filter:** Reject off-band noise (anti-aliasing filter)
- **MUX:** Provide multiple channel access
- **S/H:** Provide steady signal for A-to-D conversion
- **ADC:** Actual analog to digital conversion

ADC Architecture - Gain Stage



- Function: Provides gain and offset
- Achieve the maximal A/D resolution by scaling the input signal to match the full A/D input range.
- Drawbacks:
  - Introduces noise, nonlinearity, drift
  - Expense of tight-tolerance
  - Require calibration

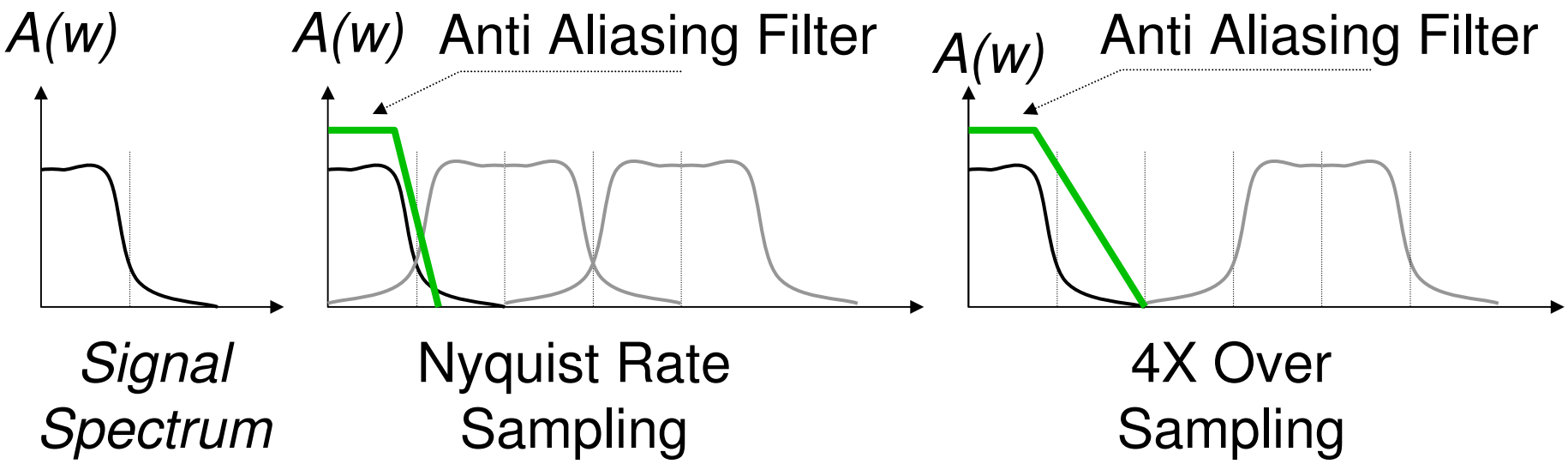
ADC Architecture - Filter Stage



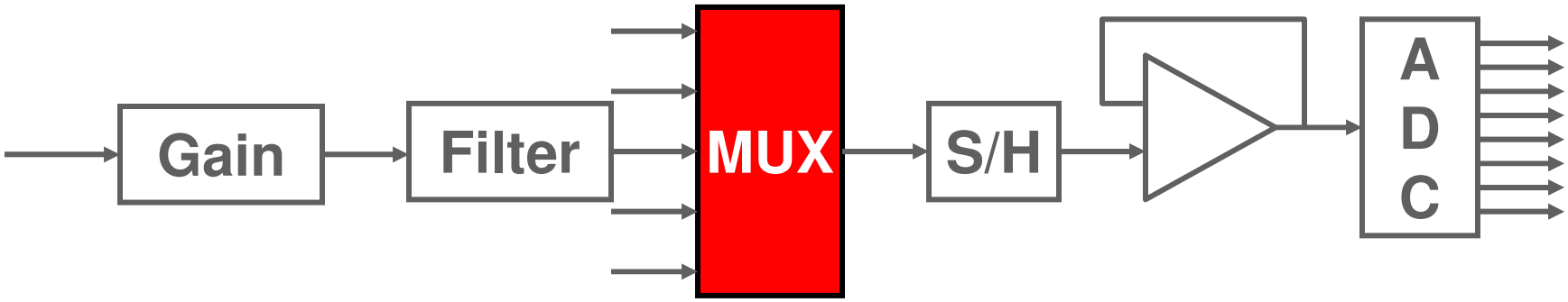
- Function: Attenuate the out-of-band noise to prevent aliasing
- Filter Position
  - Before the MUX (1 per channel) : maximize speed in switching channels.
  - After the MUX: minimize mismatching among channels.

ADC Architecture - Filter Stage

- Anti-Aliasing Filter

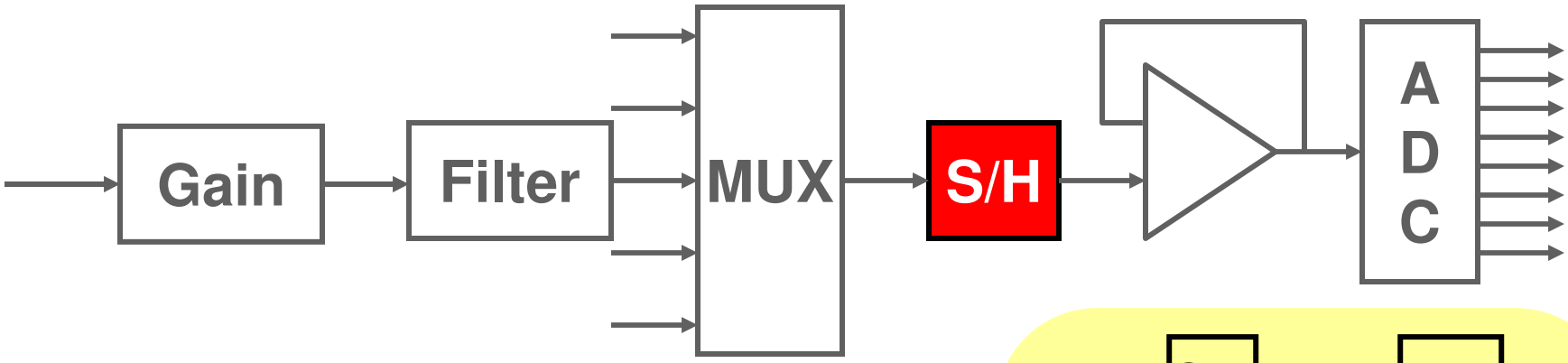


ADC Architecture - MUX Stage

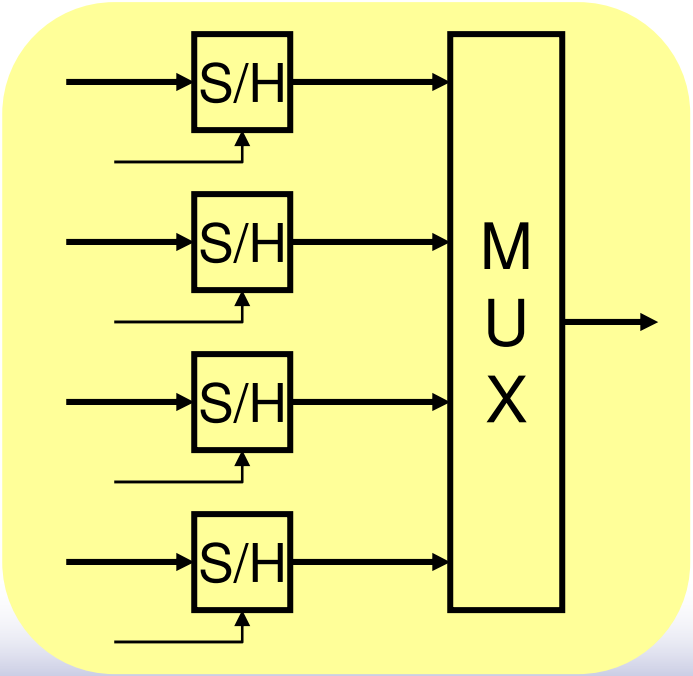


- Function: Provides multiple access
- Crosstalk:
  - The most severe problem
  - Frequency dependent
  - Can be minimized by placing amplifier before the MUX.
- Load Issues
  - Avoid too many fanins.
  - Use hierarchical structure.

ADC Architecture - S/H Stage

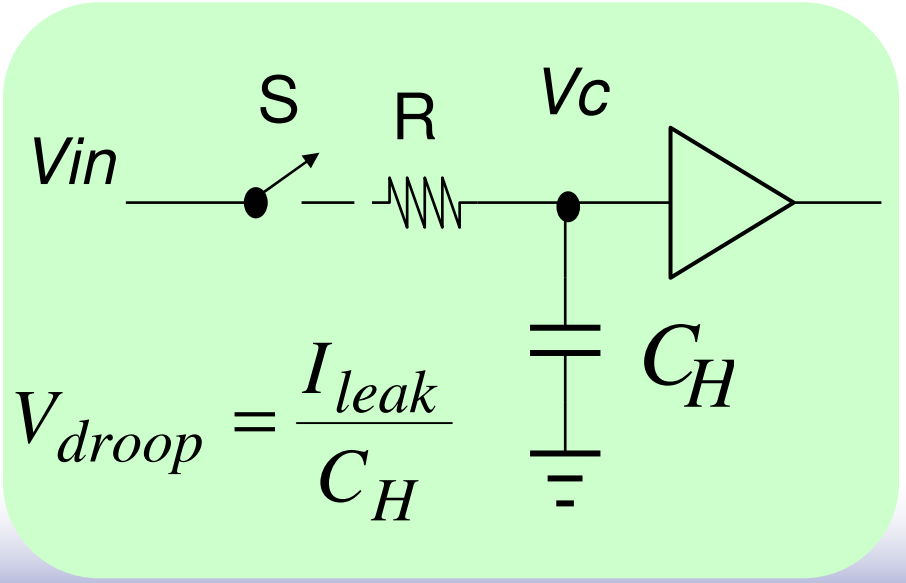


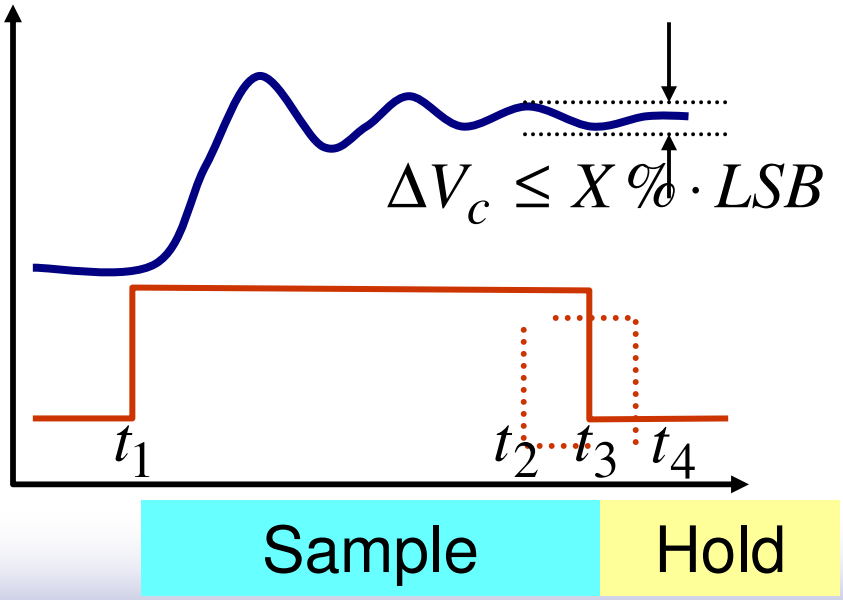
- Function:
  - Provides steady signal
  - Provides signal synchronization,
- S/H position:
  - After the MUX for cost reason
  - Before MUX for synchronization and crosstalk reduction.



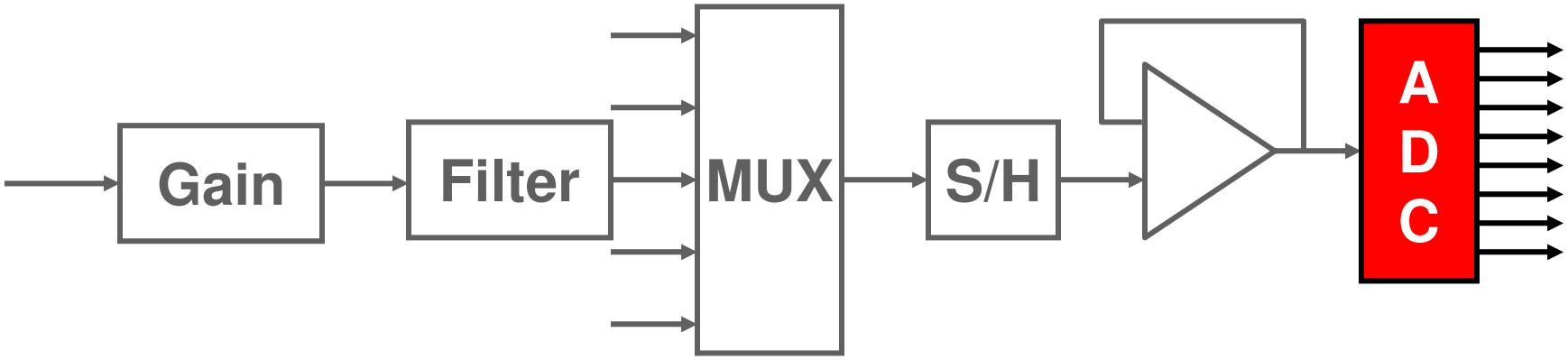
ADC Architecture - S/H Check List

- **Aperture Time**: The time aperture ***(t3)***
- **Acquisition Time**: The total time for the S/H to acquire a full-scale step input signal. ***(t3 - t1)***
- **Aperture Jitter:** The uncertainty of aperture time due to noise or jitter in clock. ***(t4-t2)***



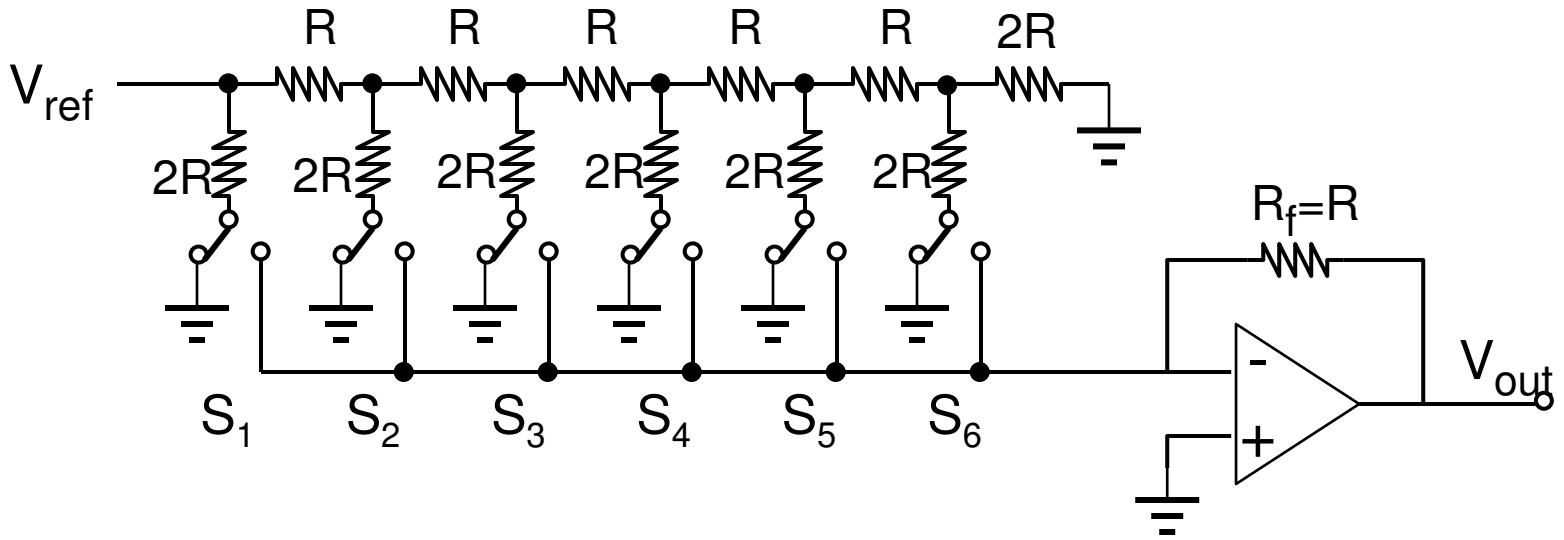


ADC Architecture - ADC Stage



- Executes analog to digital conversion
- Check List:
  - Bit length
  - Accuracy
  - Conversion Rate
  - System Error Budget
  - Input Signal Range
  - Total System Cost Target
  - Input Impedance
  - AC or DC Inputs BW

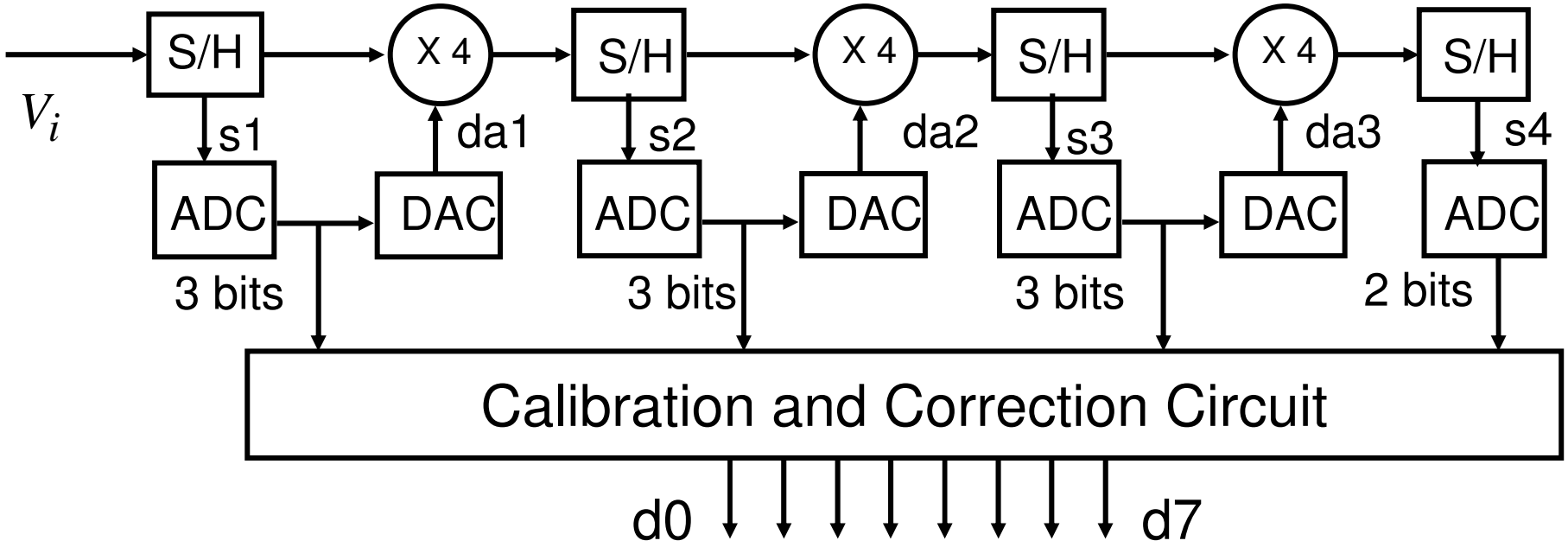
DAC Example - R-2R Ladder



$$V_o = S_5 \cdot \frac{V_{ref}}{2^1} + S_4 \cdot \frac{V_{ref}}{2^2} + S_3 \cdot \frac{V_{ref}}{2^3} + S_2 \cdot \frac{V_{ref}}{2^4} + S_1 \cdot \frac{V_{ref}}{2^5} + S_0 \cdot \frac{V_{ref}}{2^6}$$

$$= (S_5 \cdot 2^5 + S_4 \cdot 2^4 + S_3 \cdot 2^3 + S_2 \cdot 2^2 + S_1 \cdot 2^1 + S_0 \cdot 2^0) \cdot \frac{V_{ref}}{2^6}$$

ADC Example – Pipelined ADC



ADC – Bits v.s. Throughput

ADC	Bit-Length	Throughput
Flash	~ 6 bits	100 M ~
Pipelined	8 ~ 16 bits	10 ~ 100 MHz
Sigma-Delta	14 ~ bits	~ 10 M

ADC – Selection Matrix

Bits	<10kbps	10Kbps to 100Kbps	100Kbps to 1Mbps	1Mbps to 10Mbps	10 to 100Mbps	100Mbps +
17+	●	●	●	●		
14-16	●	●	●	●		
12-13		●	●	●	●	●
10-11		●	●	●	●	●
8-9			●	●	●	●
<8					●	

From Analog Devices Inc.

ADC – Example AD775

AD775–SPECIFICATIONS

(T_A = +25°C with AV_{DD}, DV_{DD} = +5 V, AV_{SS}, DV_{SS} = 0 V, V_{RT} = 2.6 V, V_{RB} = +0.6 V, CLOCK = 20 MHz unless otherwise noted)

Parameter	AD775J Min	AD775J Typ	AD775J Max	Units
RESOLUTION	8			Bits
DC ACCURACY				
Integral Nonlinearity (INL)		+0.5	1.3	LSB
Differential Nonlinearity (DNL)		±0.3	±0.5	LSB
No Missing Codes		GUARANTEED		
Offset				
To Top of Ladder V_{RT}	–10	–35	–60	mV
To Bottom of Ladder V_{RB}	0	+15	+45	mV
VIDEO ACCURACY[1]				
Differential Gain Error		1.0		%
Differential Phase Error		0.5		Degrees
ANALOG INPUT				
Input Range (V_{RT}–V_{RB})		2.0		V p-p
Input Capacitance		11		pF
AC SPECIFICATIONS[2]				
Signal-to-Noise and Distortion (S/(N + D))				
f_{IN} = 1 MHz		47		dB
f_{IN} = 5 MHz		41		dB
Total Harmonic Distortion (THD)				
f_{IN} = 1 MHz		–51		dB
f_{IN} = 5 MHz		–42		dB
REFERENCE INPUT				
Reference Input Resistance (R_{REF})	230	300	450	Ω
Case 1: V_{RT} = V_{RTS}, V_{RB} = V_{RBS}				
Reference Bottom Voltage (V_{RB})	0.60	0.64	0.68	V
Reference Span (V_{RT}–V_{RB})	1.96	2.09	2.21	V
Reference Ladder Current (I_{REF})	4.4	7.0	9.6	mA
Case 2: V_{RT} = V_{RTS}, V_{RB} = AV_{SS}				
Reference Span (V_{RT}–V_{RB})	2.25	2.39	2.53	V
Reference Ladder Current (I_{REF})	5	8	11	mA
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.75		+5.25	Volts
DV_{DD}	+4.75		+5.25	Volts
Operating Current				
IAV_{DD}		9.5		mA
IDV_{DD}		2.5		mA
IAV_{DD} + IDV_{DD}		12	17	mA
POWER CONSUMPTION		60	85	mW
TEMPERATURE RANGE				
Operating	–20		+75	°C

NOTES
[1]NSTC 40 IRE modulation ramp, CLOCK – 14.3 MSPS.
[2]f_{IN} amplitude – 0.3 dB full scale.

Specifications subject to change without notice. See Definition of Specifications for additional information.

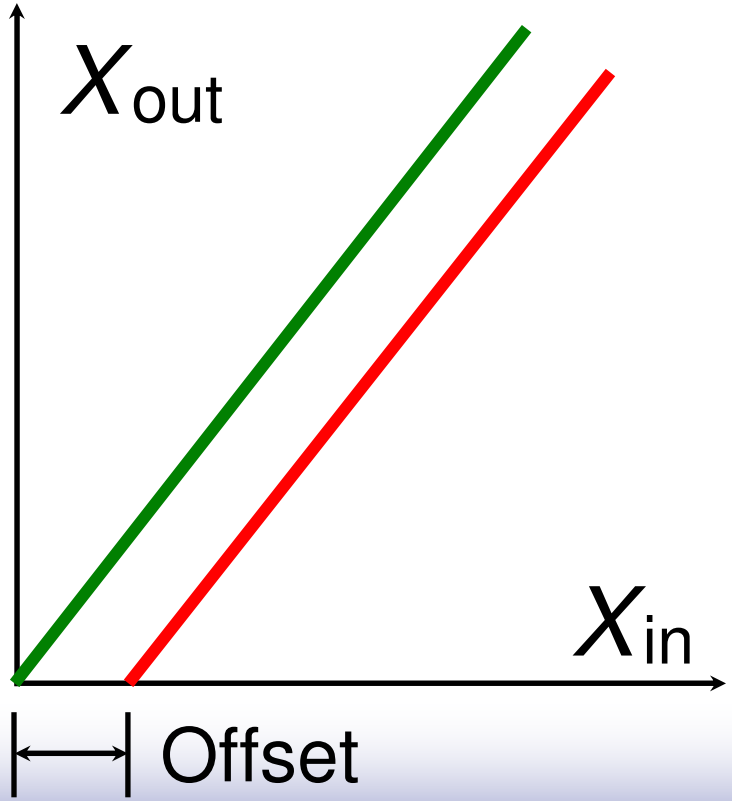
From Analog Devices inc.

11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
- ADC and DAC Circuit Structure
- **ADC/DAC Specification and Fault Models**
- IEEE Std. 1057
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing

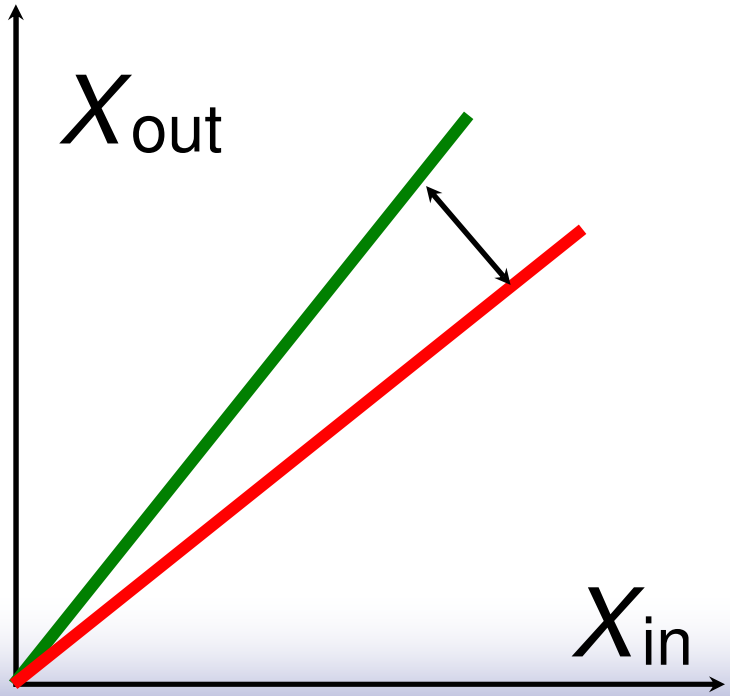
ADC – Offset Error

- **Offset:** constant component of the error that is independent of the inputs



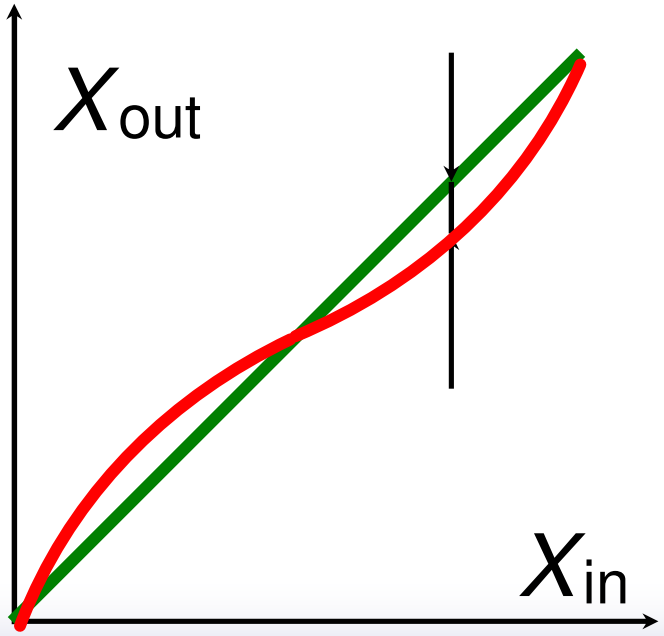
ADC – Gain Error

- **Gain Error**: difference between the actual transfer ratio and the ideal ratio
- Also called Calibration Error



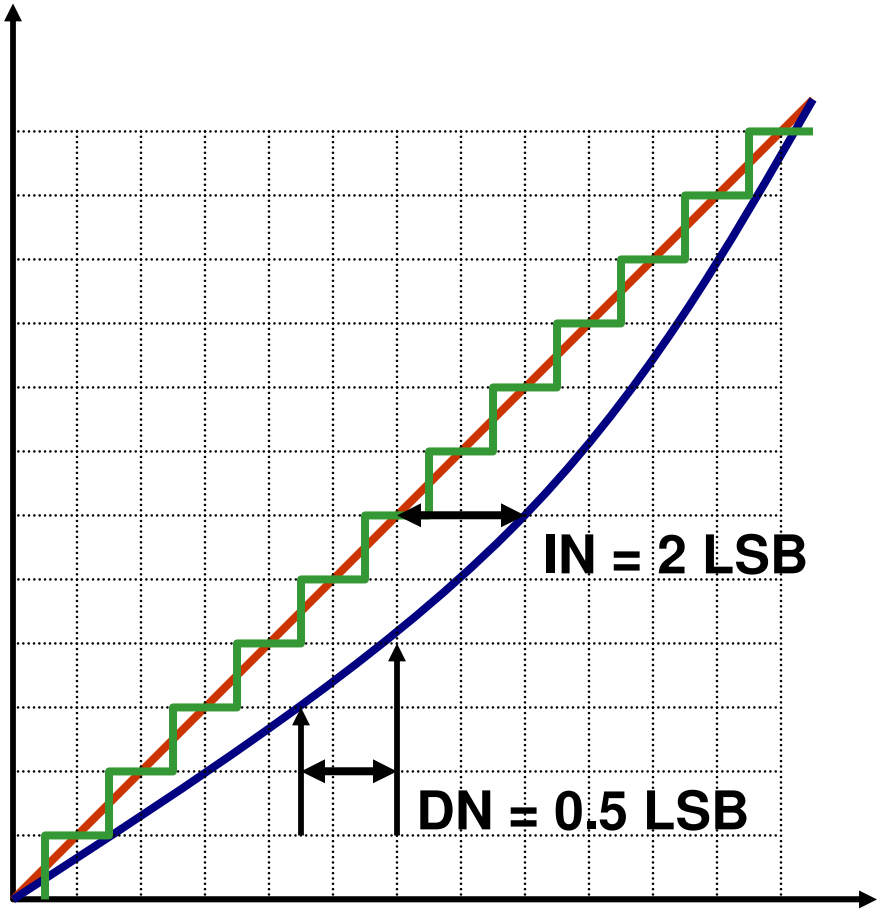
ADC – Nonlinearity Error

- **Nonlinearity error**: The deviation of the output quantity from a specified linear reference



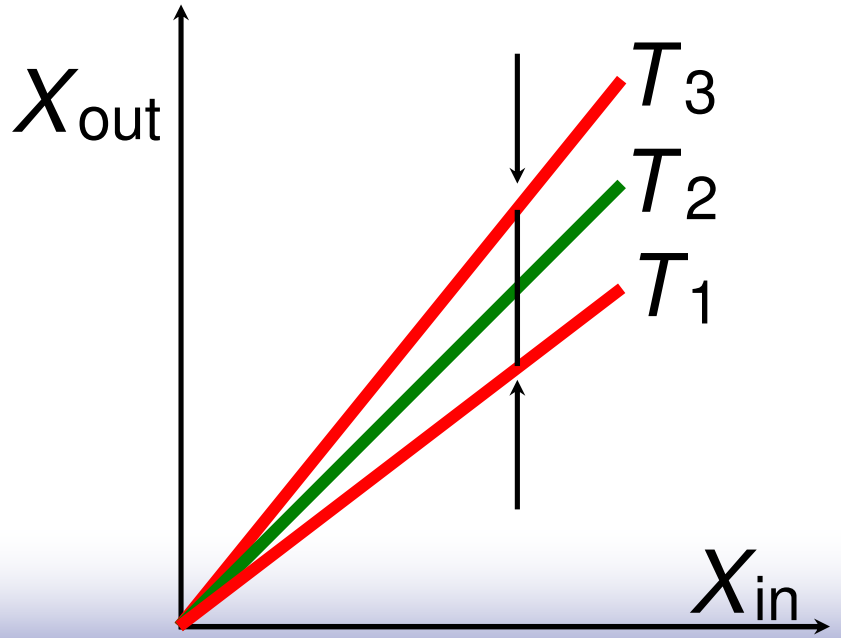
ADC – Nonlinearity Error

- **Integral Nonlinearity:**
  Worst-case deviation from the ideal transfer characteristic curve
- **Differential Nonlinearity:**
  Difference between the actual transfer ratio and the ideal ratio



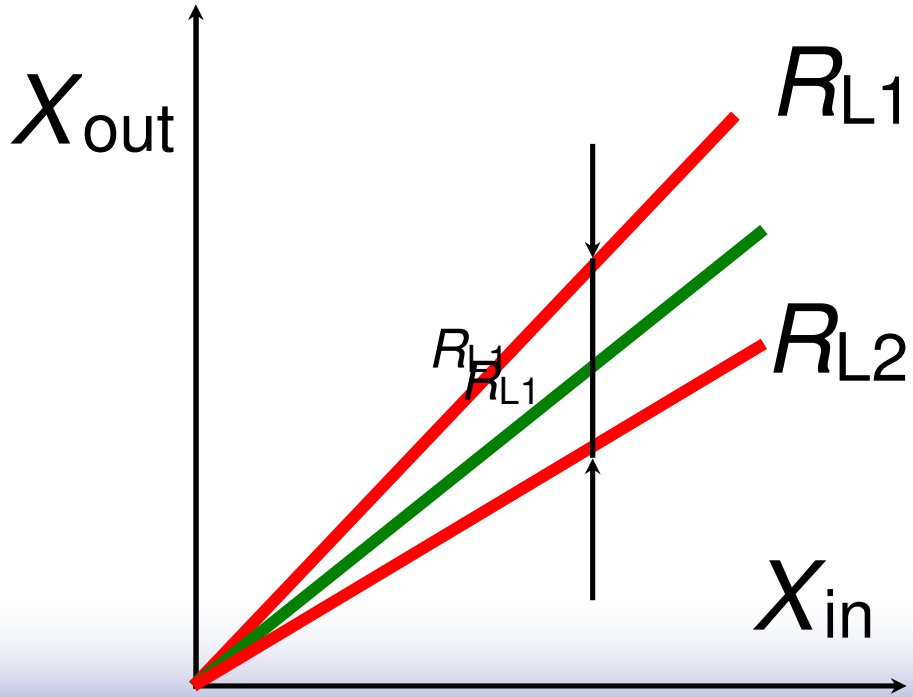
ADC – Temperature-Dependent Error

- **Temperature-Dependent Error:** Due to the change in ambient temperature or temperature variation due to self-heating (temperature stability, temperature coefficient)



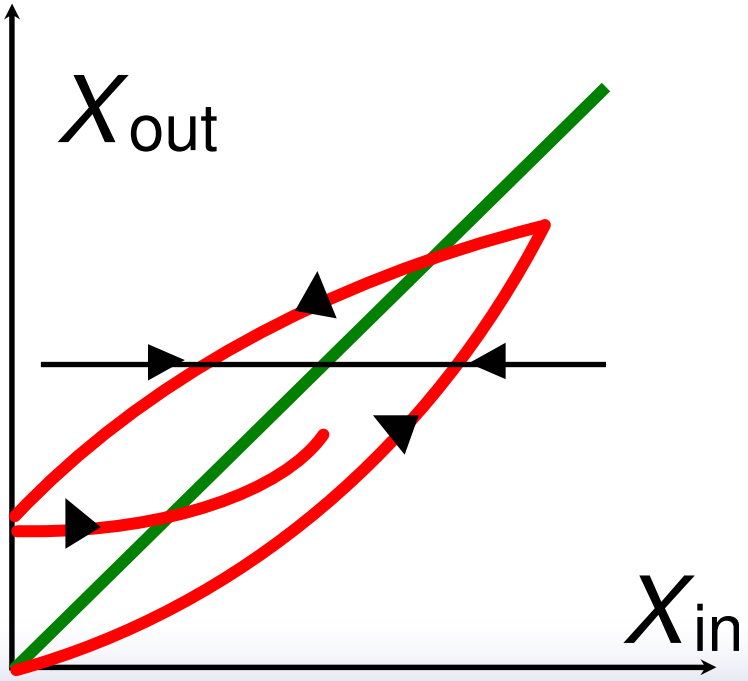
ADC – Load-Dependent Error

- **Load Error**: Loading error is due to the effect of a load impedance upon the converter or signal source driving it.



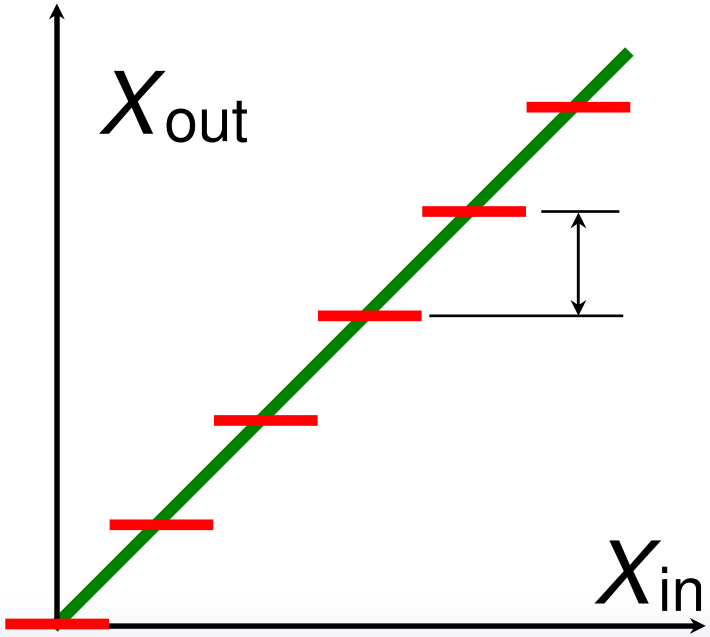
ADC – Hysteresis Error

- **Hysterisis Error**: The difference between the increasing and decreasing input values that produce the same output



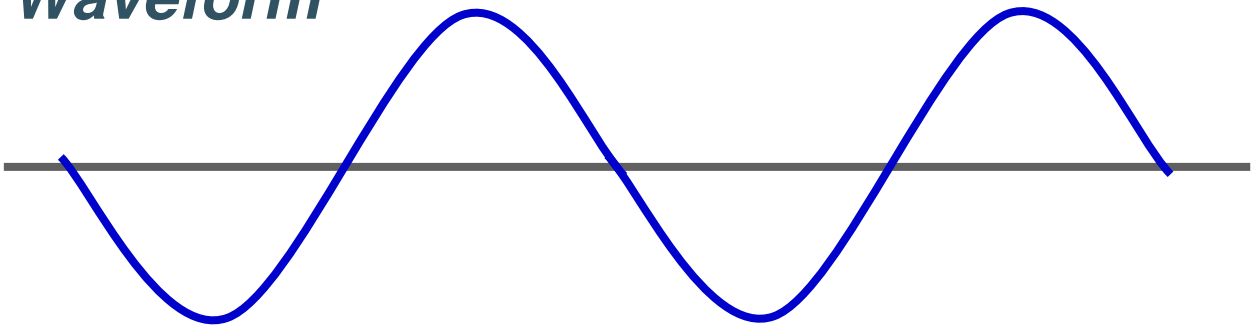
ADC – Resolution Error

- **Resolution Error:** The error due to the inability to respond to change of a variable smaller than a given increment

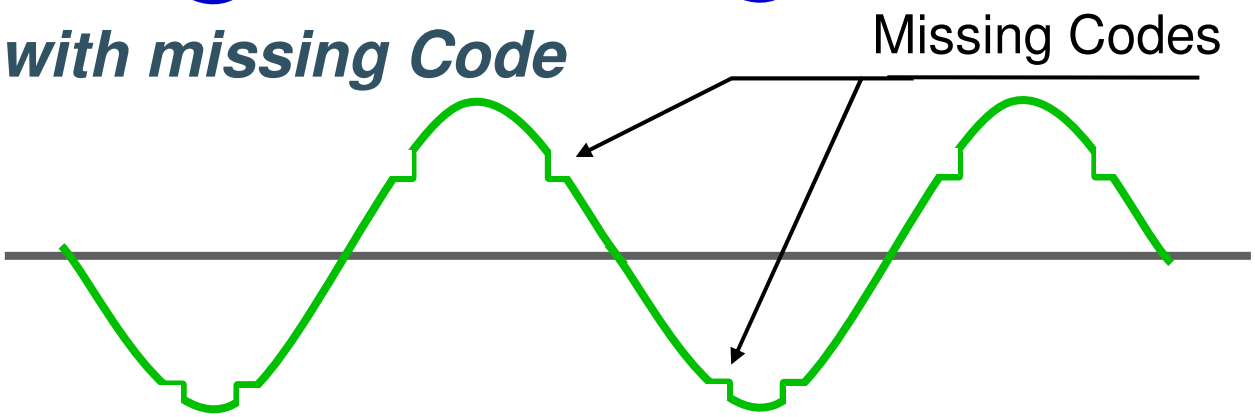


ADC – Missing Code Error

Ideal Input Waveform



Quantized with missing Code



Quantization Error

11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
- ADC and DAC Circuit Structure
- ADC/DAC Specification and Fault Models
- **IEEE Std. 1057**
- Time-Domain ADC Testing
- Frequency-Domain ADC Testing

IEEE 1057 Standard

- Scope
  - Covers electronic digitizing waveform recorders, waveform analyzers and digitizing oscilloscopes with digital outputs.
  - Applies to, but is not restricted to, general-purpose waveform recorders and analyzers.

IEEE 1057 Standard

- Purpose
  - Provides common methods for testing and terminology for describing the performance of waveform recorders.
  - Benefits users and manufacturers of such devices.
  - Presents many performance features, sources of error, and test methods.

IEEE 1057 – General Information

Model Number
Dimensions and weight
Power Requirement
Environmental conditions (tem., humidity, EMC/EMI, etc.)
Any special or peculiar characteristics
Available options and accessories
Exception to the above parameters where applicable
Calibration interval

IEEE 1057 – Minimum Specification

Number of digitizing bits	Input impedance
Sample rates	Analog bandwidth
Memory length	Input signal ranges

IEEE 1057 – Additional Specifications

Gain	Fixed error in sample time
Offset	Trigger delay and jitter
Differential nonlinearity	Trigger sensitivity
Integral nonlinearity	Trigger minimum rate of change
Harmonic distortion	Trigger hysteresis band
Spurious response	Trigger coupling to signal
Maximal static error	Crosstalk
Signal to noise ratio	Monotonicity
Effective bits	Hystersis
Peak error	Over voltage recovery
Random noise	Word error rate
Frequency response	Cycle time
Settling time	Common mode rejection ratio
Slew limit	Differential input impedance
Overshoot and precursors	Maximum operating common
Aperture uncertainty	mode signal level
Long-term stability	Transition duration of step response
Maximum common mode signal level	

IEEE 1057 – Test Methods

General methods	Triggering
Input impedance	Crosstalk
Gain and offset	Monotonicity
Noise	Hysteresis
Analog bandwidth	Overvoltage Recovery
Frequency response	Word Error Rate
Step Response parameters	Cycle Time
Time base errors	Differential Input Specification
Linearity, harmonic distortion, and spurious responses	

11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
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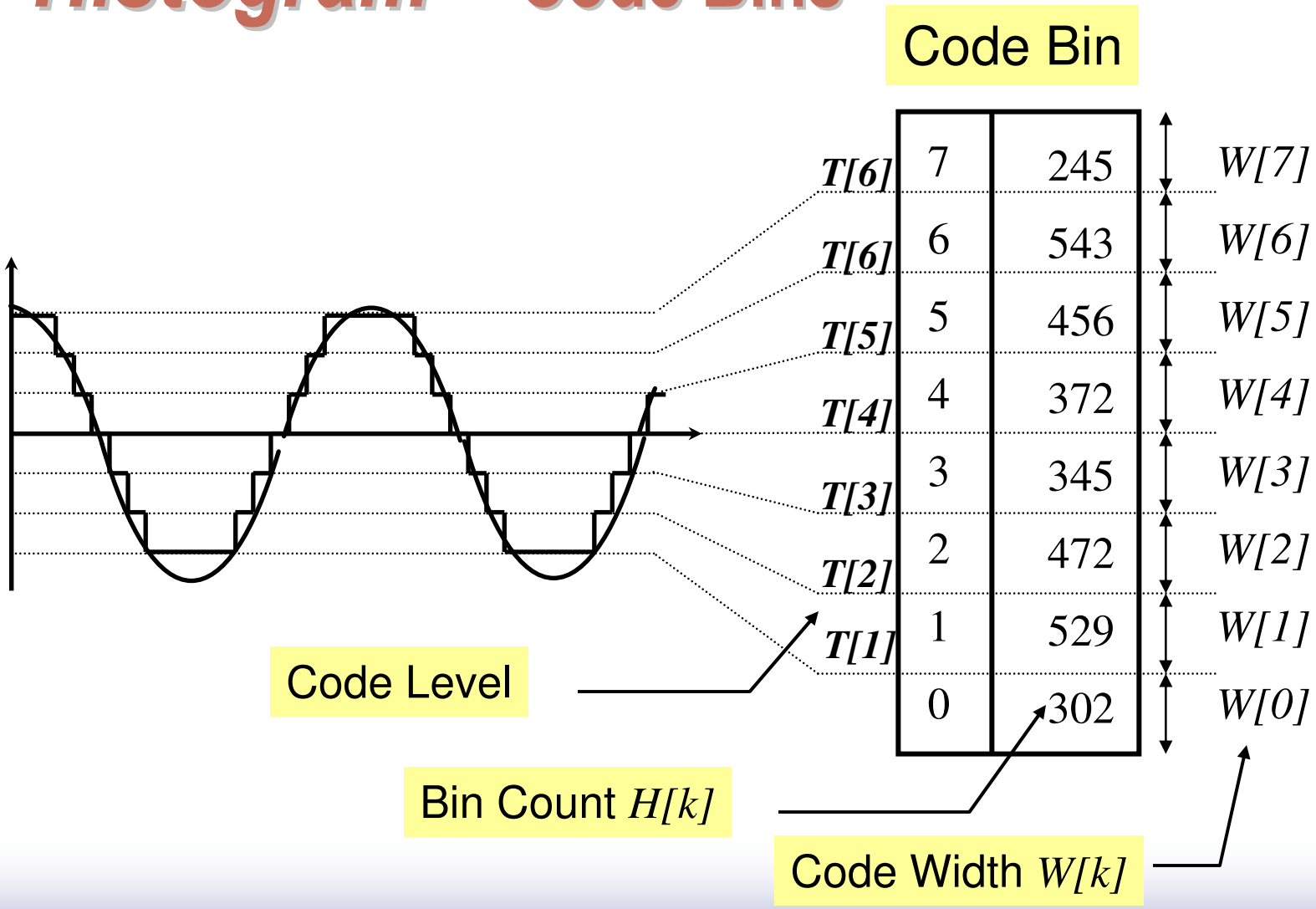
- **Time-Domain ADC Testing**
- Frequency-Domain ADC Testing

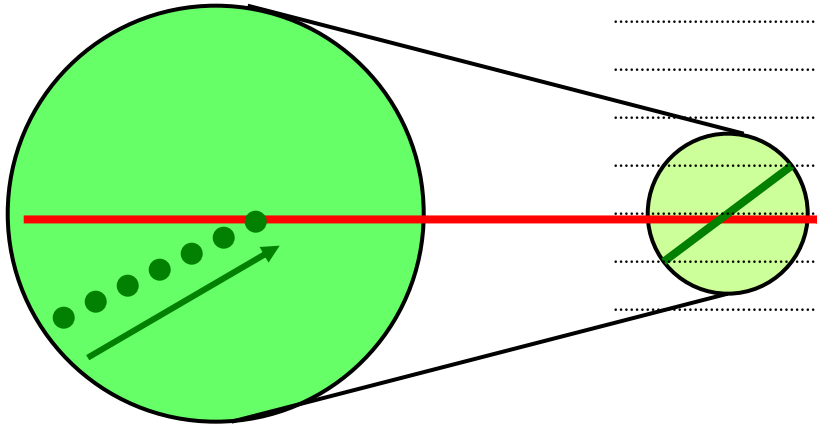
Histogram – Code Bins



Test Methods - Code Transition Level

Static Test Method

- Start from 2% below the transition level.
- Take a number of samples.
- Adjust the input level until the 50% codes are greater than k.



	Code Bin	
T[6]	7	0
T[6]	6	0
T[5]	5	12
T[4]	4	45
T[3]	3	443
T[2]	2	454
T[1]	1	30
	0	16

500

500

Samples	64	256	1024	4096
Precision	45%	23%	12%	6%

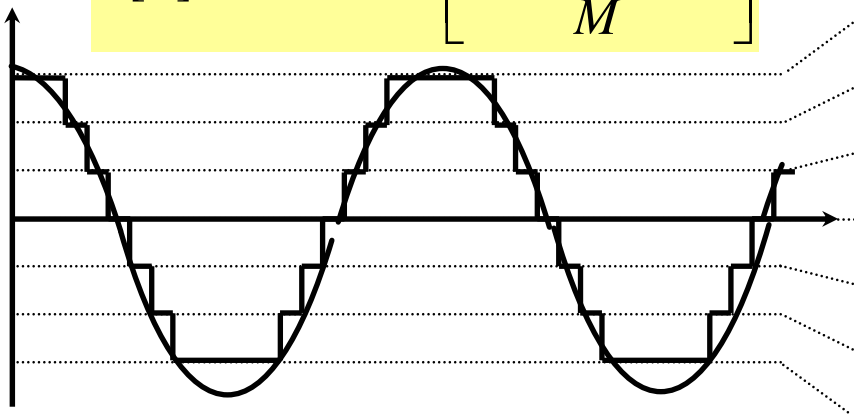
% of rms noise

Test Methods - Code Transition Level

Dynamic Test Method

- Apply full range sine wave
- Calculate the transition level from the bin count

$$T[k] = C - A\cos\left[\frac{\pi \cdot H_c[k-1]}{M}\right]$$



T[6]	7	245
T[6]	6	543
T[5]	5	456
T[4]	4	372
T[3]	3	345
T[2]	2	472
T[1]	1	529
	0	302

- A: Amplitude C: Offset
- *H[j]:* The code count of bin j.
- M: Total number of samples

$$H_c[j] = \sum_{i=0}^{j} H[i]$$

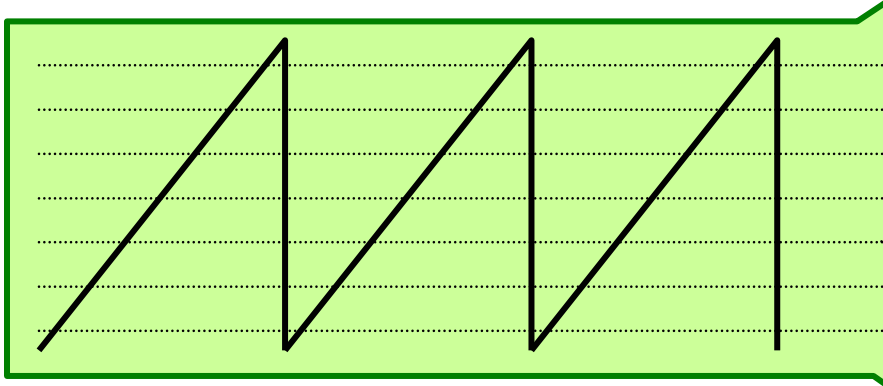
- Record Length M and Number of Cycles Mc must not have common term.

Test Methods - Gain and Offset

- Apply a slow ramp signal
- Construct the code bin table

Q: ideal width of the code bin

$$G \cdot T[k] + V_{os} + \varepsilon[k] = Q \cdot (k-1) + T_1$$



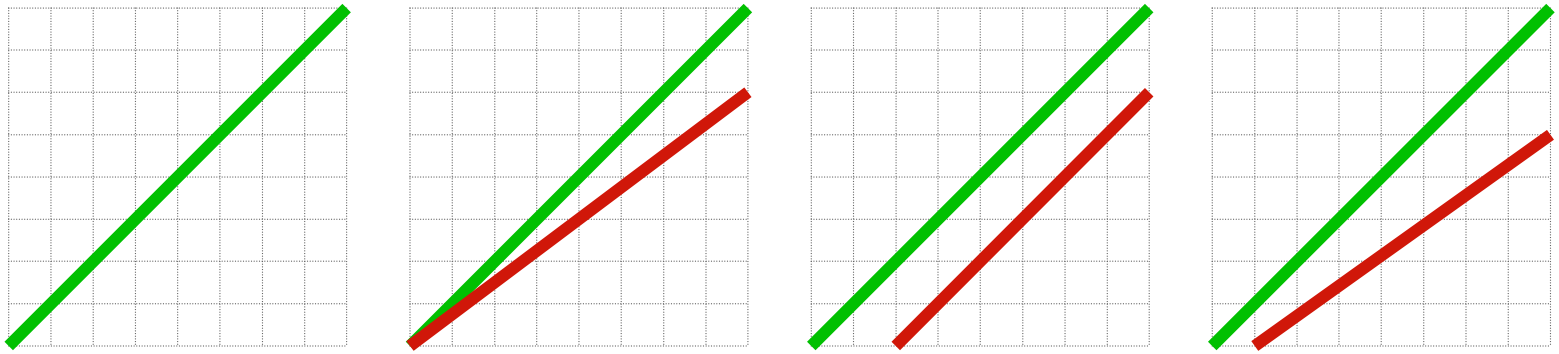
T[6]	7	203
T[6]	6	443
T[5]	5	440
T[4]	4	435
T[3]	3	439
T[2]	2	429
T[1]	1	447
	0	330

$$V_{os} = T_1 + Q\left(2^N - 1\right) - \frac{G}{2^N - 1}\sum_{k=1}^{2^N-1} T[k]$$

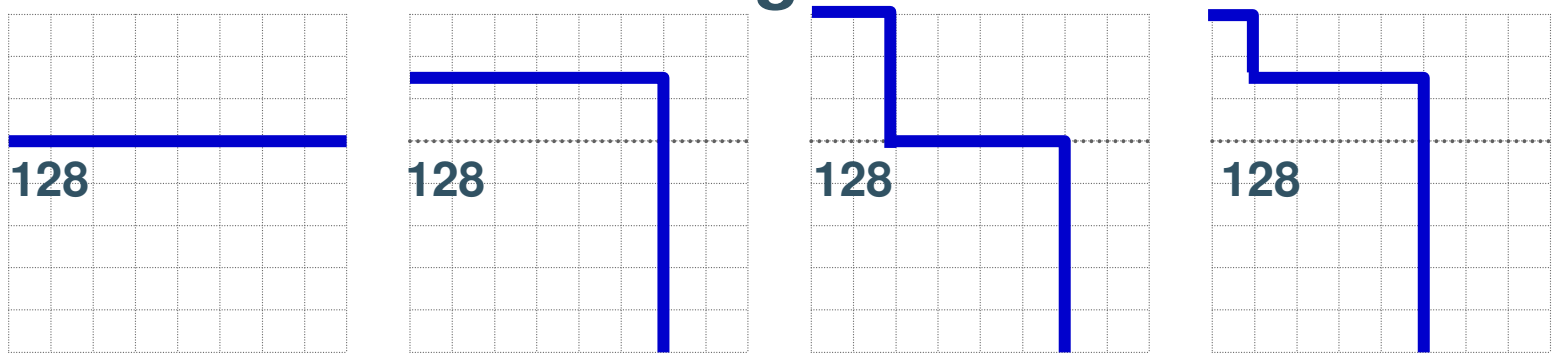
$$G = Q\frac{\left(2^N - 1\right)\sum_{k=1}^{2^N-1} kT[k]}{\left(2^N - 1\right)\sum_{k=1}^{2^N-1} T^2[k] - \left(\sum_{k=1}^{2^N-1} T[k]\right)^2} - Q\frac{\left(2^N - 1\right)\left(2^{N-1}\right)\sum_{k=1}^{2^N-1} T[k]}{\left(2^N - 1\right)\sum_{k=1}^{2^N-1} T^2[k] - \left(\sum_{k=1}^{2^N-1} T[k]\right)^2}$$

Test Methods - Gain and Offset (Example)

Transfer Curves



Histograms



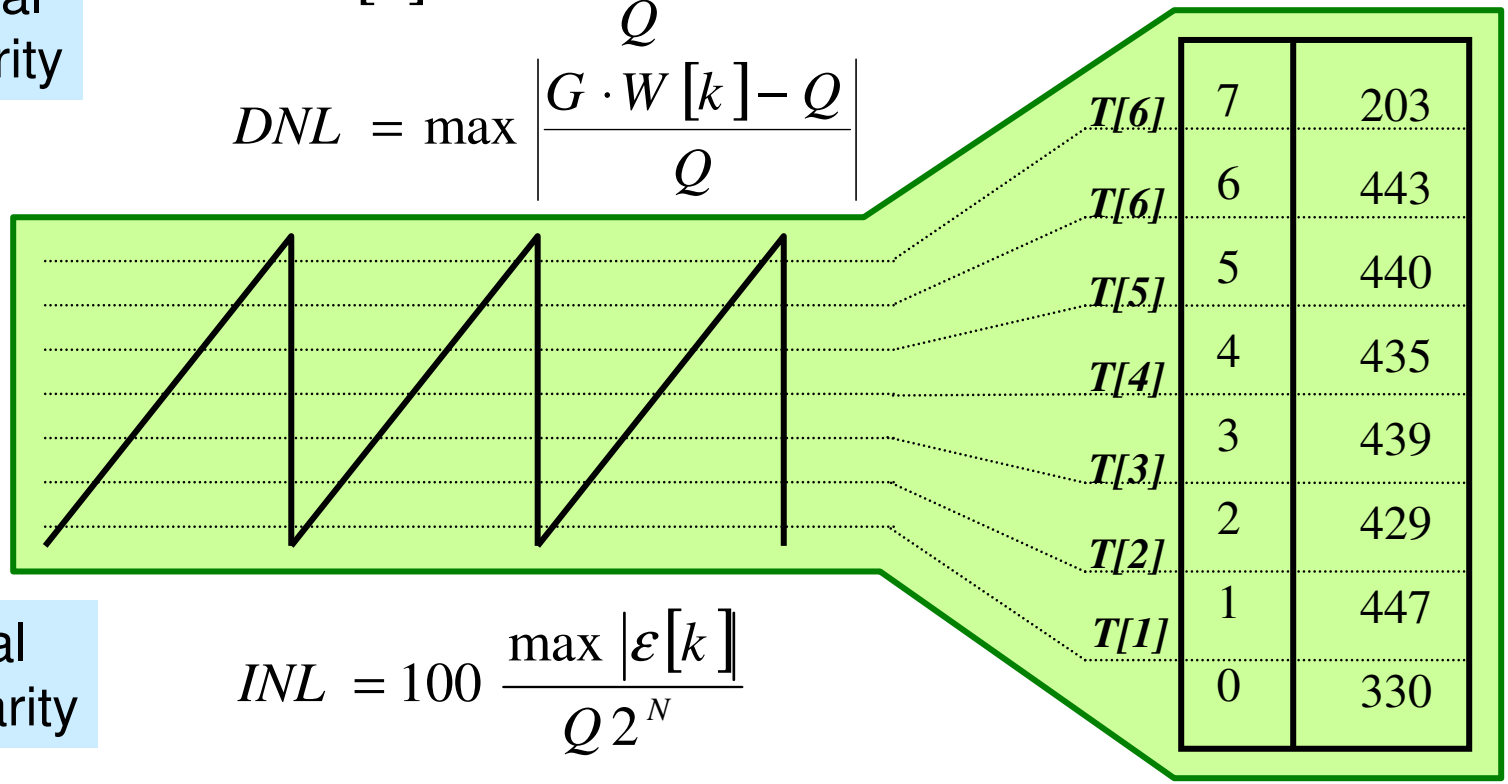
Ideal | Gain Error | Offset Error | Game/Offset

Test Methods - Nonlinearity

Differential Nonlinearity

$$DNL[k] = \frac{G \cdot W[k] - Q}{Q}$$

$$DNL = \max \left| \frac{G \cdot W[k] - Q}{Q} \right|$$



Integral Nonlinearity

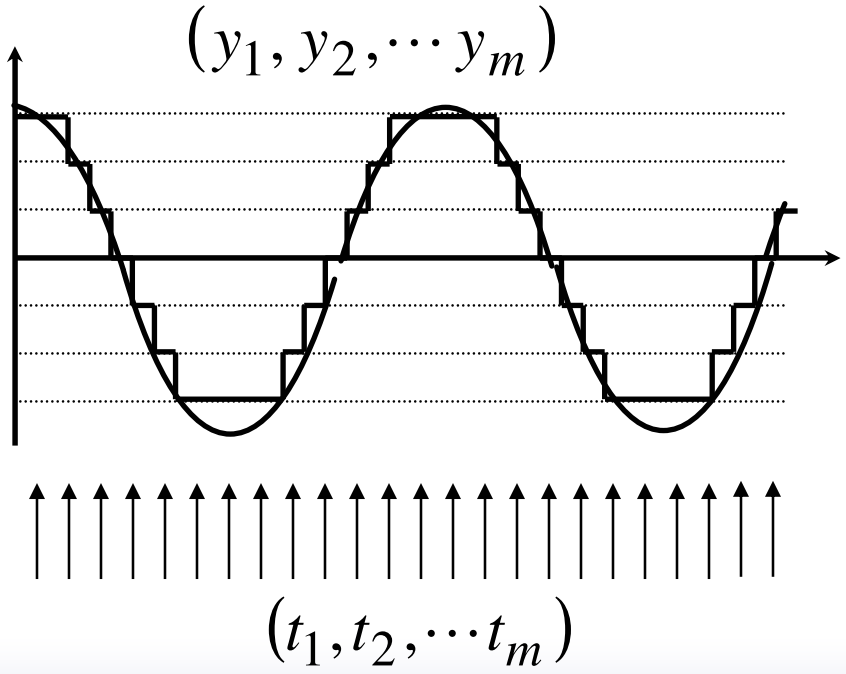
$$INL = 100 \frac{\max |\varepsilon[k]|}{Q 2^N}$$

Maximal Static Error

$$MSE = 100 \frac{\max |T[k] - Q(k-1) - T_1|}{Q 2^N}$$

Test Methods - Sine Wave Fitting

- Try to fit the sine wave to find the gain A', offset Co, and phase shift θ.
- There are matrix based and nonmatrix methods.



$$y_i = A\sin\omega_o t_i + C_o$$

$$y'_i = A'\sin(\omega t_i + \theta) + C$$

$$y'_i = A\sin(\omega t_i) + B\cos(\omega t_i) + C$$

$$Min\left[\sum_{i=1}^{m}(y_i - A\cos(\omega t_i) - B\cos(\omega t_i) - C)^2\right]$$

Test Methods - Sine Wave Fitting

Original Signal: $y(t) = A_o \sin(\varpi_o t) + C_o$

Curve Fitted: $y'(t) = A\sin(\varpi t) + B\cos(\varpi t) + C$

Gain Error: $\dfrac{\sqrt{A^2 + B^2} - A_o}{A_o}$

Offset Error: $C - C_o$

Phase Error: $\theta = \tan^{-1}\left(-\dfrac{B}{A}\right)$

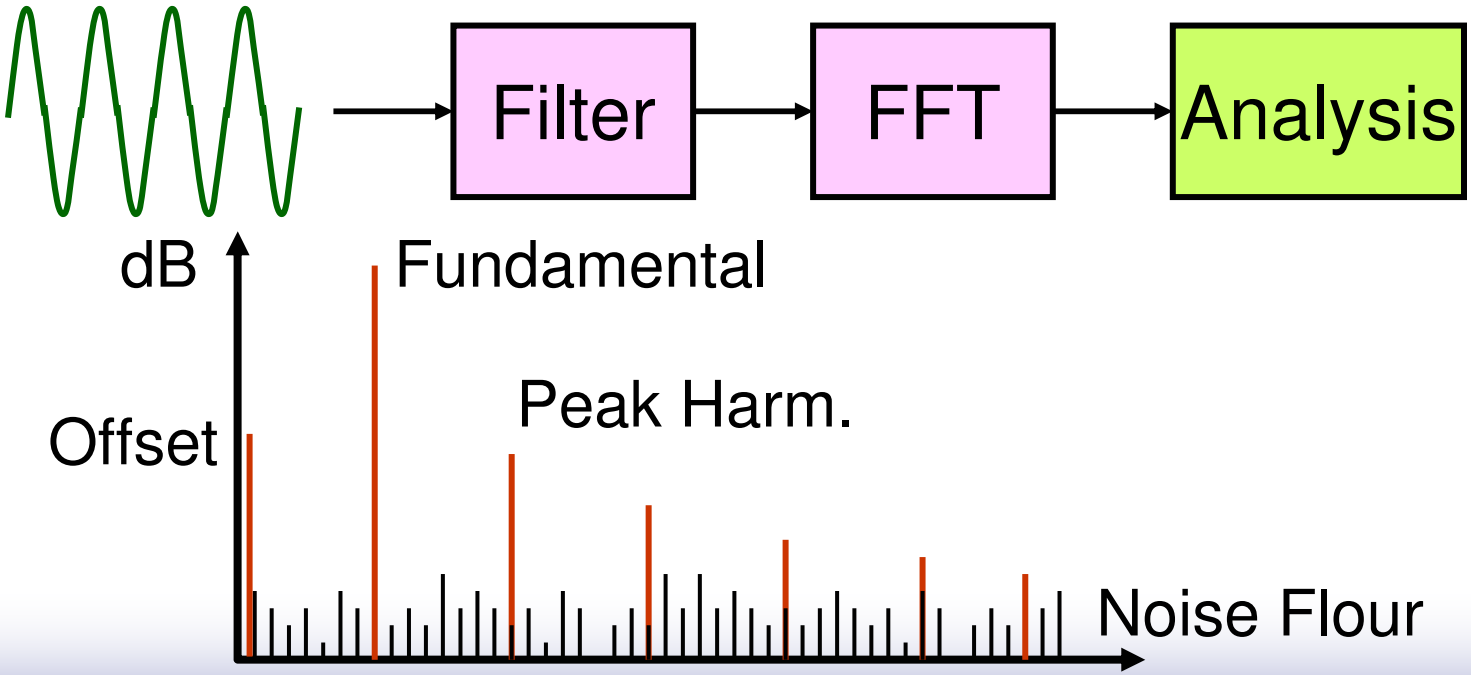
Frequency Error: $\dfrac{(\varpi - \varpi_o)}{\varpi_o}$

11.3 Mixed-Signal Testing

- Introduction to Analog-Digital Conversion
- ADC and DAC Circuit Structure
- ADC/DAC Specification and Fault Models
- IEEE Std. 1057
- Time-Domain ADC Testing
- **Frequency-Domain ADC Testing**

ADC – Frequency Domain Testing

- Similar to Analog AC Testing
- Apply sinusoidal waveform
- Do Fourier transform on response waveform
- Obtain F domain properties mathematically.

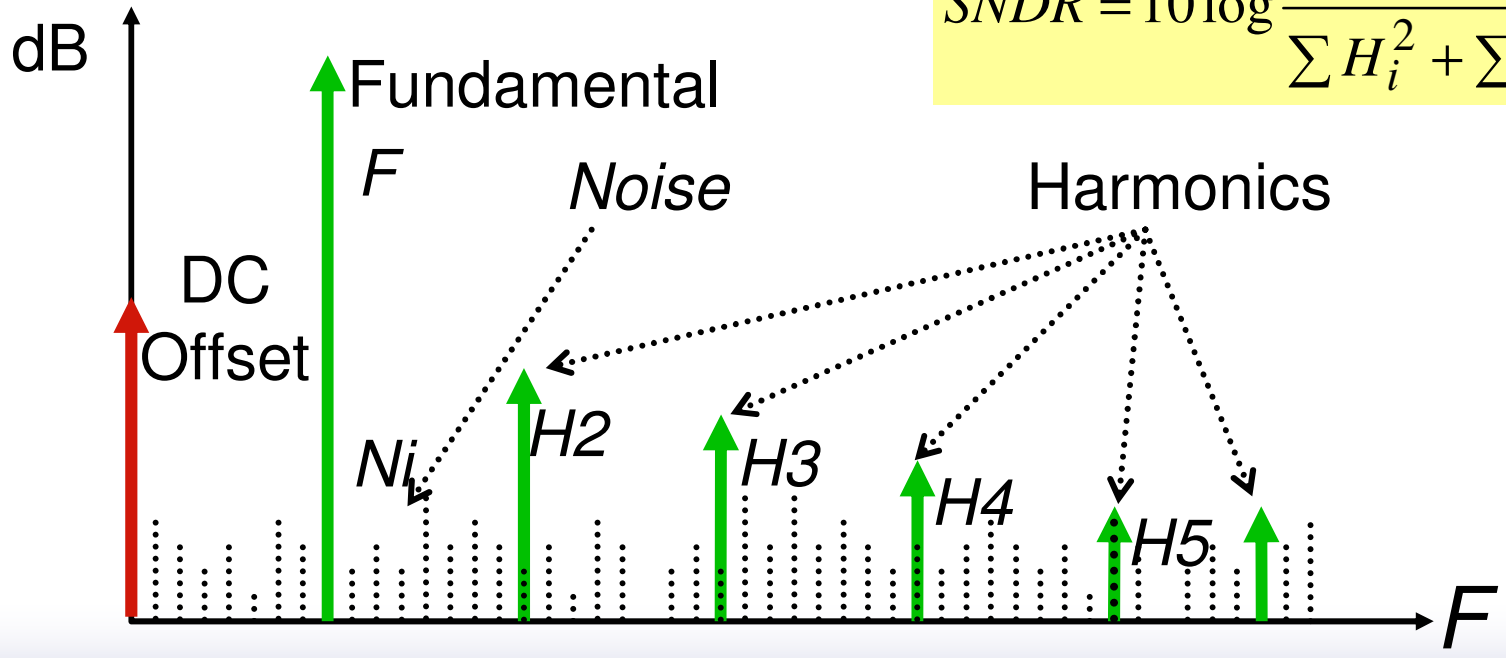


ADC – Frequency Domain Testing

$$THD = 10\log\frac{F^2}{\sum H_i^2} = 100\times\frac{F^2}{\sum H_i^2}\%$$

$$SNR = 10\log\frac{F^2}{\sum N_i^2}$$

$$SNDR = 10\log\frac{F^2}{\sum H_i^2 + \sum N_i^2}$$

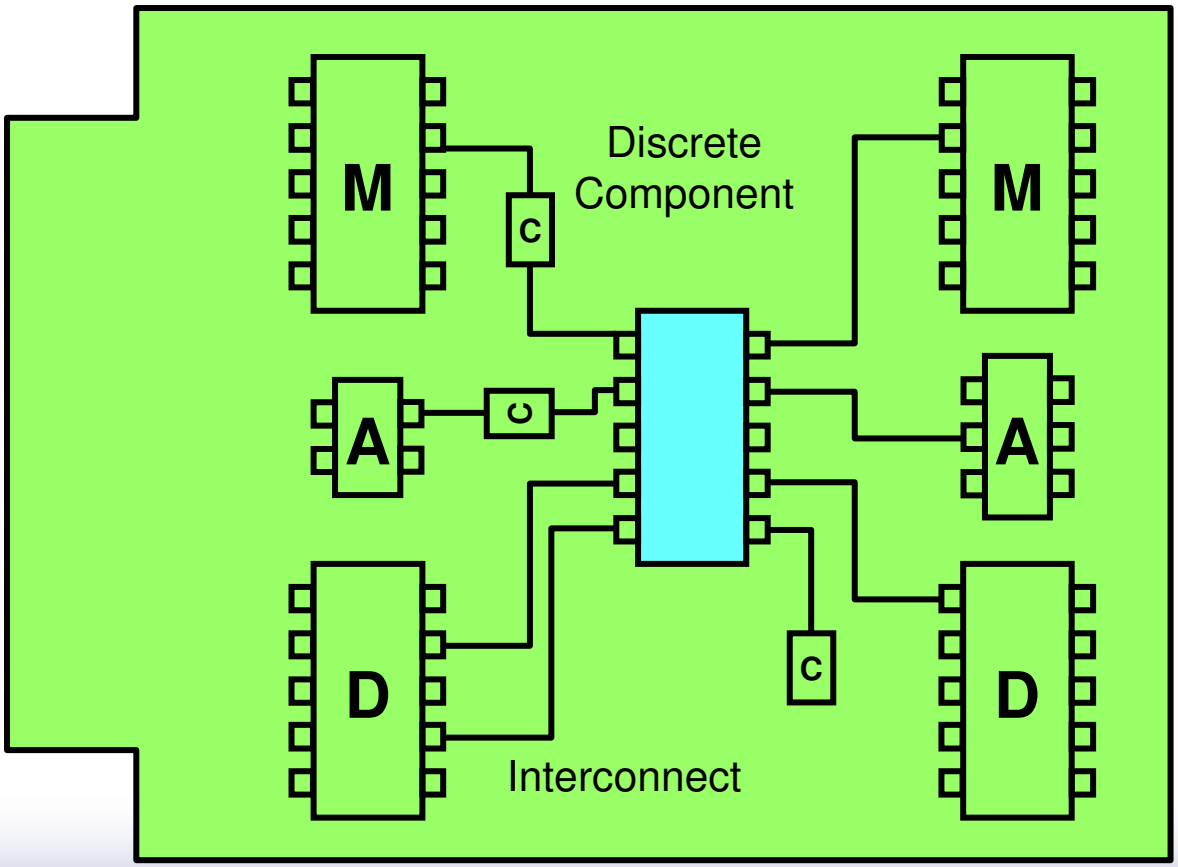


11.4 IEEE Std. 1149.4 Standard for a Mixed-Signal Test Bus

- **IEEE Std. 1149.4 Overview**
- IEEE Std. 1149.4 Circuit Structures
- IEEE Std. 1149.4 Instructions
- IEEE Std. 1149.4 Test Modes

IEEE 1149.4 - Overview

- Target mixed signal Printed Circuit Assembles (***PCA***).
- Components:
  - Mixed Signal
  - Digital
  - Analog
  - Discrete

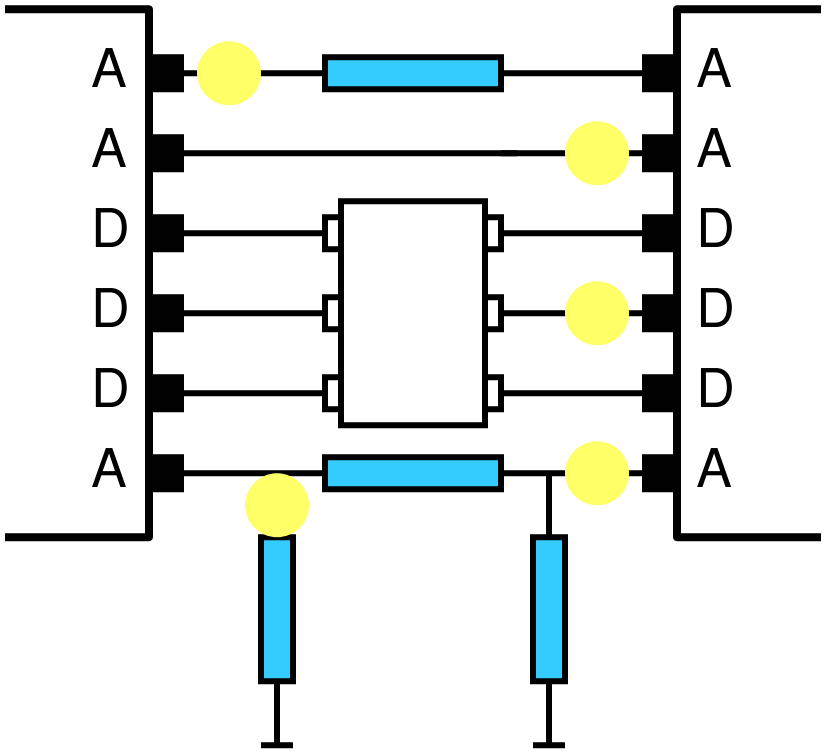


M: Mixed-signal Component
A: Analog Component
D: Digital Component

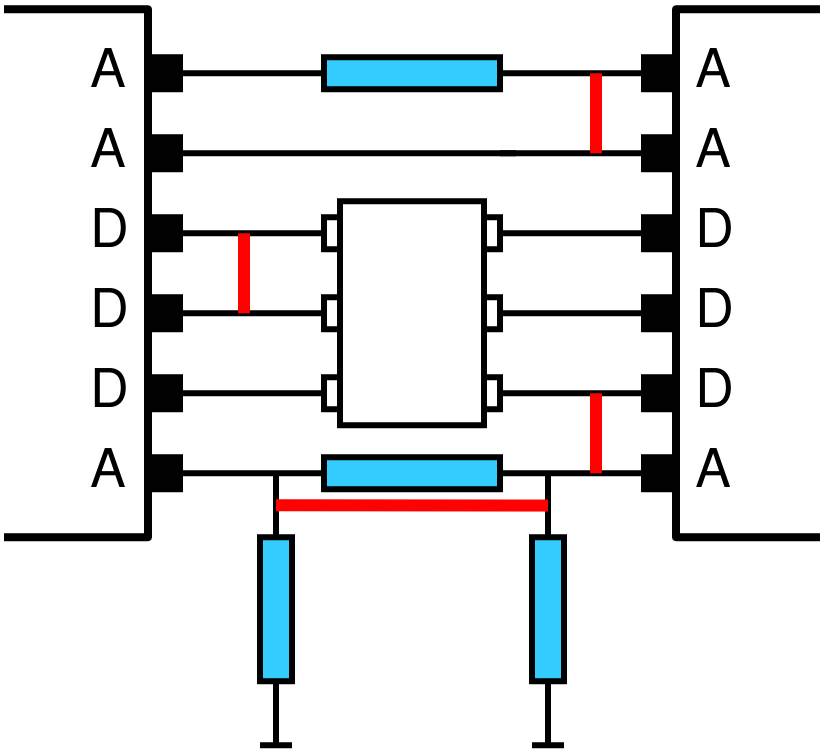
IEEE 1149.4 - Scope

- Provide standardized approaches to
  - ***Interconnect Test***
  - ***Parametric Test***
  - ***Internal Test***

IEEE 1149.4 - Interconnect Test

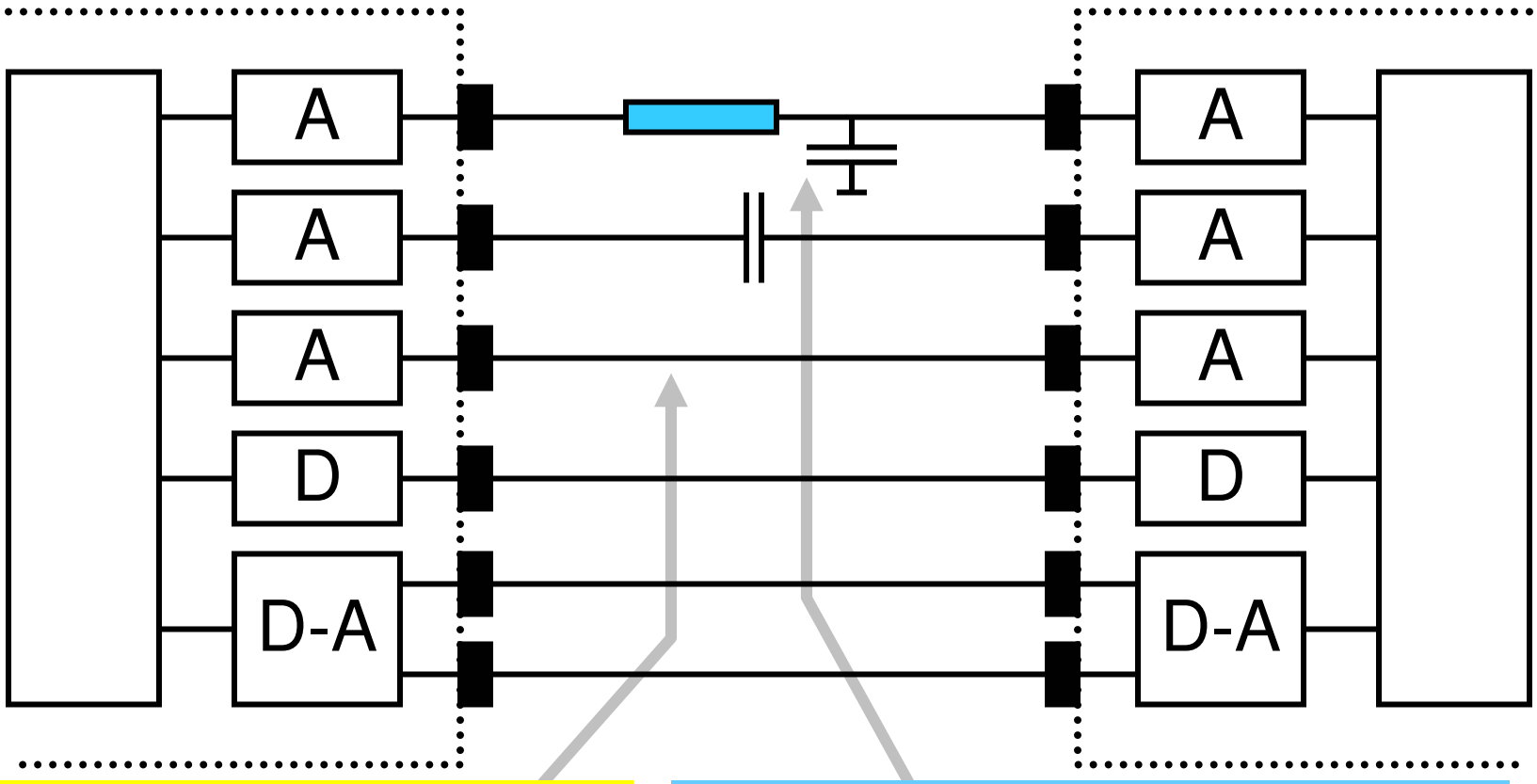


Open Defects

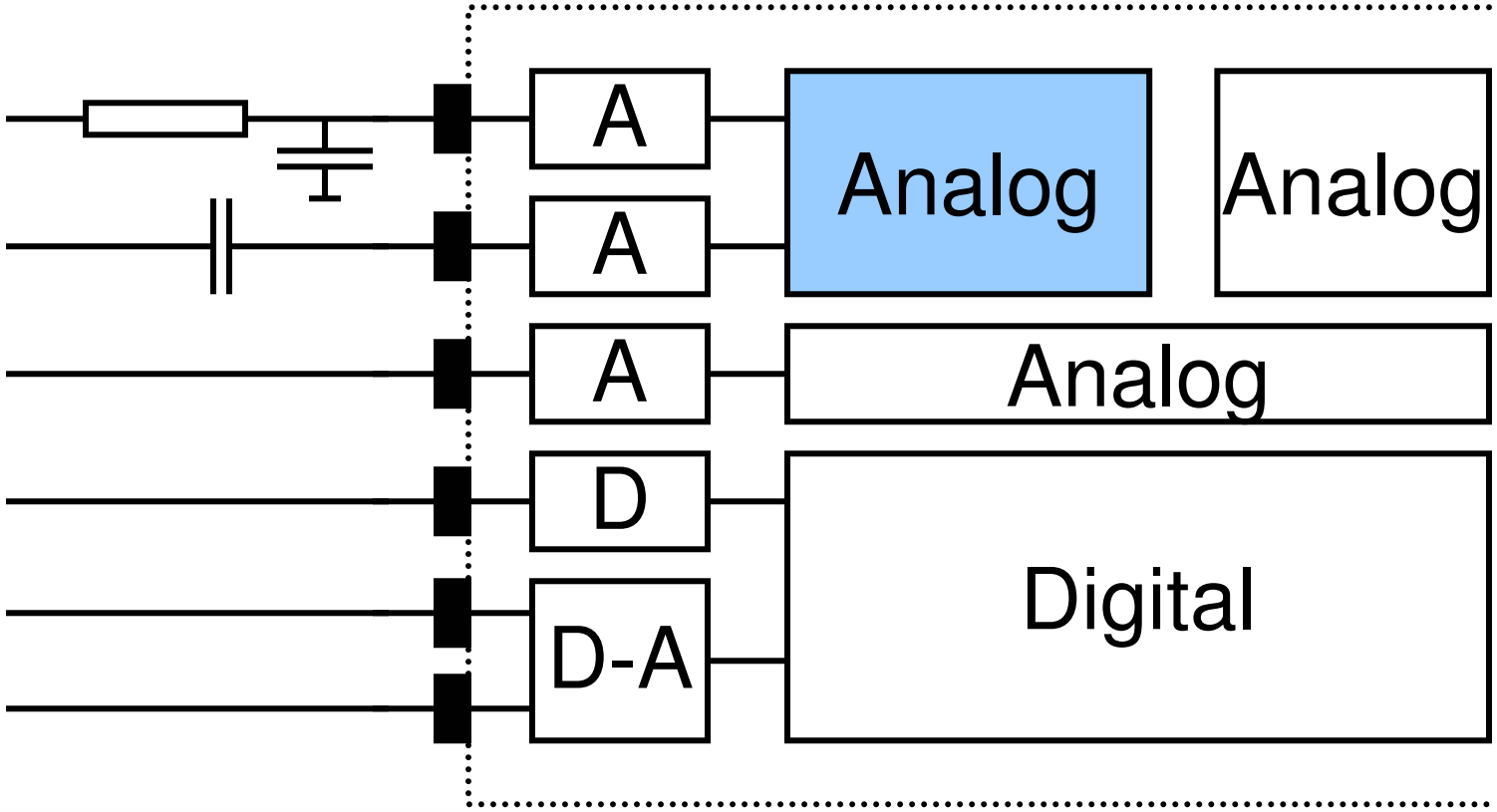


Short Defects

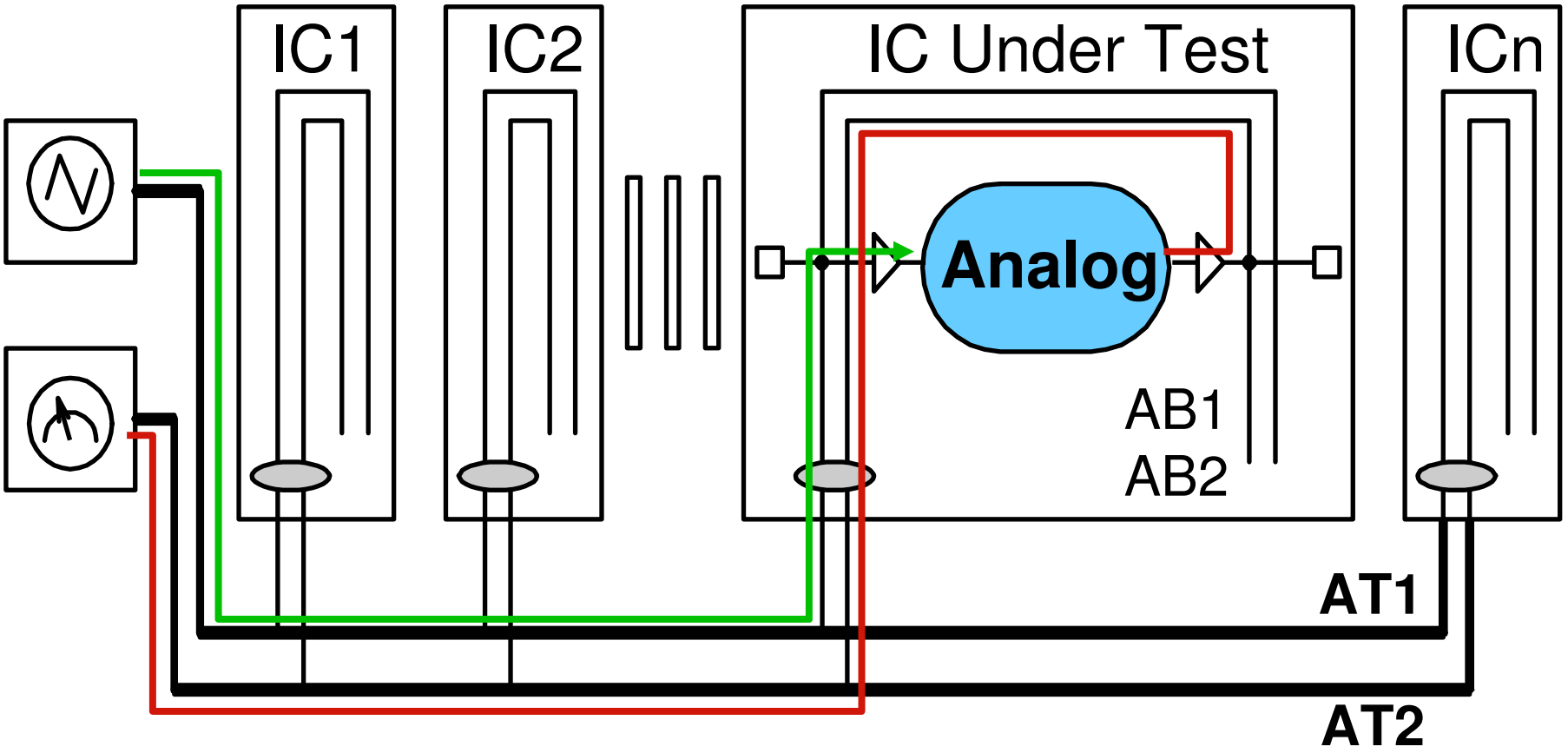
IEEE 1149.4 - Parametric Test



IEEE 1149.4 - Internal Test



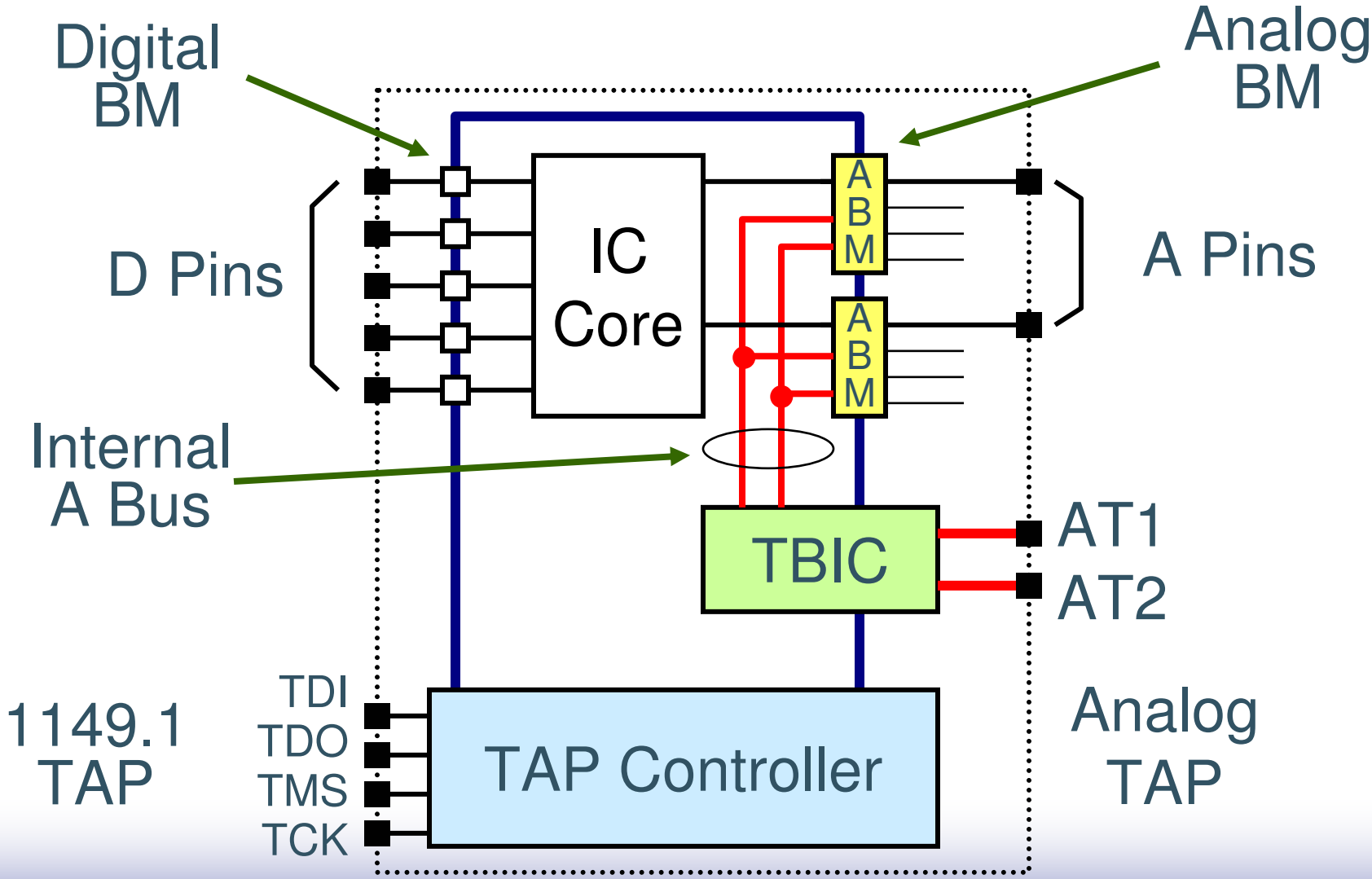
IEEE 1149.4 - Architecture



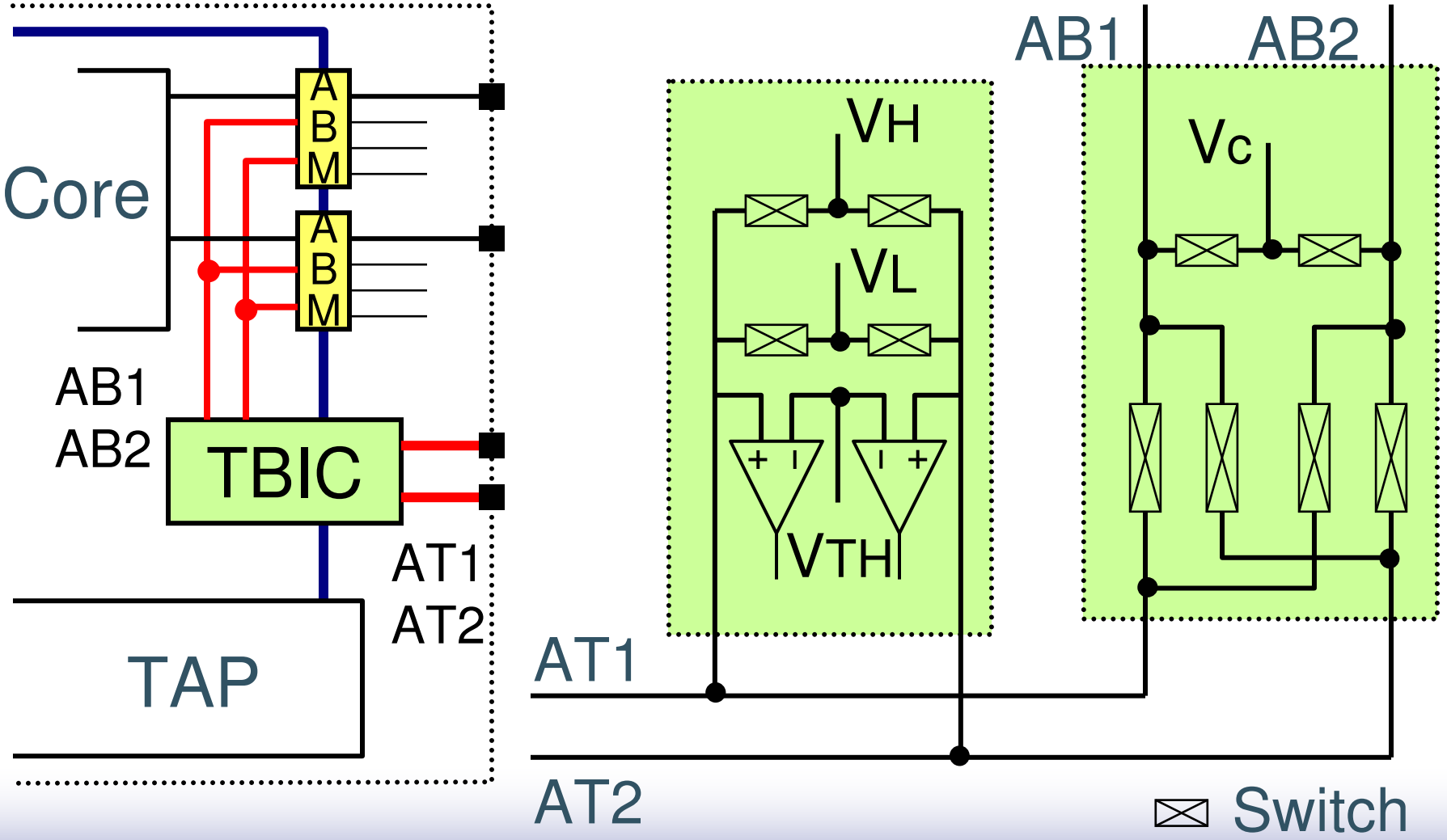
11.4 IEEE Std. 1149.4 Standard for a Mixed-Signal Test Bus

- IEEE Std. 1149.4 Overview
- **IEEE Std. 1149.4 Circuit Structures**
- IEEE Std. 1149.4 Instructions
- IEEE Std. 1149.4 Test Modes

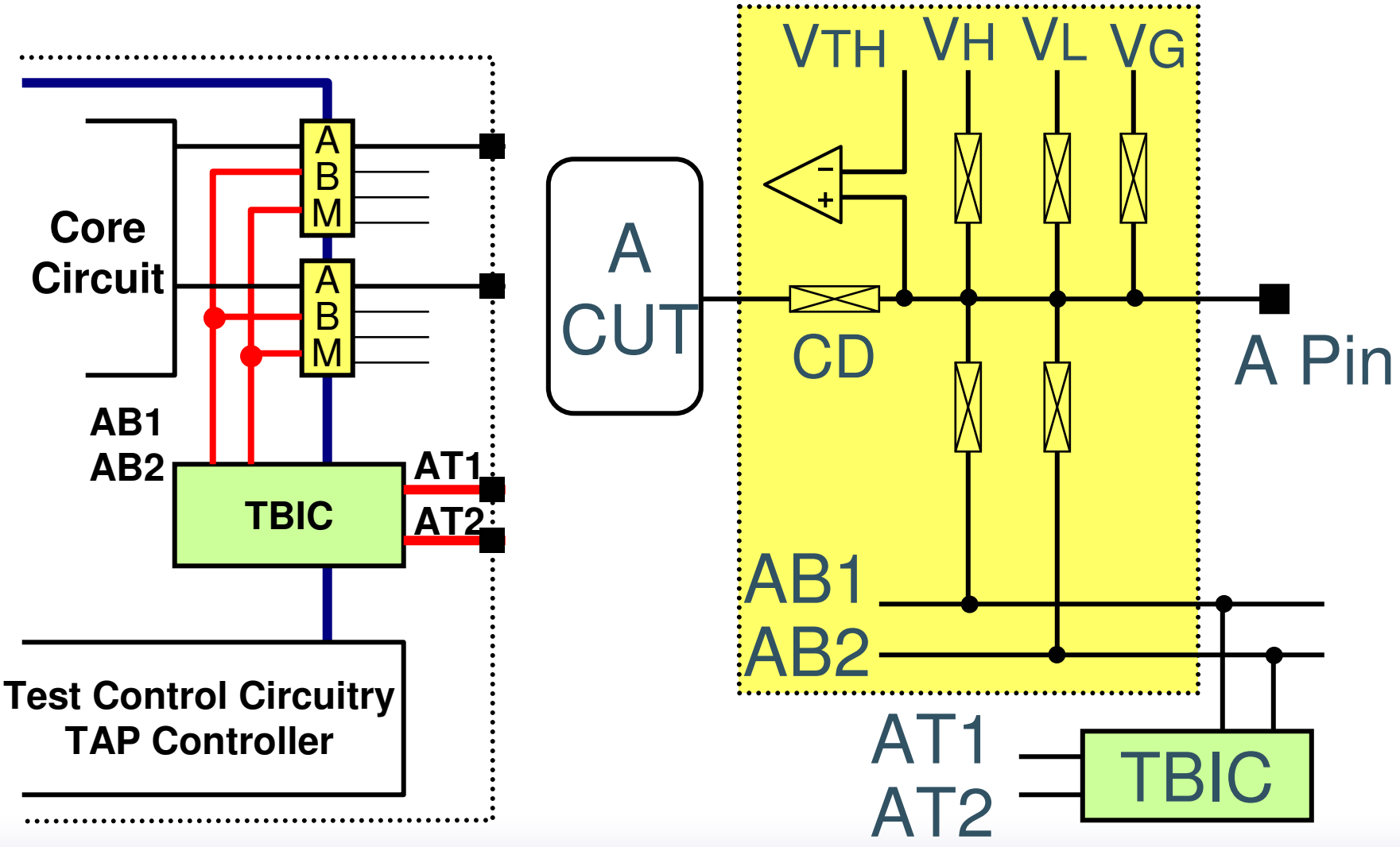
IEEE 1149.4 - Architecture



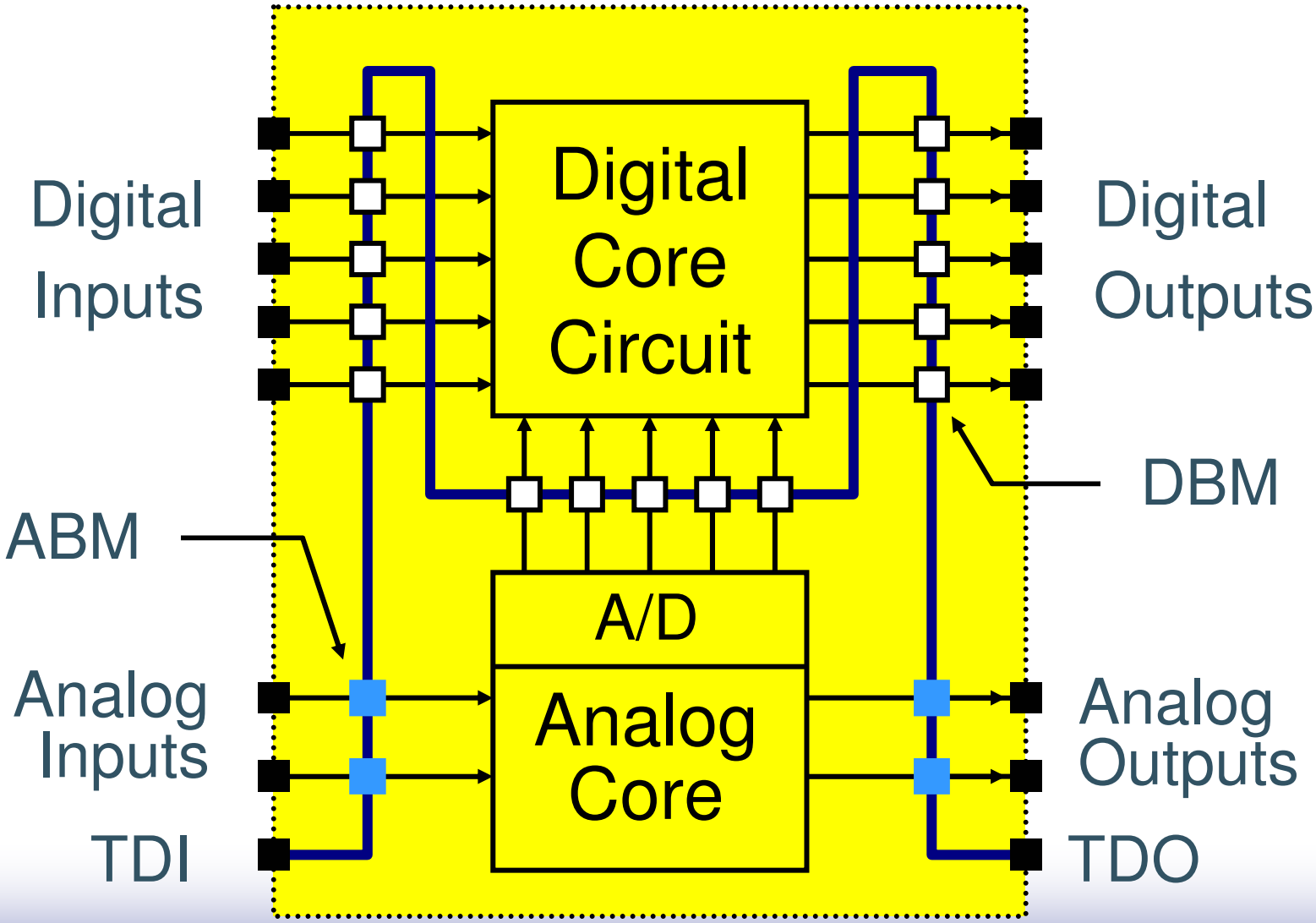
IEEE 1149.4 - TBIC



IEEE 1149.4 - ABM



1149.4 – Mixed-Signal Architecture



11.4 IEEE Std. 1149.4 Standard for a Mixed-Signal Test Bus

- IEEE Std. 1149.4 Overview
- IEEE Std. 1149.4 Circuit Structures
- **IEEE Std. 1149.4 Instructions**
- IEEE Std. 1149.4 Test Modes

IEEE 1149.4 - Instructions

- Mandatory Instructions
  - BYPASS
  - SAMPLE/PRELOAD
  - EXTEST
  - PROBE
- Same as IEEE 1149.1

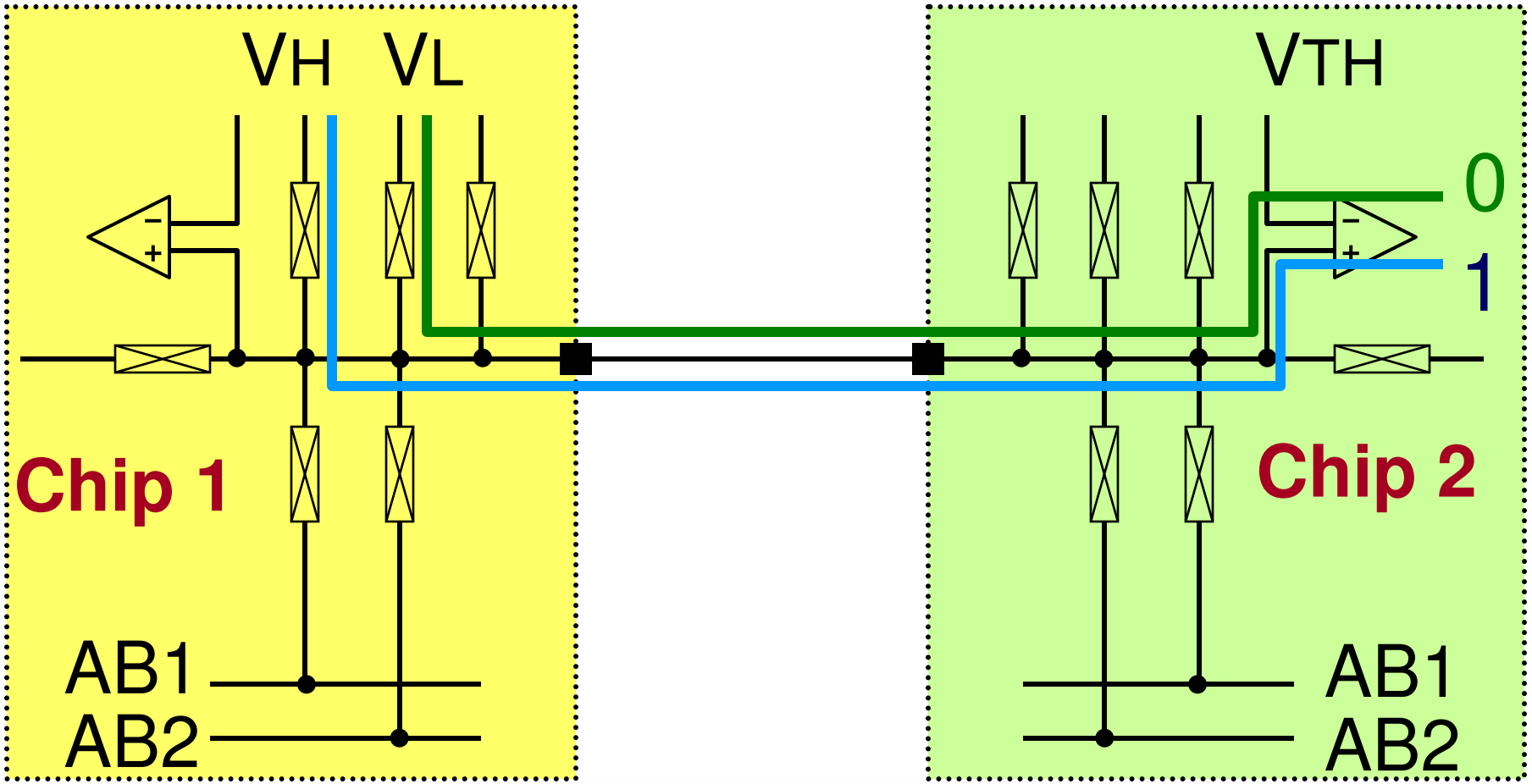
IEEE 1149.4 - Instructions

- Optional Instructions
  - INTEST
  - IDCODE/USERCODE
  - RUNBIST
  - CLAMP
  - HIGHZ
- Same as IEEE 1149.1

11.4 IEEE Std. 1149.4 Standard for a Mixed-Signal Test Bus

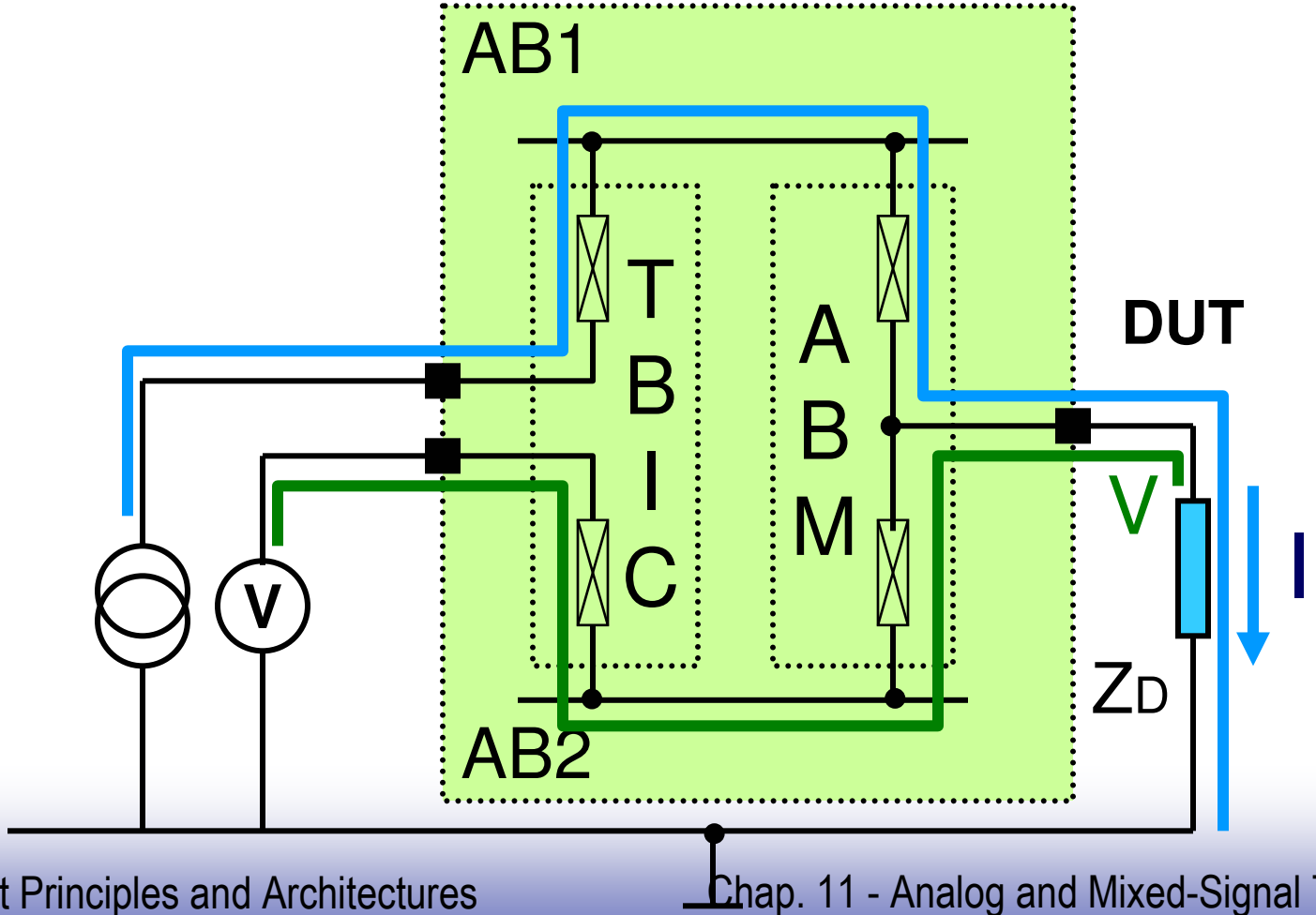
- IEEE Std. 1149.4 Overview
- IEEE Std. 1149.4 Circuit Structures
- IEEE Std. 1149.4 Instructions
- **IEEE Std. 1149.4 Test Modes**

1149.4 – Open/Short Interconnect Test



1149.4 – Extended Interconnect Test

- Grounded Impedance Measurement
- Apply current and measure voltage

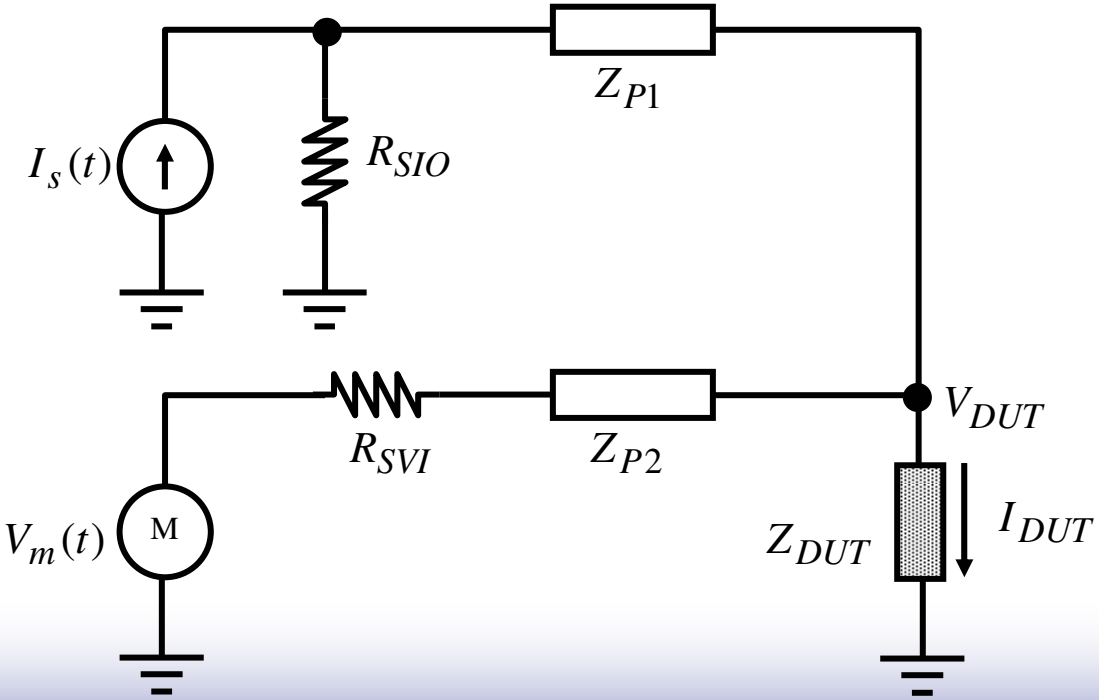


1149.4 – Extended Interconnect Test

- Equivalent Circuit Model.

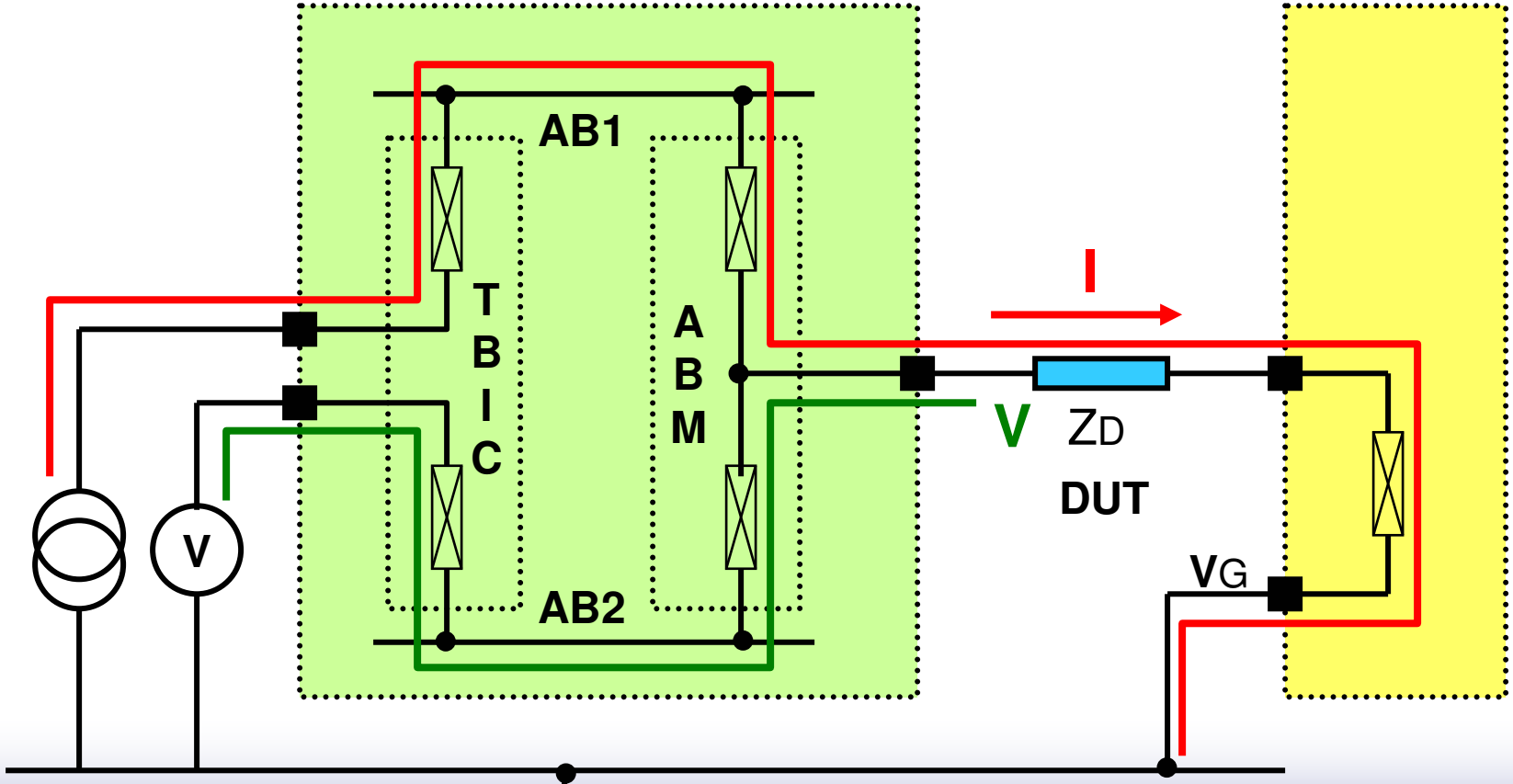
$$I_{DUT}(t) = I_s(t) \cdot \frac{R_{SIO}}{R_{SIO} + Z_{P1} + Z_{DUT}}$$

$$V_M(t) = V_{DUT}(t) \cdot \frac{R_{SVI}}{R_{SVI} + Z_{P2} + Z_{DUT}}$$



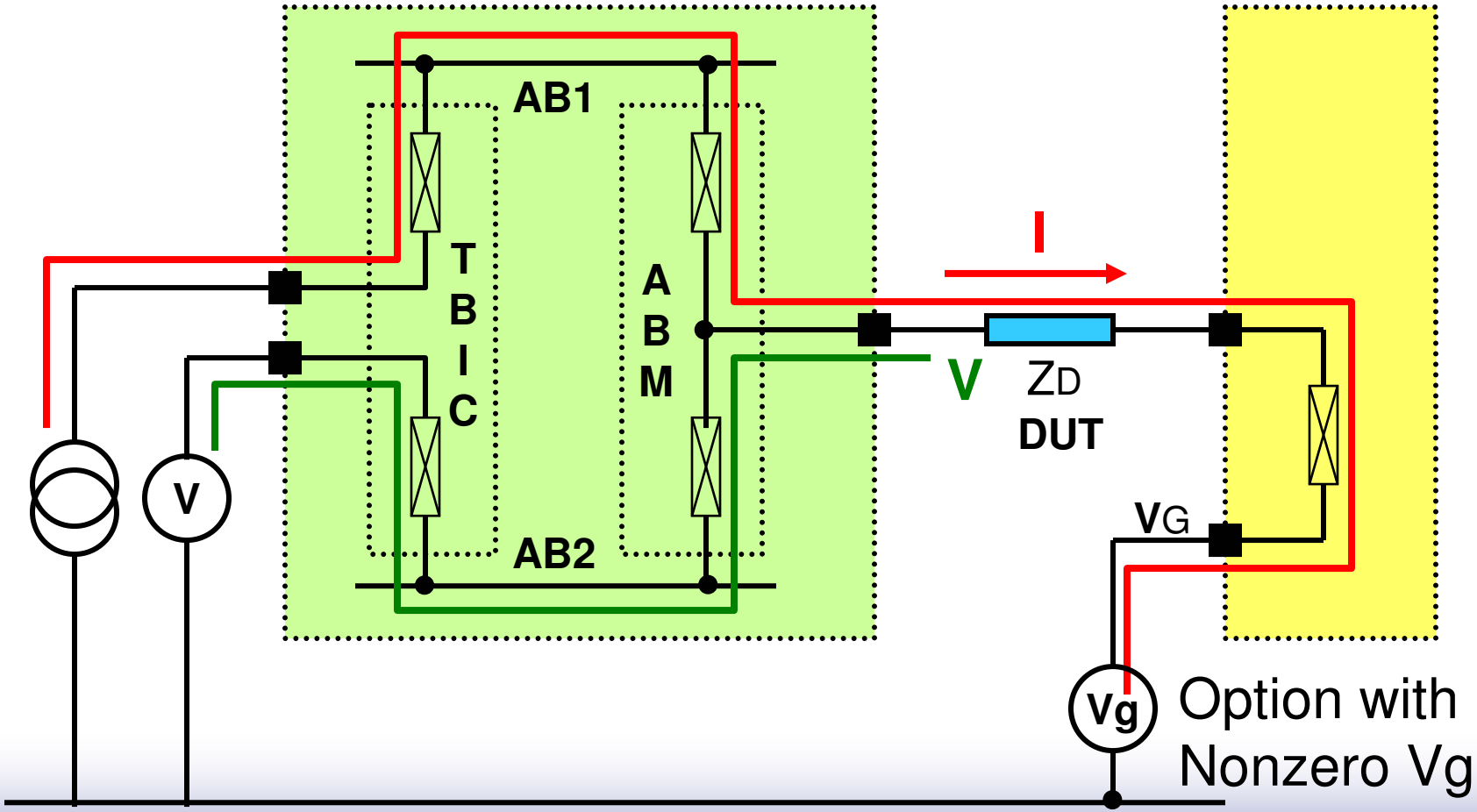
1149.4 – Extended Interconnect Test

- Floating Impedance Zd Measurement



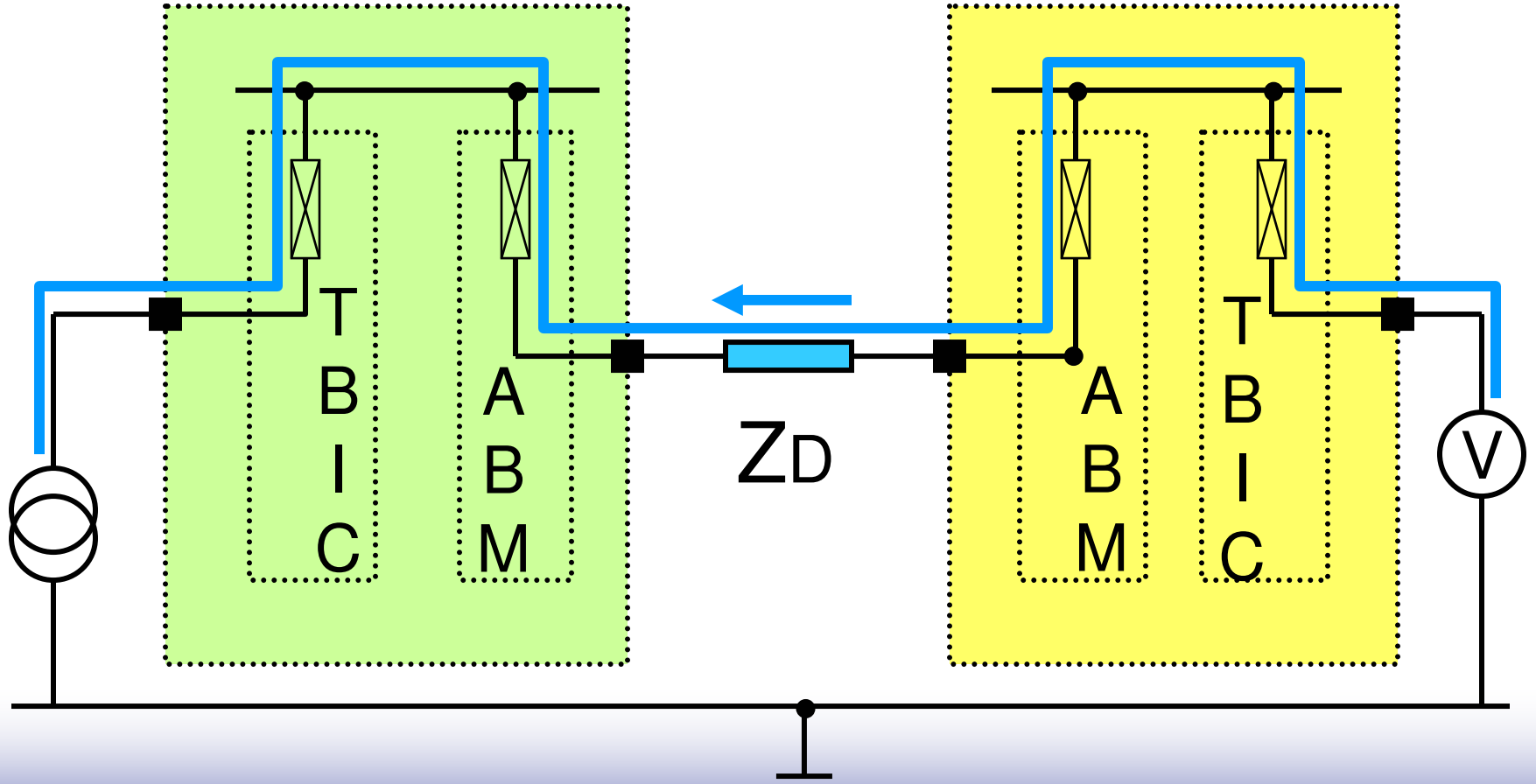
1149.4 – Extended Interconnect Test

- Floating Impedance Z_D with optional Vg



1149.4 – Extended Interconnect Test

- Apply voltage and measure current



1149.4 – Extended Interconnect Test

- Equivalent Circuit Model

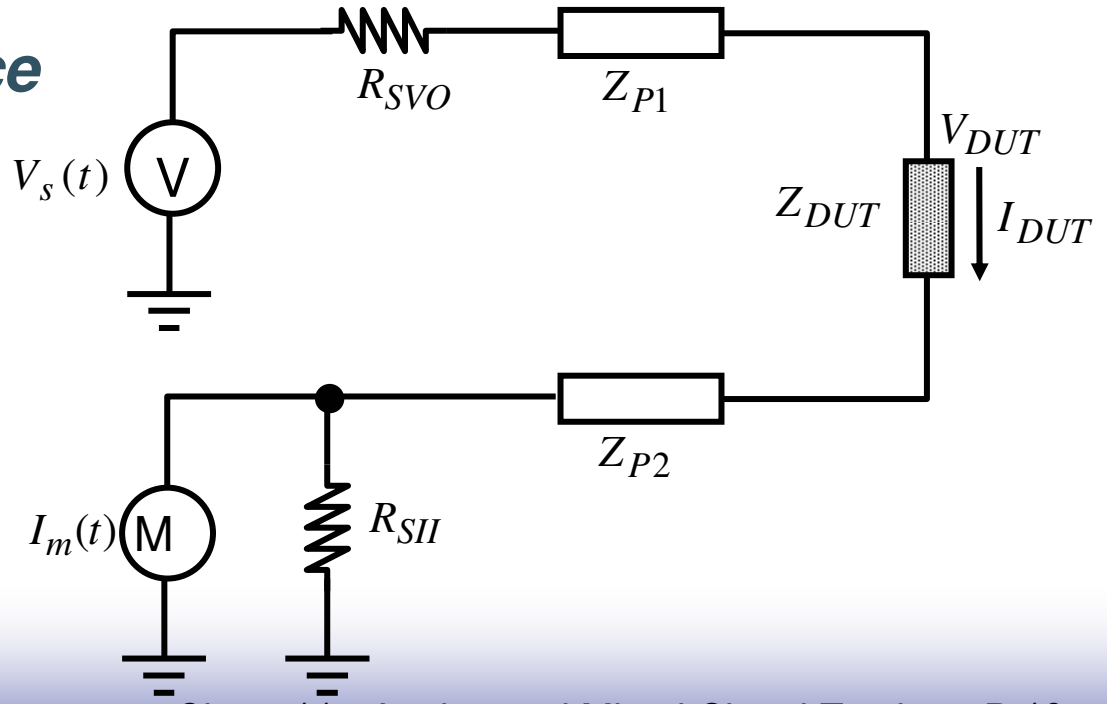
$$V_{DUT}(t) = V_s(t) \cdot \frac{Z_{DUT}}{R_{SVO} + Z_{P1} + Z_{DUT} + Z_{P2} + R_{SII}}$$

$$I_m(t) = \frac{V_s(t)}{R_{SVO} + Z_{P1} + Z_{DUT} + Z_{P2} + R_{SII}}$$

With Ideal Voltage Source and Current Meter

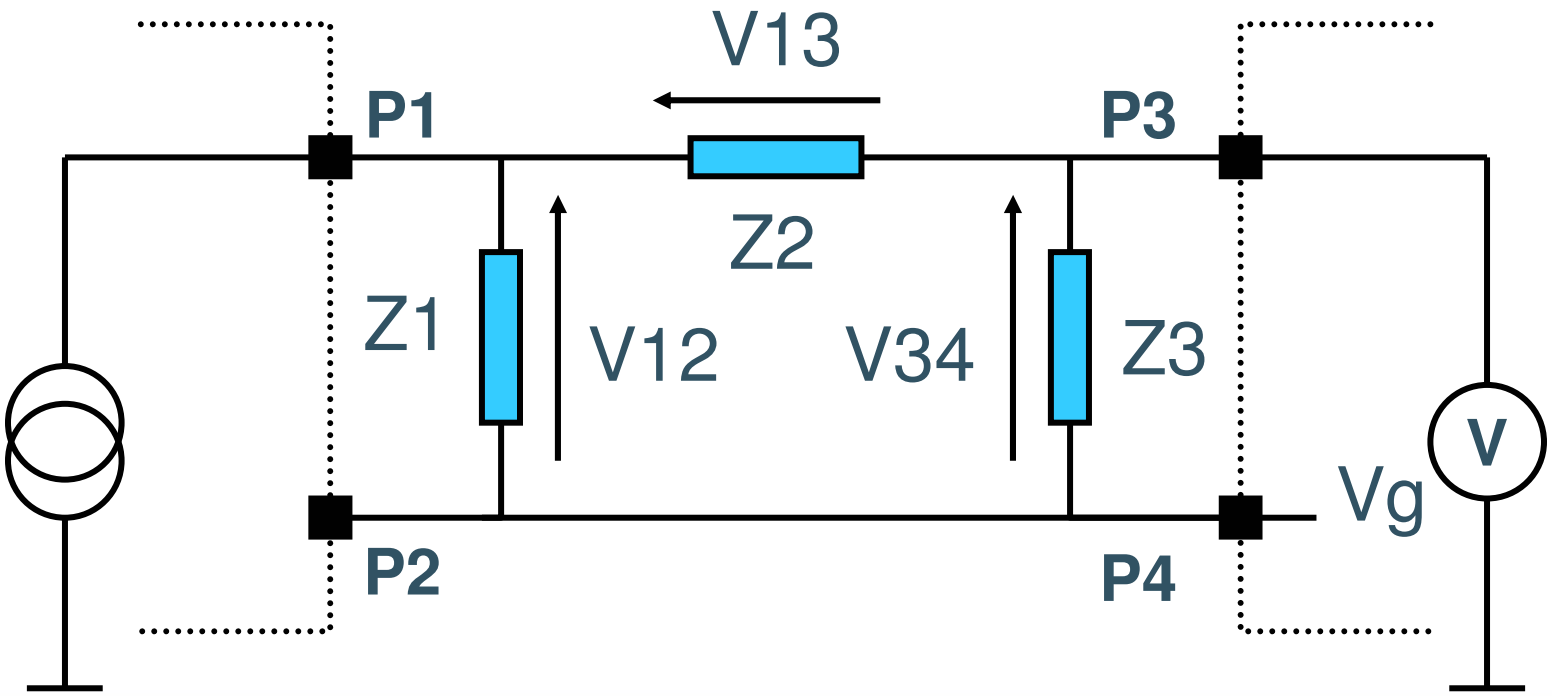
$$V_{DUT}(t) = V_s(t) \cdot \frac{Z_{DUT}}{Z_{P1} + Z_{DUT} + Z_{P2}}$$

$$I_m(t) = \frac{V_s(t)}{Z_{P1} + Z_{DUT} + Z_{P2}}$$

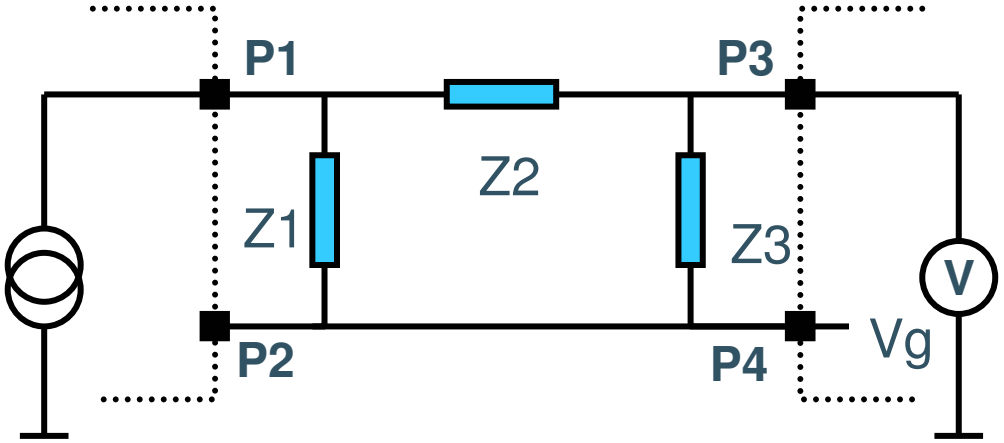


1149.4 – Extended Interconnect Test

- Measure complex interconnect network



1149.4 – Extended Interconnect Test



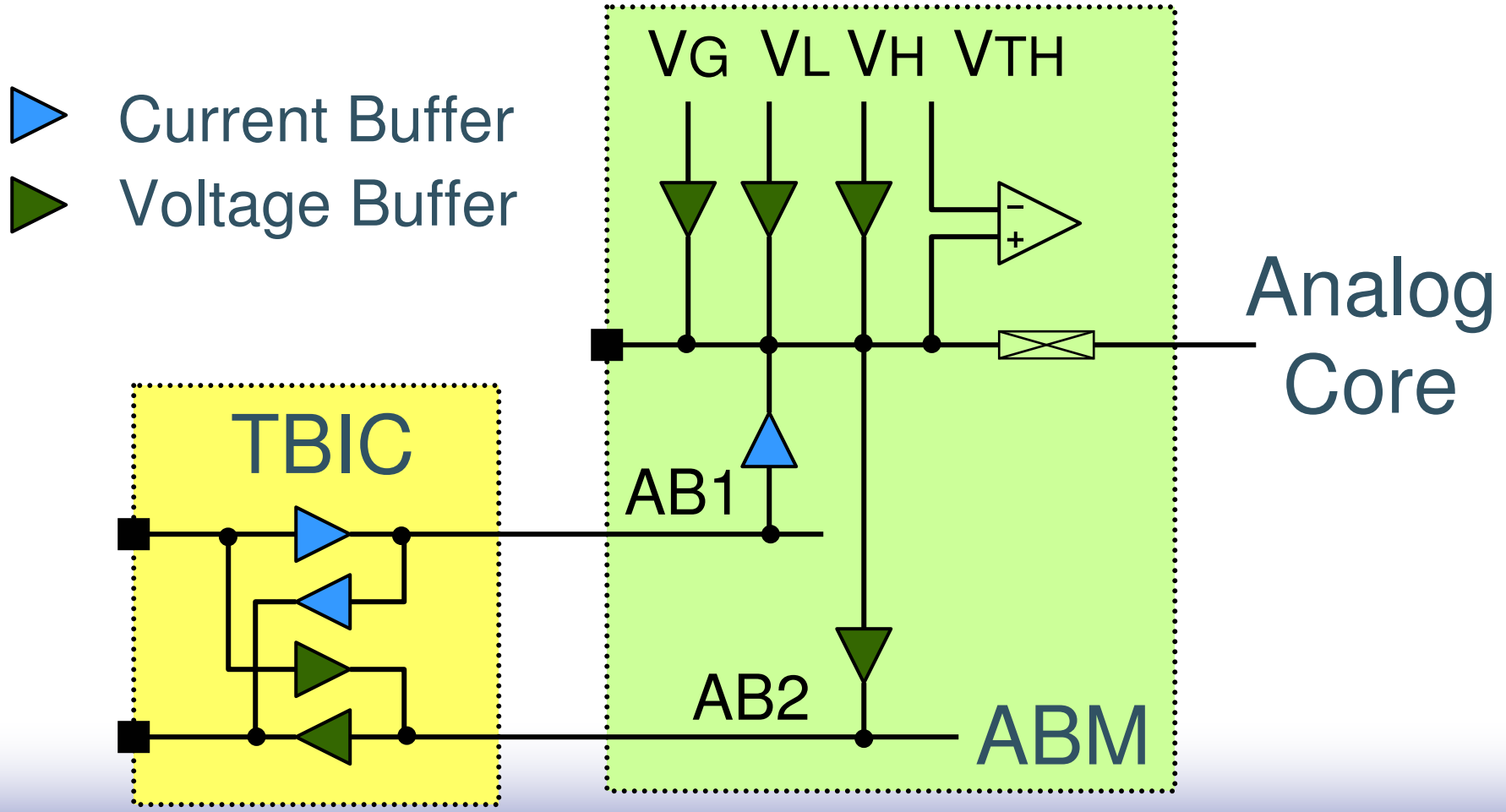
$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} \qquad h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$$

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} \qquad h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

H	P1	P2	P3	P4
h11	Is/Vm	GND	GND	GND
h12	Vm	GND	Vs	GND
h21	Is	GND	Im	GND
h22	Open	GND	Vs/Im	GND
Notations	Is: Apply Current		Vm: Measure Voltage	
	Vs: Apply Voltage		Im: Measure Current	

1149.4 - High Speed Applications

- Use buffers for better frequency response



11.5 Concluding Remarks

- AMS testing requires specialized approaches and experienced engineers because of the large varieties of signals, functions and circuits.
- DSP approaches are so pervasive that even basic analog test items can be accomplished.
- IEEE 1057 with formal terminologies and standardized test methods provides a solid theoretical background for ADC/DAC testing.
- IEEE 1149.4 is one solution to extending and incorporating the digital counterpart.