EnCore™ 400
Embedded Processor
Reference Manual

P/N 5001653A Revision B

Notice Page

NOTICE

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REVISION HISTORY

Revision	Reason for Change	Date
A	Initial Release	June/02
B	Updates/Changes	Oct/02

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Audience Assumptions

This reference manual is for the person who designs computer related equipment, including but not limited to hardware and software design and implementation of the same. Ampro Computers, Inc. assumes you are qualified in designing and implementing your hardware designs and its related software into your prototype computer equipment.

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Chapter 1 About this Manual

Purpose of this Manual

This manual is for designers of systems based on the EnCore™ 400 module. This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- EnCore 400 Specifications
- Environmental requirements
- Major integrated circuits and features implemented
- EnCore 400 connector/pin numbers and definition
- BIOS Setup information

Information not provided in this reference manual includes:

- Detailed Chip specification
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard buses and signals

Reference Material

The following list of reference materials may be helpful for you to complete your custom design successfully. Most of this reference material is also available on the Ampro web site in the Embedded Design Resource Center. The Embedded Design Resource Center was created for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience.

Specifications

- EnCore Architecture Specifications
- PCI 2.1 Compliant Specifications

For latest revision of the PCI specifications, contact the PCI Special Interest Group Office at:

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
800-433-5177 (U.S.)
503-797-4207 (International)

- EnCore EBX Baseboard Specification v 1.1
- EnCore EBX Baseboard Drawings

White Papers

- Reducing Time to Profit with High-Integration CPU Modules

Chip specifications used in the EnCore 400 module:

- STMicroelectronics' chip, STPC® Atlas, used for the embedded CPU.

  Web site: http:// us.st.com/stonline/products/support/stpc

- Standard Microsystems Corp's chip, FD37C669, used for the Super I/O controller.

  Web site: http:// www.smsc.com/main/catalog/fdc37c669.html

- Intel Corporation's chip, 82559ER, used for the Ethernet controller.

  Web site: http:// developer.intel.com/design/network/products/82559er.html

Related Ampro Products

The following items are directly related to successfully using the Ampro product you have just purchased or plan to purchase. Ampro highly recommends that you purchase and utilize an EnCore QuickStart Kit simultaneously with the design of your custom logic board.

EnCore 400 Support Products

- EnCore 400 QuickStart Kit (QSK)

  The QuickStart Kit includes the EnCore 400 module with 128MB of SODIMM SDRAM, the EnCore EBX Baseboard, and the EnCore Development Kit (EDK) CD-ROM. Included on the EDK CD-ROM are product manuals, reference items for the EBX baseboard, such as schematics and BOM, software development tools, board support packages (BSP) and utilities. .

- EnCore EBX baseboard

  The EnCore EBX baseboard, included with EnCore 400 QuickStart Kit, can be utilized as a substitute for your custom design. The Ampro baseboard provides a "gold board" to compare your custom design against as well as a convenient vehicle for development and test of application software.

  The EnCore EBX baseboard provides all the peripheral connections necessary to test and debug much of your software. All of the main I/O and peripheral device connections, including the keyboard, mouse, floppy drive, IDE hard drive, IDE CD-ROM, parallel port, serial ports, audio connections, and a standard ATX power supply connection are provided on the EnCore EBX baseboard.

- EnCore Development Kit

  This is the basic support package provided with the EnCore 400 module. The CD-ROM includes all of the documentation in PDF format, including this reference manual, the EnCore 400 QuickStart Guide, and the EnCore EBX Baseboard Reference Manual. This CD-ROM also provides reference material for the EnCore EBX Baseboard, such as OrCad schematics and Allegro layout files, a bill of materials (BOM), and an Approved Vendor List (AVL).

Other Ampro EnCore Products

- EnCore™ M3 – This embedded processor module is a low-power, high-performance, high-integration MIPS32™-compatible module using a 400MHz AMD Alchemy Au1500™ processor rated at 480 Dhrystone MIPS. The typical power consumption of an EnCore M3 module is less than 2.5 watts. In addition to the standard EnCore features, the EnCore M3 includes a second 10/100BaseT Ethernet port and a third serial port for debugging purposes.

- EnCore™ PP1 – This embedded processor module is a low-power, high-performance module using a PowerPC™ based processor from Motorola. The typical power consumption of an EnCore PP1 module is less than 4.0 watts at 300MHz. In addition to the standard EnCore features, the EnCore PP1 drives the PCI Bus at 33 or 66MHz.

- EnCore™ 500 – This embedded processor module uses a 266MHz Mobile Pentium processor for its computing functions. In addition to the standard EnCore features, the EnCore 500 includes a high performance 3D graphics controller for CRTs and popular LCD panels.

- EnCore™ 700 – This embedded processor module is the highest performance EnCore product offering a high performance 850MHz Pentium® III processor and incorporates the Intel 815em chipset. In addition to the standard EnCore features, the EnCore 700 includes a 2D/3D graphics controller, which provides both CRT and TFT flat panel video interfaces.

Other Ampro Products

- Little Board™ Family – These highly integrated single-board computers using the EBX form factor (5.75x8.00 inches), are available with 486, Mobile Pentium and Pentium II processors. The Little Board single-board computers offer functions equivalent to a complete laptop or desktop PC system, plus several expansion cards. Built-in extras to meet the critical requirements of embedded applications include onboard solid state disk compatibility, watchdog timer, smart power monitor, and other embedded-PC BIOS enhancements.

- CoreModule™ Family – These complete embedded-PC subsystems on single PC/104 or PC/104-Plus form-factor (3.6x3.8 inches) modules feature 386SX, 486DX, and Mobile Pentium CPUs. Each CoreModule includes a full complement of PC core logic functions, plus disk controllers, and serial and parallel ports. Some modules include CRT and flat panel graphics controllers or an Ethernet interface. The CoreModules also come with built-in extras to meet the critical reliability requirements of embedded applications. These include onboard solid state disk compatibility, watchdog timer, smart power monitor, and other embedded-PC BIOS enhancements.

- MiniModule™ Family – This extensive line of peripheral interface modules compliant with PC/104 and PC/104-Plus can be used with Ampro CoreModule and Little Board single-board computers to configure embedded system solutions. Ampro's highly reliable MiniModule products currently support CRT and flat-panel display interfacing, networking, and PC Card expansion.

Chapter 2 Product Overview

This introduction presents general information about the EnCore concept and the EnCore 400 Embedded Processor module. After reading this chapter you should understand:

- EnCore Concept
- Developmental strategies using the EnCore 400 Embedded Processor
- EnCore 400 architecture
- EnCore 400 module features
- Major components
- Connectors
- Specifications

EnCore Concept

Embedded CPU technology is undergoing a period of rapid change. Many next-generation system designs require increased performance, low power consumption, heat dissipation, and Internet ready connectivity. CPU choices have grown from a simple choice between Intel and Motorola architectures to include a wide variety of new low power RISC processors.

During this period of rapid change, designers of embedded systems face increasing pressures to bring products to market quickly. Many products that once incorporated a custom CPU design can no longer afford the time to develop and debug a custom CPU let alone port operating system software to it. Furthermore, CPU subsystem design usually plays a small part in providing any uniqueness to an embedded product. The remainder of the embedded product design adds key logic elements that provide a unique product and differentiate it from other products serving the same market. The challenge is to speed these designs to market by eliminating the need for a custom CPU design while providing the flexibility to include all critical elements, which make the embedded product unique.

EnCore modules provide a standard, off-the-shelf CPU subsystem that can be included in virtually any product. EnCore modules work like a high integration chip, plugging into your circuit board to provide the custom logic for your application. EnCore provides a simple, industry standard interface that is independent of CPU type. The EnCore interface includes the industry-standard PCI bus, I/O signals from the peripheral components on the EnCore module, power, and ground. The EnCore modules support Intel architecture (x86), MIPS and PowerPC processors, and other RISC processors. Go to the Ampro web site (www.ampro.com) for the latest processor support information.

This standard EnCore interface lets you try different processors and different processor types in your actual product environment with the ability to defer a processor choice until late in the project if you choose. The interface also lets you easily offer different versions of your product with different capabilities by either selecting different EnCore modules with the same baseboard, or by designing different baseboards for the same CPU. This same capability leads to simpler ability to upgrade by either selecting a more powerful CPU (without baseboard redesign) or enhancing the baseboard without touching the CPU subsystem or the bulk of the applications software.

EnCore's flexibility enables designers to take an accelerated, low risk path with EnCore-based designs. Unlike chip based designs, the approach with EnCore allows design to begin independent of a processor decision. Your custom logic board design can begin, and be completed without identifying which processor is to be used in your application. The system can be prototyped with any available EnCore module. Your design flow diagram might look similar to the one shown in Figure 2-1.

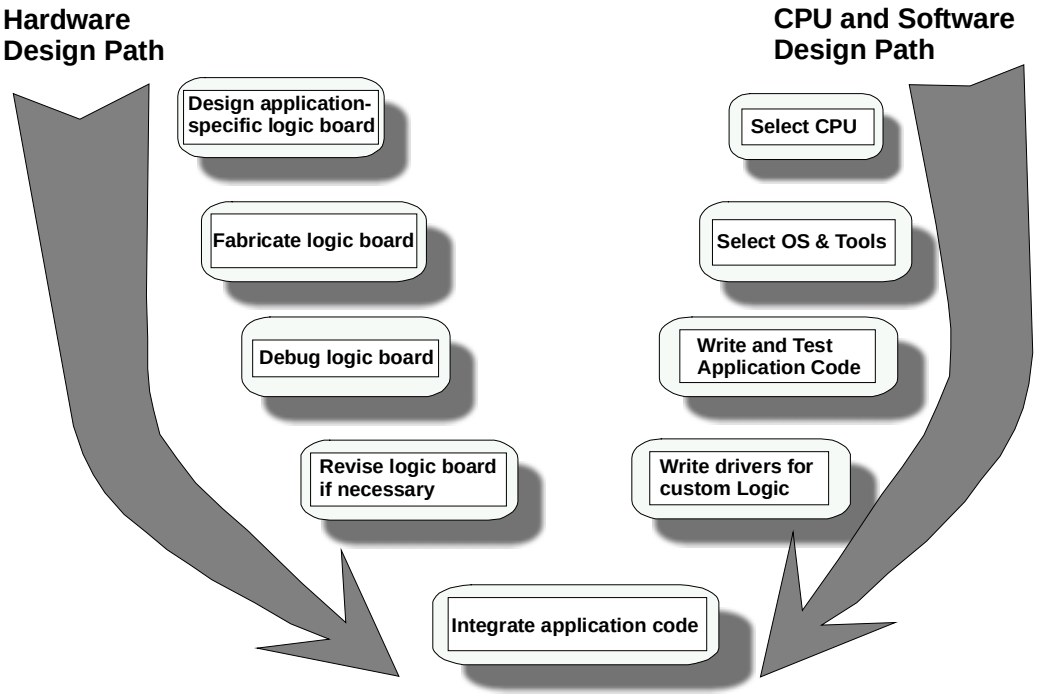

Figure 2-1. Typical Design Flow

Product Description

The EnCore 400 module is one in a series of modules based on Ampro's EnCore platform. This platform was created to provide the efficient delivery of high performance CPU technology while reducing time-to-market for OEM embedded applications. Based on the STPC® Atlas processor-on-a-chip, the EnCore 400 module provides the functionality of a complete computer in the 100x145mm (3.94x5.71 inch) form factor.

The EnCore 400 module includes high performance 2D graphics for CRTs and the most popular TFT flat panels, and a 10/100BaseT Ethernet interface. It supports up to 128MB SDRAM in the Small Outline (SO) DIMM package, a floppy drive or ECP/EPP parallel port, USB ports, Infrared port, two serial ports, primary IDE controller, and PCI expansion bus.

Like all modules in the EnCore series, the EnCore 400 module is designed to interface with a host baseboard that provides application-specific logic, I/O connections, and DC power. All EnCore modules interface to the baseboard via the industry-standard PCI bus and a set of I/O signals. The small form-factor of an EnCore module gives OEM designers a great deal of flexibility in baseboard design.

EnCore modules enhance time to market for systems that seek to combine a standard 32- or 64-bit processor subsystem with applications specific logic on a custom baseboard. To speed baseboard design, Ampro offers a sample baseboard to OEM customers as a reference design for development of their own system boards. The EnCore 400 module is compatible with PC hardware and software standards assuring seamless integration with a wide range of off-the-shelf operating systems, application software and peripheral devices.

Module Features

- x86 Processor Core
  - Supports processor core speed up to 133MHz
  - Supports external memory up to 128MB
  - 8kB Unified Instruction and Data Cache
  - Parallel Processing Integral Floating Point Unit
  - Low Power and System Management Modes
- Memory
  - 64-Bit Data Bus
  - 100MHz Clock Speed (Maximum)
  - Supports 3.3V SDRAM
  - Supports 16MB–128MB System Memory
  - 144-Pin Standard Small Outline (SO) DIMM Socket
  - 256kB Flash Memory on module
- PCI Bus
  - PCI 2.1 Compliant Devices (32-bit bus)
  - Supports up to four PCI devices on the baseboard
  - Two PCI Master on the baseboard
  - 32-Bit PCI Master And Target Operations
- Input/Output Interfaces
  - Ultra DMA IDE Interface
    - Single Bus Master, Two EIDE Devices
    - Supports ATAPI and Tape Peripherals
    - Supports 40-pin IDE interface
  - Utility Interface
    - USB – Two root USB hubs with four functional USB ports
    - Two Serial Ports
    - One ECP/EPP Parallel Port Floppy Drive Interface /
    - Keyboard and PS/2 Mouse Interface
    - One dedicated two-way Infrared (IrDA) Port Interface
    - Integrated Peripheral Controllers
      - 2X8237/AT compatible DMA controller
      - 2X8259/AT compatible Interrupt controllers
- Ethernet
  - Intel GD82559ER Fast Ethernet PCI Controller
  - IEEE 802.3 10BaseT/100BaseTX compatible physical layer

- LCD/CRT Interface

  CRT

  - Graphics Enhanced 2D Accelerator
  - 64-bit wide Pipelined Architecture @100MHz
  - VGA Controller with 135MHz triple RAMDACs for 1280 x 1024 x 75Hz display
  - Supports 24-bit pixel depth
  - Interlaced or non-interlaced output

  LCD/TFT

  - TFT Display Controller
  - Supports PanelLink™ high speed serial transmitter on the baseboard for high resolution panel interface
  - Supports VGA, SVGA, XGA, SXGA active matrix TFT flat panels
  - Supports programmable panel size up to 1024 x 1024 pixels
  - Supports programmable control for:
    - Image positioning
    - Blank space insertions in text mode
    - Horizontal and vertical image expansion in graphic mode
    - Two Pulse Width Modulator (PWM) signals for brightness and contrast
- Miscellaneous
  - Real Time Clock with On Board Battery
  - WatchDog timer
  - Battery-Free Boot Capability
- Power Requirements
  - 3.3V @ 0.5 Amps
  - 5.0V @ 1.5 Amps

Block Diagram

The functional block diagram of the EnCore 400 module is shown below, in Figure 2-1.

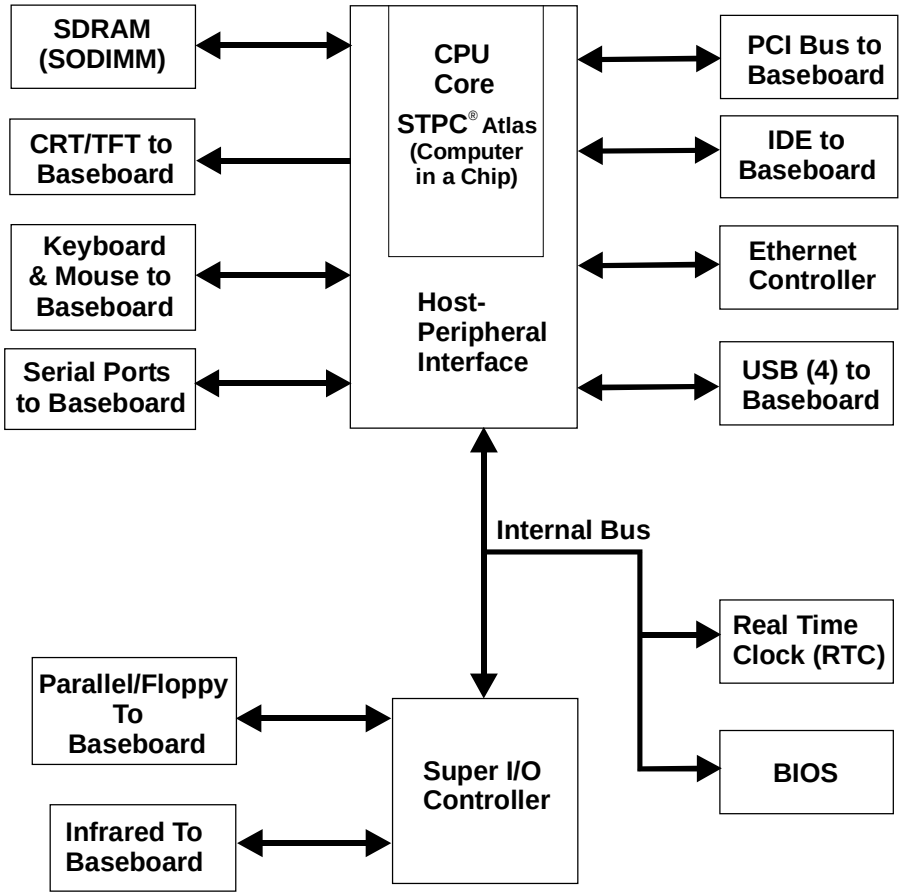

Figure 2-2. EnCore 400 Block Diagram

Major Integrated Circuits

Table 2-1 lists and describes the major ICs and Figure 2-2 indicates the location of the components.

Table 2-1. Major Integrated Circuit Descriptions

Manufacture	Model	Description	Features
STMicroelectronics	STPC® Atlas	Embedded CPU (U3) – The combination of features in the CPU include a graphics controller, PCI controller, EIDE controller, and I/O features.	CPU cpre Graphics controller PCI controller EIDE Controller I/O features
Standard Microsystems Corp.	FD37C669	Super I/O (U15) – This chip provides the Floppy controller, Parallel controller, and the Infrared controller.	Floppy controller Parallel controller IrDA controller
Intel	82559ER	Ethernet (U8) – This chip provides the 10BaseT/100BaseT internet controller.	Ethernet

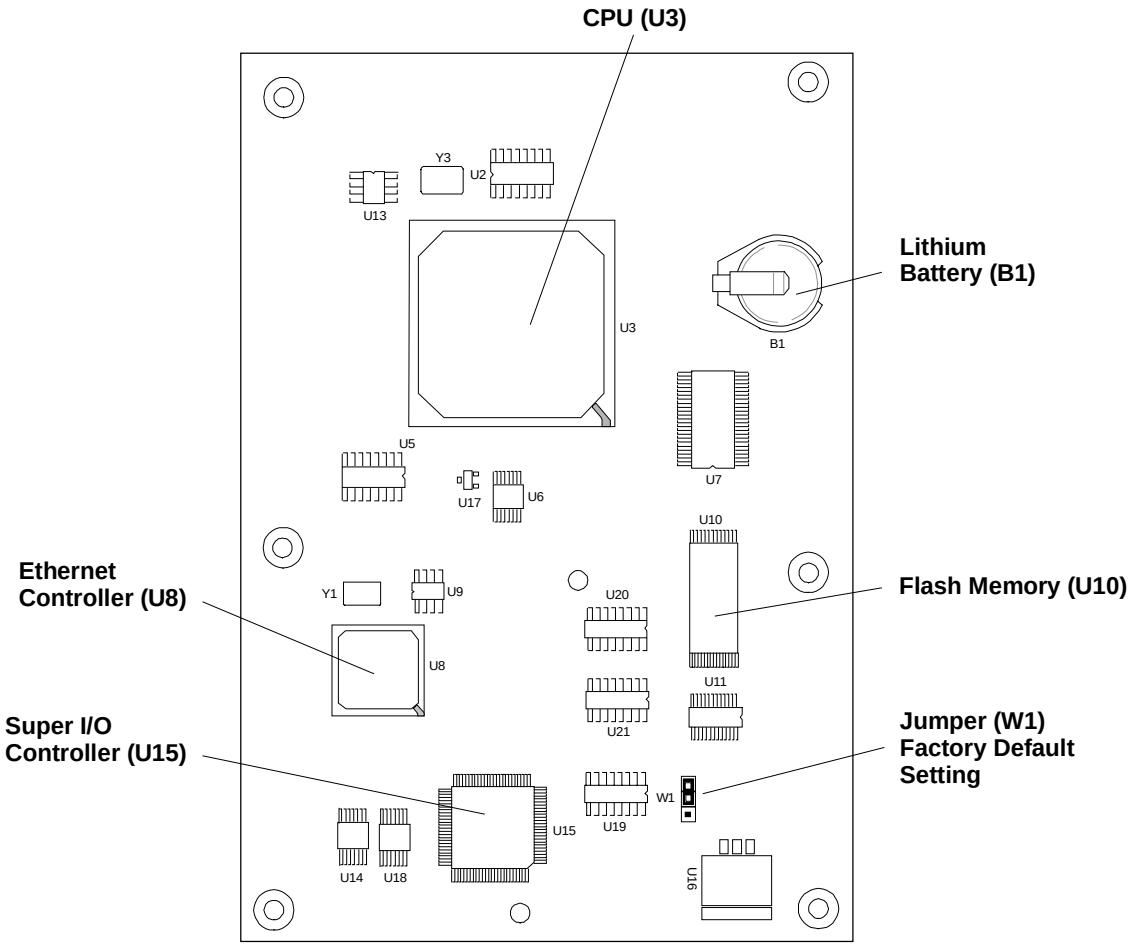

Figure 2-3. Major Component Locations (top view)

Specifications

Physical Specifications

Table 2-2 gives the physical dimensions of the module.

Table 2-2. Weight and Footprint Dimensions

Weight	0.136kg (0.3lbs.)
Height (overall above baseboard)	38.1mm (1.5in.)
Width	100mm (3.94in.)
Length	145mm (5.71in.)

Mechanical Specifications

Figure 2-4 illustrates the "see-through" view of the EnCore 400 module's bottom connectors with dimensions. Figure 2-5 illustrates the normal bottom view of the EnCore 400 module.

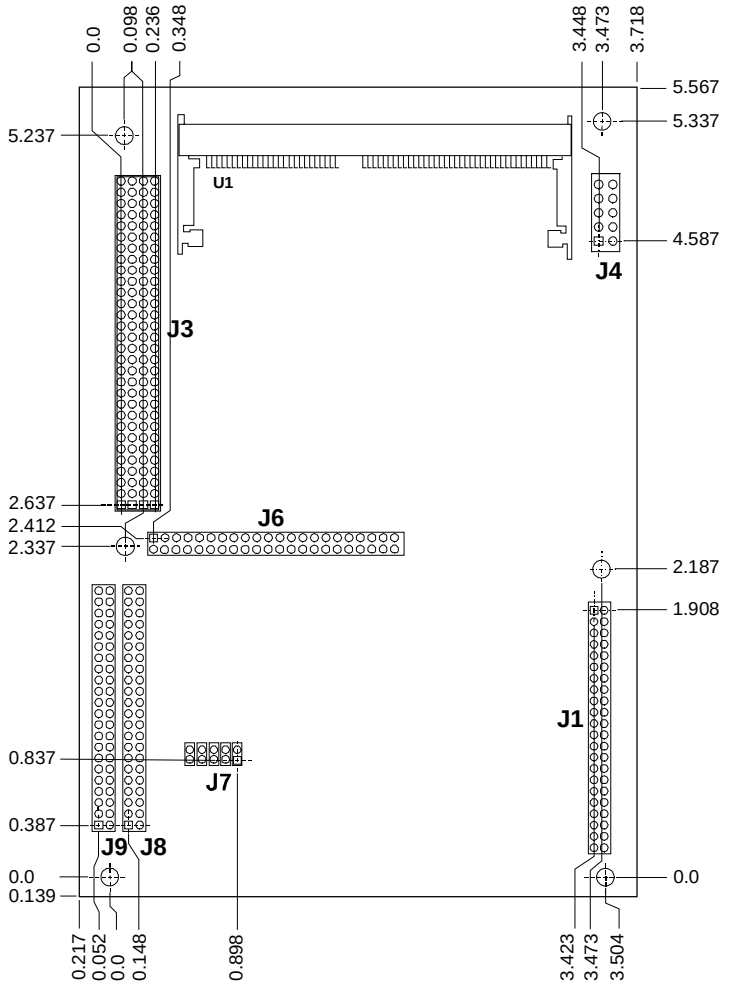

Figure 2-4. Mechanical Layout of Module (through board view)

NOTE	All dimensions are given in inches.

Table 2-3. Connector Definition/Table

Jack # – Identity	Board Access	Description
J1 – IDE	Bottom	A 44-pin connector used for the IDE interface.
J3 – PCI Bus	Bottom	A 120-pin connector used for the PCI interface.
J4 – Power	Bottom	A 10-pin connector used for the Power interface.
J6 – LCD/CRT	Bottom	A 44-pin connector used for the LCD/CRT interface.
J7 – Ethernet	Bottom	A 10-pin connector used for the Ethernet interface.
J8 – Floppy/Parallel/ Serial	Bottom	A 44-pin connector used for the Floppy/Parallel/Serial interface.
J9 – Utility	Bottom	A 44 pin connector used for the Utility interface.

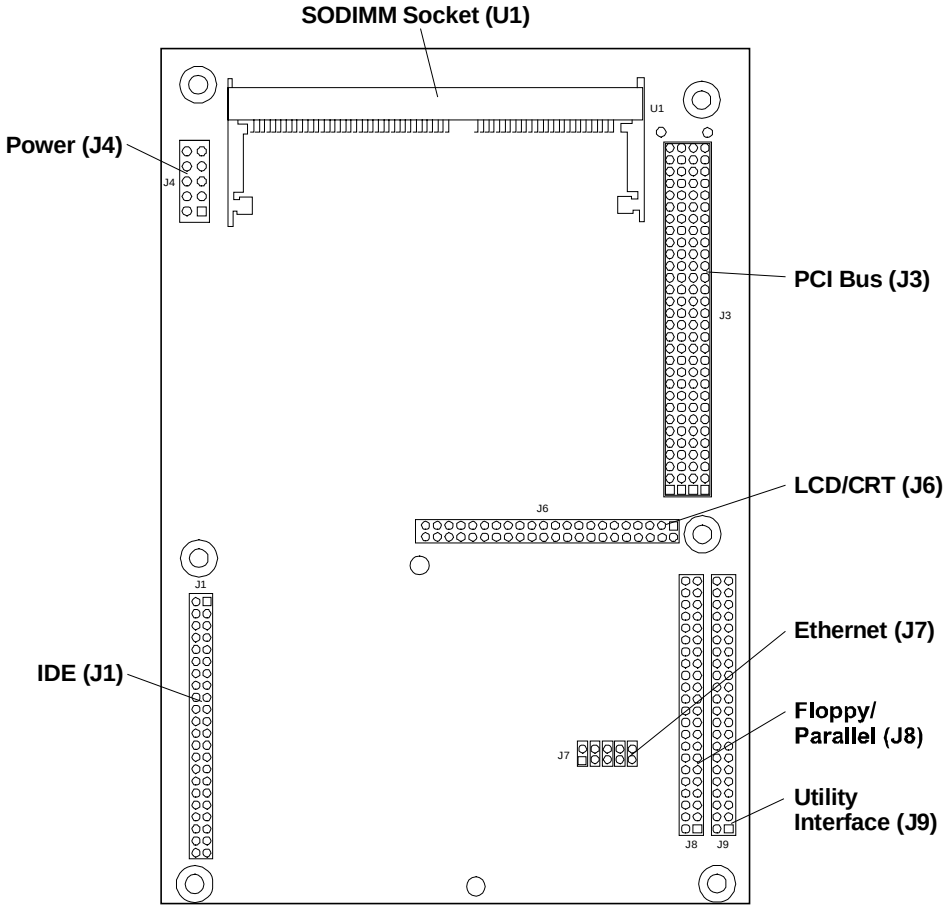

Figure 2-5. Connector Locations (bottom view)

Power Specifications

Table 2-4. Power Supply Requirements

Parameter	Characteristics
Input Type	Regulated DC voltages
Inputs Voltages	+3.3 Volts DC +/- 5 % @ 0.5 Amps
	+5 Volts DC +/- 5 % @ 1.5 Amps
Operating Power	9 Watts

Environmental Specifications

Table 2-5. Environmental Limitations

Parameter	Conditions
Temperature	
Operating	0° to +70° C (32° to 158° F)
Extended (Optional)	Contact the Factory
Non-operating	-55° to +85° C (-67° to +185° F)
Humidity	
Operating	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU, the I/O chip, and the voltage regulator draw most of the power and generate most of the heat. However, a CPU heatsink is not required at the slower CPU speeds, but may be needed at the higher CPU speeds, depending on your EnCore 400 module's application. A CPU heatsink is provided in the ship kit, if not installed on the CPU.

Chapter 3 Hardware

Overview

This chapter is divided into the following chapter headings with descriptions, and tables where appropriate.

- CPU
- Memory
- PCI Bus Interface (J3)
- IDE Interface (J1)
- Floppy/Parallel/Serial Interface (J8)
- Utility Interface (J9)
  - USB (Universal Serial Bus)
  - Keyboard
  - PS/2 Mouse Controller
  - Infrared Port (IrDA)
- Ethernet Interface (J7)
- LCD/CRT Graphics Interface (J6)
- Miscellaneous
  - Real Time Clock (RTC)
  - WatchDog Timer
- Power Supply Interface (J4)

NOTE	The EnCore 400 module uses a variety of chips to provide all of the features listed in this manual. However, not all the features available for each chip in the set have been implemented.

CPU

The EnCore 400 uses an embedded microprocessor that combines a powerful x86 core and a selection of peripheral interfaces into one chip. The STPC®Atlas integrates a standard 5th generation x86 core along with a powerful UMA graphics/video chipset. It supports logic including PCI, USB, UIDE controllers and combines them with standard I/O interfaces to provide a single PC compatible subsystem in a single chip, suitable for various kinds of embedded applications.

Memory

The EnCore 400 contains one standard 64-bit Small Outline (SO) DIMM socket (144-pin) and supports a 64-bit wide data path. Synchronous DRAM modules are supported with configurations from 16MB to 128MB. Ampro supplies fully qualified and tested memory, which is compatible with the EnCore 400.

Should the user wish to provide his own memory, these SODIMMs are commercially available, but use the PC100 (100MHz or faster), 3.3V, 8ns, SDRAM 144-pin SODIMMs.

Memory Map

The following table provides the common PC/AT memory allocations. Memory below 000500h is used by the CPU and BIOS.

Table 3-1. Memory Map List

Base Address			Function
00000000h	-	0009FFFFh	Conventional Memory
000A0000h	-	000AFFFFh	Graphics Memory
000B0000h	-	000B7FFFh	Mono Text Memory
000B8000h	-	000BFFFFh	Color Text Memory
000C0000h	-	000C7FFFh	Standard Video BIOS
000C8000h	-	000DFFFFh	PCI Peripheral BIOS Area
000E0000h	-	000FFFFFh	System BIOS Area
00100000h	-	08000000h	Extended Memory
FFFC0000h	-	FFFFFFFFh	System Flash

Table 3-2. I/O Memory Map List

Base Address			Function
0000h	–	000Fh	DMA Controller 1 (8237)
0020h	–	0021h	Interrupt Controller 1 (8259)
0022h	–	0023h	EnCore Specific Registers (STPC)
0040h	–	0043h	Timer (8254)
0060h	–		Keyboard Controller DATA
0061h	–		AT Port B
0064h	–		Keyboard Controller Command/Status
0070h	–	0071h	RTC Index/Data
0080h	–	008Fh	DMA Page Registers
0094h	–		VGA mother board enable register
00A0h	–	00A1h	Interrupt Controller 2 (8259)
00C0h	–	00dfh	DMA controller 2 (8257)
0102h	–		VGA setup register
370h	–	371h	Super I/O Config
3B4h,3B5h,3BAh, 3D4h,3D5h,3DAh	–		VGA Registers
3C0h	–	3CFh	VGA Registers
3F0h	–	3F1h	STPC LPT config
0CF8h	–		PCI configuration address register
0CFCh	–	0CFFh	PCI configuration data register
46E8h	–		VGA add-in mode enable register

PCI Bus Interface (J3)

The PCI Bus uses a 120-pin (30x4) 2mm header interface. This interface header will carry all of the appropriate PCI signals operating at clock speeds up to 33MHz. The interface header is located on the bottom of the board. The module has been designed to accommodate four PCI devices on the baseboard design.

NOTE There are four groups of signals and each group has its own clock signal. The four PCI clock signals have staggered trace lengths, where PCI Clk3 is the shortest, while PCI Clk0 is the longest. Each Clock line has an additional trace length of 650 mils.

Table 3-3. PCI Bus Interface Pin/Signal Descriptions (J3)

Pin #	Signal	Input/ Output	Description
1 (A1)	Reserved (Key)		Reserved
2 (A2)	VI/O		+5 volts ±5% power supply
3 (A3)	AD05	T/S	PCI Address and Data Bus Line 5 – There are 32 signal lines (address and data) and the signals on these lines are multiplexed. A bus transaction consists of an address followed by one or more data cycles.
4 (A4)	C/BE0*	T/S	PCI Bus Command/Byte Enable 0 – This signal line is one of four signal lines. These signal lines are multiplexed, so that during the address cycle, the command is defined and during the data cycle, the byte enable is defined.
5 (A5)	GND		Digital Ground
6 (A6)	AD11	T/S	PCI Address and Data Bus Line 11 – Refer to Pin 3 for more information.
7 (A7)	AD14	T/S	PCI Address and Data Bus Line 14 – Refer to Pin 3 for more information.
8 (A8)	+3.3V		+3.3 volts ±5% power supply
9 (A9)	SERR*	O/D	System Error – This signal is for reporting address parity errors.
10 (A10)	GND		Digital Ground
11 (A11)	STOP*	S/T/S	Stop – This signal indicates the current selected device is requesting the master to stop the current transaction
12 (A12)	+3.3V		+3.3 volts ±5% power supply
13 (A13)	FRAME*	S/T/S	PCI bus Frame access – This signal is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle
14 (A14)	GND		Digital Ground
15 (A15)	AD18	T/S	PCI Address and Data Bus Line 18 – Refer to Pin 3 for more information.
16 (A16)	AD21	T/S	PCI Address and Data Bus Line 21 – Refer to Pin 3 for more information.
17 (A17)	+3.3V		+3.3 volts ±5% power supply
18 (A18)	IDSEL0	In	Initialization Device Select 0 – This signal line is one of four signal lines. These signals are used as the chip-select signals during configuration
19 (A19)	AD24	T/S	PCI Address and Data Bus Line 24 – Refer to Pin 3 for more information.
20 (A20)	GND		Digital Ground
21 (A21)	AD29	T/S	PCI Address and Data Bus Line 29 – Refer to Pin 3 for more information.
22 (A22)	+5V		+5 volts ±5% power supply
23 (A23)	REQ0*	T/S	Bus Request 0 – This signal line is one of three signal lines. These signals indicate the device desires use of the bus to the arbitrator.
24 (A24)	GND		Digital Ground
25 (A25)	GNT1*	T/S	Grant 1 – This signal line is one of three signal lines. These signal lines indicate access has been granted to the requesting device (PCI Masters).
26 (A26)	+5V		+5 volts ±5% power supply

Pin #	Signal	Input/ Output	Description
27 (A27)	CLK2	In	PCI clock 2 – This signal line is one of four signal lines. These clock signals provide the timing outputs for four external PCI devices and the timing for all transactions on the PCI bus
28 (A28)	GND		Digital Ground
29 (A29)	+12V		+12 volts ±5% power supply
30 (A30)	NC		Not connected - Reserved
31 (B1)	NC		Not connected - Reserved
32 (B2)	AD02	T/S	PCI Address and Data Bus Line 2 – Refer to Pin 3 for more information.
33 (B3)	GND		Digital Ground
34 (B4)	AD07	T/S	PCI Address and Data Bus Line 7 – Refer to Pin 3 for more information.
35 (B5)	AD09	T/S	PCI Address and Data Bus Line 9 – Refer to Pin 3 for more information.
36 (B6)	VI/O		+5 volts ±5% power supply
37 (B7)	AD13	T/S	PCI Address and Data Bus Lines 13 – Refer to Pin 3 for more information.
38 (B8)	C/BE1*	T/S	PCI Bus Command/Byte Enable 1 – Refer to Pin 4 for more information.
39 (B9)	GND		Digital Ground
40 (B10)	PERR*		Parity Error – This signal is for reporting data parity errors.
41 (B11)	+3.3V		+3.3 volts ±5% power supply
42 (B12)	TRDY*	S/T/S	Target Ready – This signal indicates the selected device's ability to complete the current cycle of transaction. Both IRDY* and TRDY* must be asserted to terminate a data cycle
43 (B13)	GND		Digital Ground
44 (B14)	AD16	T/S	PCI Address and Data Bus Line 16 – Refer to Pin 3 for more information.
45 (B15)	+3.3V		+3.3 volts ±5% power supply
46 (B16)	AD20	T/S	PCI Address and Data Bus Lines 20 – Refer to Pin 3 for more information.
47 (B17)	AD23	T/S	PCI Address and Data Bus Line 23 – Refer to Pin 3 for more information.
48 (B18)	GND		Digital Ground
49 (B19)	C/BE3*	T/S	PCI Bus Command/Byte Enable 3 – Refer to Pin 4 for more information.
50 (B20)	AD26	T/S	PCI Address and Data Bus Line 26 – Refer to Pin 3 for more information.
51 (B21)	+5V		+5 volts ±5% power supply
52 (B22)	AD30	T/S	PCI Address and Data Bus Line 30 – Refer to Pin 3 for more information.
53 (B23)	GND		Digital Ground
54 (B24)	REQ2*	T/S	Bus Request – Not supported
55 (B25)	VI/O		+5 volts ±5% power supply
56 (B26)	CLK0	In	PCI clock 0 – Refer to Pin 27 for more information
57 (B27)	+5V		+5 volts ±5% power supply
58 (B28)	INTD*	O/D	Interrupt D – This signal is used to request interrupts only for multi-function devices.
59 (B29)	INTA*	O/D	Interrupt A – This signal is used to request an interrupt.
60 (B30)	NC		Not connected - Reserved
61 (C1)	+5		+5 volts ±5% power supply
62 (C2)	AD01	T/S	PCI Address and Data Bus Line 1 – Refer to Pin 3 for more information.
63 (C3)	AD04	T/S	PCI Address and Data Bus Lines 4 – Refer to Pin 3 for more information.
64 (C4)	GND		Digital Ground
65 (C5)	AD08	T/S	PCI Address and Data Bus Line 8 – Refer to Pin 3 for more information.
66 (C6)	AD10	T/S	PCI Address and Data Bus Line 10 – Refer to Pin 3 for more information.

Pin #	Signal	Input/ Output	Description
67 (C7)	GND		Digital Ground
68 (C8)	AD15	T/S	PCI Address and Data Bus Line 15 – Refer to Pin 3 for more information.
69 (C9)	SB0*		Snoop Backoff
70 (C10)	+3.3V		+3.3 volts ±5% power supply
71 (C11)	LOCK*	S/T/S	Lock – This signal indicates an operation that may require multiple transactions to complete
72 (C12)	GND		Digital Ground
73 (C13)	IRDY*	S/T/S	Initiator Ready – This signal indicates the master's ability to complete the current data cycle of the transaction
74 (C14)	+3.3V		+3.3 volts ±5% power supply
75 (C15)	AD17	T/S	PCI Address and Data Bus Line 17 – Refer to Pin 3 for more information.
76 (C16)	GND		Digital Ground
77 (C17)	AD22	T/S	PCI Address and Data Bus Line 22 – Refer to Pin 3 for more information.
78 (C18)	IDSEL1		Initialization Device Select 1 – Refer to Pin 18 for more information
79 (C19)	VI/O		+5 volts ±5% power supply
80 (C20)	AD25	T/S	PCI Address and Data Bus Line 25 – Refer to Pin 3 for more information.
81 (C21)	AD28	T/S	PCI Address and Data Bus Line 28 – Refer to Pin 3 for more information.
82 (C22)	GND		Digital Ground
83 (C23)	REQ1*	T/S	Bus Request 1 – Not supported
84 (C24)	+5V		+5 volts ±5% power supply
85 (C25)	GNT2*	T/S	Grant 2 – Refer to Pin 25 for more information
86 (C26)	GND		Digital Ground
87 (C27)	CLK3	In	PCI clock 3 – Refer to Pin 27 for more information
88 (C28)	+5V		+5 volts ±5% power supply
89 (C29)	INTB*	O/D	Interrupt B – This signal is used to request interrupts only for multi-function devices.
90 (C30)	PME*		Power Management Event – This signal is used for power management events.
91 (D1)	AD00	T/S	PCI Address and Data Bus Line 0 – Refer to Pin 3 for more information.
92 (D2)	+5V		+5 volts ±5% power supply
93 (D3)	AD03	T/S	PCI Address and Data Bus Lines 3 – Refer to Pin 3 for more information.
94 (D4)	AD06	T/S	PCI Address and Data Bus Lines 6 – Refer to Pin 3 for more information.
95 (D5)	GND		Digital Ground
96 (D6)	GND		Digital Ground
97 (D7)	AD12	T/S	PCI Address and Data Bus Line 12 – Refer to Pin 3 for more information.
98 (D8)	+3.3V		+3.3 volts ±5% power supply
99 (D9)	PAR	T/S	PCI bus Parity bit – This signal is the even parity bit on AD[31:0] and C/BE[3:0]*
100 (D10)	SDONE		Snoop Done
101 (D11)	GND		Digital Ground
102 (D12)	DEVSEL*	S/T/S	Device Select – This signal is driven by the target device when its address is decoded.
103 (D13)	+3.3V		+3.3 volts ±5% power supply
104 (D14)	C/BE2*		PCI Bus Command/Byte Enable 2 – Refer to Pin 4 for more information.
105 (D15)	GND		Digital Ground
106 (D16)	AD19	T/S	PCI Address and Data Bus Line 19 – Refer to Pin 3 for more information.

Pin #	Signal	Input/ Output	Description
107 (D17)	+3.3V		+3.3 volts ±5% power supply
108 (D18)	IDSEL2		Initialization Device Select 2 – Refer to Pin 18 for more information.
109 (D19)	IDSEL3		Initialization Device Select 3 – Refer to Pin 18 for more information.
110 (D20)	GND		Digital Ground
111 (D21)	AD27	T/S	PCI Address and Data Bus Line 27 – Refer to Pin 3 for more information.
112 (D22)	AD31	T/S	PCI Address and Data Bus Line 31 – Refer to Pin 3 for more information.
113 (D23)	VI/O		+5 volts ±5% power supply
114 (D24)	GNT0*	T/S	Grant 0 – Refer to Pin 25 for more information.
115 (D25)	GND		Digital Ground
116 (D26)	CLK1	In	PCI clock 1 – Refer to Pin 27 for more information
117 (D27)	GND		Digital Ground
118 (D28)	RST*	In	PCI bus reset – This signal is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset
119 (D29)	INTC*	O/D	Interrupt C – This signal is used to request interrupts only for multi-function devices.
120 (D30)	GND		Digital Ground

Notes: The shaded area denotes power or ground. The signals marked with * indicate signal inversion.

The Input/Output signals in this table refer to the input/output signals listed in the *PCI Local Bus Manual*, Revision 2.1, Chapter 2, paragraph 2.1, Signal definitions. The following acronyms are used in this table:

- In – Input is standard input only signal
- Out – Totem Pole output is a standard active driver
- T/S – Tri-State is a bi-directional input output pin
- S/TS – Sustained Tri-State is an active low tri-state signal driven by one and only one agent at a time
- O/D – Open Drain allows multiple devices to share as a wire-OR.

I/O Interface

The I/O Interface in the EnCore 400 is actually divided into three separate 44-pin I/O interface connectors:

- IDE interface connector (J1)
- Floppy/Parallel/Serial Interface connector (J8)
- Utility Interface connector (J9)

IDE Interface (J1)

The IDE device signals are provided to the baseboard through the IDE 44-pin connector (J1).

IDE Features:

- Master mode PCI supporting Enhanced IDE devices
- Supports two EIDE devices
- Increased reliability using UDMA 33 transfer protocols
- Full scatter-gather capability
- Supports ATAPI compliant devices including DVD
- Support IDE native and ATA compatibility modes

Table 3-4. IDE Interface Pin/Signal Descriptions (J1)

Pin #	Signal	Description
1	RESET*	Low active hardware reset (RSTDRV inverted)
2	GND	Digital Ground
3	D7	Disk Data - These signals (0 to 15) provide the disk data signals
4	D8	Disk Data - These signals (0 to 15) provide the disk data signals
5	D6	Disk Data - These signals (0 to 15) provide the disk data signals
6	D9	Disk Data - These signals (0 to 15) provide the disk data signals
7	D5	Disk Data - These signals (0 to 15) provide the disk data signals
8	D10	Disk Data - These signals (0 to 15) provide the disk data signals
9	D4	Disk Data - These signals (0 to 15) provide the disk data signals
10	D11	Disk Data - These signals (0 to 15) provide the disk data signals
11	D3	Disk Data - These signals (0 to 15) provide the disk data signals
12	D12	Disk Data - These signals (0 to 15) provide the disk data signals
13	D2	Disk Data - These signals (0 to 15) provide the disk data signals
14	D13	Disk Data - These signals (0 to 15) provide the disk data signals
15	D1	Disk Data - These signals (0 to 15) provide the disk data signals
16	D14	Disk Data - These signals (0 to 15) provide the disk data signals
17	D0	Disk Data - These signals (0 to 15) provide the disk data signals
18	D15	Disk Data - These signals (0 to 15) provide the disk data signals
19	GND	Digital Ground
20	Key	Key pin plug

Pin #	Signal	Description
21	IDRQ0	Primary Device DMA Channel Request - Used for DMA transfers between host and drive (direction of transfer controlled by IOR* and IOW*). Used in an asynchronous mode with IDACK0*. Drive asserts IDRQ0 when ready to transfer or receive data.
22	GND	Digital Ground
23	IOW*	Primary Device I/O Read/Write Strobe - Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
24	GND	Digital Ground
25	IOR*	Primary Device I/O Read/Write Strobe - Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
26	GND	Digital Ground
27	IORDY	Primary Device I/O-DMA Channel Ready - When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
28	CSEL	Cable Select - Used to configure IDE drives as device 0 or device 1 using a special cable.
29	IDACK0*	Primary Device DMA Channel Acknowledge - Used by the host to acknowledge that data has been accepted or data is available. Used in response to IDRQ0 asserted.
30	GND	Digital Ground
31	IRQ14	Interrupt Request 14 - Asserted by drive when it has a pending interrupt (PIO transfer of data to or from the drive to host.
32	NC	Not connected
33	A1	IDE ATA Primary Disk Address (0 to 2) - Used to indicate which byte in the ATA command block or control block is being accessed
34	NC	Not connected
35	A0	IDE ATA Primary Disk Address (0 to 2) - Used to indicate which byte in the ATA command block or control block is being accessed.
36	A2	IDE ATA Primary Disk Address (0 to 2) - Used to indicate which byte in the ATA command block or control block is being accessed.
37	CS0	Primary Slave/Master Chip Select - Used to select the host-accessible Command Block Register
38	CS1	Primary Slave/Master Chip Select - Used to select the host-accessible Command Block Register
39	Reserved	Reserved – Not used
40	GND	Digital Ground
41	+5V	+5 volts ±5% power supply
42	+5V	+5 volts ±5% power supply
43	GND	Digital Ground
44	Reserved	Reserved – Not used

Note: The shaded area denotes power or ground. The signals marked with * indicate signal inversion.

Floppy/Parallel/Serial Interface (J8)

The Floppy disk controller, Parallel Port, and two Serial Ports are connected to the baseboard through the standard I/O 44-pin header (J8).

Floppy Disk Port/Parallel Port

The Super I/O chip contains the Floppy Disk Controller, which shares the same output connector as the Parallel Port, but you can only use one of these devices at a time.

The Super I/O chip also provides the Parallel port interface, which shares the same output connector as the Floppy Disk Controller. The Parallel port supports a Standard Printer Port (SPP), Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP) output.

NOTE	Due to the shared status of the output connector, only one device can be connected, that is, the floppy disk controller (floppy drive) or the parallel interface (printer port), but not both at the same time.

Serial Ports

The STPC chip contains the circuitry for the two 2 serial ports and both serial ports use TTL signals. The two serial ports support the following features:

- Both are 15540 compatible
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Two 16-bit FIFOs

Table 3-5. Floppy/Parallel/Serial Interface Pin/Signal Descriptions (J8)

Pin #	Signal	Description
1	STB*/ DS0*	Strobe – Output used to strobe data into the printer. I/O pin in ECP/EPP mode. Drive Select 0 – Select drive 0.
2	AFD/ DRVEN0*	Auto Feed – This is Request signal to the printer to automatically feed one line after each line is printed. Drive (Floppy) Density Select 0
3	PD0/ INDEX*	Parallel Port Data 0 - These signals (0 to 7) provide the parallel port data. Index – Sense to detect the head is positioned over the beginning of a track
4	ERR/ HDSEL	Error – This is a Status output signal from the printer. A Low State indicates an error condition on the printer Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
5	PD1/ TRK0	Parallel Port Data - These signals (0 to 7) provide the parallel port data Track 0 – Sense to detect that the head is positioned over track 0.
6	INIT*/ DIR*	Initialize – This signal used to Initialize printer. Output in standard mode, I/O in ECP/EPP mode. Direction – Direction of head movement (0 = inward motion, 1 = outward motion).
7	PD2/ WRTPRT*	Parallel Port Data - These signals (0 to 7) provide the parallel port data Write Protect – Senses the diskette is write protected.

Pin #	Signal	Description
8	SLIN/ STEP*	Select In – This signal Output used to select the printer. I/O pin in ECP/EPP mode. Step – Low pulse for each track-to-track movement of the head.
9	PD3/ RDATA*	Parallel Port Data - These signals (0 to 7) provide the parallel port data Read Data – Raw serial bit stream from the drive for read operations.
10	GND	Digital Ground
11	PD4/ DSKCHG*	Parallel Port Data 4 - These signals (0 to 7) provide the parallel port data. Disk Change – Senses the drive door is open or the diskette has been changed since the last drive selection.
12	GND	Digital Ground
13	PD5	Parallel Port Data 5 - These signals (0 to 7) provide the parallel port data
14	GND	Digital Ground
15	PD6/ MTR0*	Parallel Port Data 6 - These signals (0 to 7) provide the parallel port data Motor Control 0 – Select motor on drive 0.
16	GND	Digital Ground
17	PD7	Parallel Port Data 7 - These signals (0 to 7) provide the parallel port data
18	GND	Digital Ground
19	ACK*/ DS1*	Acknowledge – This is a Status output signal from the printer. A Low State indicates it has received the data and is ready to accept new data. Drive Select 1 – Select drive 1.
20	GND	Digital Ground
21	BSY/ MTR1*	Busy – This is a Status output signal from the printer. A High State indicates the printer is not ready to accept data. Motor Control 1 – Select motor on drive 1.
22	GND	Digital Ground
23	PE/ WDATA*	Paper End – This is a Status output signal from the printer. A High State indicates it is out of paper. Write Data – Encoded data to the drive for write operations.
24	GND	Digital Ground
25	SLCT/ WGATE*	Select – This is a Status output signal from the printer. A High State indicates it is powered on. Write Gate – Signal to the drive to enable current flow in the write head.
26	NC	Not Connected
27	DCD1*	Data Carrier Detect 1 – Indicator to serial port 1 that external modem is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR1 as part of the DTR/DSR handshake. Designed for direct input from external RS232 receiver.
28	DSR1*	Data Set Ready 1 – Indicator to serial port 1 that external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate. Designed for direct input from external RS232 receiver.
29	RXD1	Receive Data 1– Serial port 1 receive data in
30	RTS1*	Request To Send 1 – Indicates serial output port 1 is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control. Designed for direct input to external RS232 driver.

Pin #	Signal	Description
31	TXD1	Transmit Data 1 – Serial port 1 transmit data out
32	CTS1*	Clear To Send 1 – Indicator to serial port 1 that external serial communications device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control. Designed for input from external RS232 receiver.
33	DTR1*	Data Terminal Ready 1 –Indicates serial port 1 is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate. Designed for direct input to external RS232 driver.
34	RI1*	Ring Indicator 1 – Indicator to serial port 1 that external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. Designed for direct input from external RS232 receiver (whose input is typically not connected in direct connect environments).
35	GND	Digital Ground
36	DSR2*	Data Set Ready 2 – Indicates to serial port 2 that external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate. Designed for direct input from external RS232 receiver.
37	RXD2	Receive Data 2 – Serial port 2 receive data in.
38	RTS2*	Request To Send 2 – Indicator to serial output port 2 is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control. Designed for direct input to external RS232 driver.
39	TXD2*	Transmit Data 2 – Serial port 2 transmit data out.
40	CTS2*	Clear To Send 2 – Indicator to serial port 2 the external serial communications device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control. Designed for input from external RS232 receiver.
41	VCC	+5 volts ±5% power supply input
42	VCC	+5 volts ±5% power supply input
43	GND	Digital Ground
44	DTR2*	Data Terminal-Ready 2 – Indictor to Serial port 2 that external serial communications device is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate. Designed for direct input from external RS232 receiver.

Notes: The shaded area denotes power or ground. * = Negative true logic

Utility Interface (J9)

The Utility interface uses a 44-pin 2mm header on the module to interface various utility signals to the baseboard. The Utility interface consist of the following items:

- USB (Universal Serial Bus)
- PS/2 Controller (Keyboard and Mouse)
- Infrared Port (IrDA)

Table 3-6. Utility Interface Pin/Signal Descriptions (J9)

Pin #	Signal	Description
1	AC_BIT_CLK	Audio CODEC 97 Clock – Not Connected
2	AC_DATA_IN	Audio CODEC 97 Data In – Not Connected
3	AC_DATA_OUT	Audio CODEC 97 Data Out – Not Connected
4	AC_SYNC	Audio CODEC 97 Sync – Not Connected
5	AC_RESET#	Audio CODEC 97 Reset – Not Connected
6	GND	Digital Ground
7	SPKR	Speaker Output
8	GND	Digital Ground
9	RSTSW#	Reset Switch
10	KBDATA	Keyboard Data
11	KBCLK	Keyboard Clock
12	GND	Digital Ground
13	+5V	+5 volts ±5% power supply input
14	MDATA	Mouse Data
15	MCLK	Mouse Clock
16	GND	Digital Ground
17	+5V	+5 volts ±5% power supply input
18	NC	Not connected – Reserved for future use
19	IRTX	Infrared Transmit – IR transmit data out from serial port 2
20	IRRX	Infrared Receive – IR receive data in to serial port 2
21	GND	Digital Ground
22	NC	Not connected – Reserved for future use
23	USBPWR0	USB Port 0 Power Protection – Port 0 is disabled if this input is low. Direct inputs are provided for over current protection.
24	USBP0N	Universal Serial Bus Port 0 Data Negative.
25	USBP0P	Universal Serial Bus Port 0 Data Positive
26	USBPWR1	USB Port 1 Power Protection – Port 1 is disabled if this input is low. Direct inputs are provided for over current protection.
27	USBP1N	Universal Serial Bus Port 1 Data Negative.
28	USBP1P	Universal Serial Bus Port 1 Data Positive.
29 (NC)	USBP2N	Universal Serial Bus Port 2 Data Negative – Not Connected
30 (NC)	USBP2P	Universal Serial Bus Port 2 Data Positive – Not Connected
31 (NC)	USBP3N	Universal Serial Bus Port 3 Data Negative – Not Connected

Pin #	Signal	Description
32 (NC)	USBP3P	Universal Serial Bus Port 3 Data Positive – Not Connected
33 (NC)	NC	Not Connected - Reserved
34 (NC)	DETECT#	Battery Low Indicator – Active Low (10K Pull up to 3.3V if not used) – Not Connected
35 (NC)	RI#	Ring Indicator – Not Connected
36	GND	Digital Ground
37 (NC)	SLPPWR	+3.3V Sleep Power – Not Connected
38 (NC)	AEN	Reserved - Not Connected
39 (NC)	SUSC#	Suspend Control – Not Connected
40	SMBDATA	System Management Bus Clock. – Not Connected
41	SMBCLK	System Management Bus Data – Not Connected
42 (NC)	SMBALRT#	System Management Bus Alert – Not Connected
43	V1	Voltage 1st – Not Connected
44	GND	Digital Ground

Note: The shaded area denotes power or ground.

NOTE	Pin-7, speaker output (PC speaker) requires an external drive circuit for the speaker on the baseboard design.

USB (Universal Serial Bus)

The EnCore 400 contains two root USB hubs with two ports each for a total of four functional USB ports. USB ports 1 and 2 include over-current detection status on the USB inputs (software function). Both USB v.1.1 and Intel Universal HCI v.1.1 are supported, as well as legacy keyboard and PS/2 mouse support.

NOTE	The EnCore 400 does not provide over-current fuses for any of the USB Ports on the module. If implemented the baseboard design requires integration of over-current fuses for the USB Ports.

Keyboard and PS/2 Mouse Controller

The embedded CPU provides the PS/2 controller support for both keyboard and mouse. You may also use a USB keyboard and mouse, but these USB I/O devices are software dependent.

Infrared Port (IrDA)

The Super I/O chip, FD37C669, provides the infrared controller. The Infrared Data Association (IrDA) port provides a two-way wireless communications port using infrared as a transmission medium. The IrDA (HPSIR) method is used for the infrared implementation provided on the module and uses a separate serial type port.

The IrDA port allows serial communication at baud rates up to 115k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a single infrared pulse is sent at the beginning of the serial bit time. A one is sent when no infrared pulse is sent during the bit time.

Using the IrDA port requires an understanding of the timing diagrams provided in the Super I/O controller chip specifications available on the manufacture's web site and referenced earlier in this manual. For more information, refer to the Standard Microsystems Corp Super I/O chip data book and the Infrared Data Association web site at http://www.irda.org.

Ethernet Interface (J7)

The Ethernet solution is provided by the Intel 82559ER PCI controller chip and consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution. The 82559 family members build on the basic functionality of the 82558 and contain power management enhancements.

The 82559ER is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the 82559ER to perform high-speed data transfers over the PCI bus. The 82559ER bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU. Two large transmit and receive FIFOs of 3 Kbytes each help prevent data underflow and overflow, allowing the 82559ER to transmit data with of minimum interframe spacing (IFS).

- Ethernet physical connections:
  - Ethernet interconnect uses a 10-pin 2mm header between the module and baseboard.
- Ethernet Controller Chip features:
  - Intel Corporation's 82559ER chip
  - The 82559ER can operate in either full duplex or half-duplex mode.
    - In full duplex mode the 82559ER adheres to the IEEE 802.3x Flow Control specification.
    - In half-duplex mode, performance is enhanced by a proprietary collision reduction mechanism.
- Implemented features on the Ethernet chip (82559ER) include the following:
  - IEEE 802.3 10BaseT/100BaseT compatible physical layer
  - 32-bit PCI controller
  - Enhanced scatter-gather
  - Bus mastering capabilities
  - Digital adaptive equalization control
  - Link status interrupt capability
  - Boundary scan support
  - 3-port LED support (speed, link and activity)
  - 10BaseT auto-polarity correction
  - Diagnostic loopback mode
  - Low power (300mW typical in active transmit mode)
  - Reduced power in "unplugged mode" (less than 50mW)
  - Low power 3.3V device
  - Automatic detection of "unplugged mode"
  - Full duplex support at 10Mbps or 100Mbps
  - IEEE 802.3u Auto-Negotiation support
  - 3kB transmit and 3kB receive FIFOs
  - IEEE 802.3x 100BASE-TX flow control support

The 82559ER includes a simple PHY interface to the wire transformer at rates of 10BaseT and 100BaseTX, and Auto-Negotiation capability for speed, duplex, and flow control. These features and others reduce cost, real estate, and design complexity.

Table 3-7. Ethernet Internal Interface Pin/Signal Descriptions (J7)

Pin #	GND	Descriptions
1	TX+	Analog Twisted Pair Ethernet Transmit Differential Pair – These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair Cable (UTP). These signals interface directly with an isolation transformer.
2	TX-	
3	TXCT	Transmit center tap connected to the magnetic coil of isolation transformer
4	RXCT	Receive center tap connected to the magnetic coil of isolation transformer
5	RX+	Analog Twisted Pair Ethernet Receive Differential Pair – These pins receive the serial bit stream from the isolation transformer.
6	RX-	
7	GND	Digital Ground
8	LINKLED	Link Integrity LED – The LINK LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off.
9	ACTLED	Activity LED – The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.
10	SPEEDLED	Speed LED – The Speed LED pin indicates the speed of the connection. The speed LED will be on for 100Mbps and off for 10Mbps.

Note: The shaded area denotes power or ground.

NOTE The EnCore 400 module does not include an Isolation Transformer or RJ45 Jack for signal conditioning of the Ethernet connection. An Ethernet Interface Circuit is required on your custom logic baseboard.

LCD/CRT Graphics Interface (J6)

The CPU provides the LCD/CRT graphics interface provides the video signals for flat panel displays and the traditional glass CRT monitors. The video interface (LCD/CRT) between the module and baseboard uses a 44-pin 2mm header. The features are listed below:

NOTE	The EnCore 400 modules shipped from the factory are only configured for CRT support. Ampro provides LCD/TFT support for flat panels with specific resolutions. Refer to the Release Notes and the Ampro web site for instructions and additional information when customizing the BIOS to a particular flat panel.

Features

- Enhanced 2D Graphics Controller
  - Supports Pixel Depths of 8, 16, 24 and 32-bit
  - Full BitBLT Implementation for All 256 Raster Operations Defined for Windows
  - Supports 4 Transparent BLT Modes
    - Bitmap Transparency
    - Pattern Transparency
    - Source Transparency
    - Destination Transparency
  - Hardware Clipping
  - Fast Line Draw Engine with Anti-aliasing
  - Fast Triangle Fill Engine
  - Supports 4-bit Alpha Blend Font for Anti-aliased Text Display
  - Complete Double Buffered Registers for Pipelined Operation
  - 64-bit Wide Pipelined Architecture running at 100MHz
  - Video memory up to 4MB; selected in BIOS Setup
- CRT Controller
  - Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz Display
  - Supports 24-bit pixel depth
  - Interlaced or Non-interlaced Output
- TFT Display Controller
  - Supports Up to 1024 x 1024 Display Resolutions
  - Supports 9-, 12-, 18-bit Interface (1 Pixel/Clock)
  - Supports 2x9-bit Interface (2 Pixels/Clock)
  - Programmable Image Position and Size
  - Image Expansion Capability in graphics mode
- Video Interface Connector (J6)

Table 3-8. Video Interface Pin/Signal Descriptions (J6)

Pin #	Signal	Description
1	SHFCLK	Shift Clock. – This signal provides the clock for transferring digital pixel data.
2	M/DE	Data Enable – This signal indicates valid data is on any of the FP[23:0] lines.
3	LP	Line Pulse – This signal is the digital monitor equivalent of HSYNC
4	FLM	First Line Marker – This signal is digital monitor equivalent of VSYNC
5	GND	Digital Ground
6	GND	Digital Ground
7	FP0	Panel Data 0 – This signal provides the (Red 5) Digital pixel output signal.
8	FP1	Panel Data 1 – This signal provides the (Red 4) Digital pixel output signal.
9	FP2	Panel Data 2 – This signal provides the (Red 3) Digital pixel output signal.
10	FP3	Panel Data 3 – This signal provides the (Red 2) Digital pixel output signal.
11	FP4	Panel Data 4 – This signal provides the (Green 5) Digital pixel output signal.
12	FP5	Panel Data 5 – This signal provides the (Green 4) Digital pixel output signal.
13	FP6	Panel Data 6 – This signal provides the (Green 3) Digital pixel output signal.
14	FP7	Panel Data 7 – This signal provides the (Green 2) Digital pixel output signal.
15	FP8	Panel Data 8 – This signal provides the (Blue 5) Digital pixel output signal.
16	FP9	Panel Data 9 – This signal provides the (Blue 4) Digital pixel output signal.
17	FP10	Panel Data 10 – This signal provides the (Blue 3) Digital pixel output signal.
18	FP11	Panel Data 11 – This signal provides the (Blue 2) Digital pixel output signal.
19	FP12	Panel Data 12 – This signal provides the (Red 1) Digital pixel output signal.
20	FP13	Panel Data 13 – This signal provides the (Red 0) Digital pixel output signal.
21	FP14	Panel Data 14 – This signal provides the (Green 1) Digital pixel output signal.
22	FP15	Panel Data 15 – This signal provides the (Green 0) Digital pixel output signal.
23	FP16	Panel Data 16 – This signal provides the (Blue 1) Digital pixel output signal.
24	FP17	Panel Data 17 – This signal provides the (Blue 0) Digital pixel output signal.
25	FP18 (NC)	Panel Data signal 18 – Not connected
26	FP19 (NC)	Panel Data signal 19 – Not connected
27	FP20 (NC)	Panel Data signal 20 – Not connected
28	FP21 (NC)	Panel Data signal 21 – Not connected
29	FP22 (NC)	Panel Data signal 22 – Not connected
30	FP23 (NC)	Panel Data signal 23 – Not connected
31	ENAVDD	Enable Panel VDD Power – This signal is the power to Flat panel displays.
32	ENAVEE	Enable Panel VEE Power – This signal is the power to Flat panel displays.
33	+3.3V Out	+3.3 volts ±5%
34	+12V Out	+12 volts ±5%
35	GND	Digital Ground
36	GND	Digital Ground
37	HSYNC	Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT. Also used (with VSYNC) pass to signal power management state information to the CRT per the VESA™ DPMS™ standard.

Pin #	Signal	Description
38	VSYNC	Vertical Sync – This signal is used for the digital vertical sync output to the CRT. Also used (with HSYNC) to pass signal power management state information to the CRT per the VESA™ DPMS™ standard.
39	AGNDR	Analog Ground for Red
40	RED	Red – This signal is the Red analog output to the CRT.
41	AGNDG	Analog Ground for Green
42	GREEN	Green – This signal is the Green analog output to the CRT.
43	AGNDB	Analog Ground for Blue
44	BLUE	Blue – This signal is the Blue analog output to the CRT.

Note: The shaded area denotes power or ground.

Miscellaneous

Real Time Clock (RTC)

The EnCore 400 module contains a Real Time Clock (RTC) and is backed up with a replaceable Lithium Battery on the module. The replacement battery should provide a 7-to-10 year battery life. The module will function without an RTC battery in an environment, which prohibits inclusion of a battery. The module will also continue to operate after the battery life has been exceeded. Under these conditions all setup information is restored from the onboard serial EEPROM during POST along with default data and time information.

NOTE	Some operating systems require a valid default date and time to function.

OOPs Jumper

The OOPs jumper is provided in the event the BIOS settings you've selected prevent you from booting the system. By using the OOPs jumper you can prevent the current BIOS settings in the EEPROM from being loaded, allowing use of the default settings. Connect the DTR pin to the RI pin on Serial port 1 prior to boot up to prevent the present BIOS settings from loading. After booting with the OOPs jumper in place, remove the OOPs jumper and go into BIOS Setup. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

NOTE	On all Ampro provided EnCore baseboards, DTR pin = pin 4 and RI pin = pin 9 on Serial Port 1 using a female serial connector.

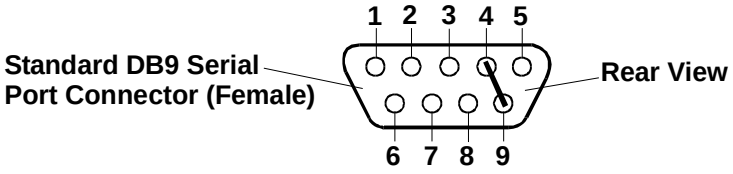

Figure 3-1. OOPs Jumper

WatchDog Timer (WDT)

The watchdog timer restarts the system if a mishap occurs, ensuring proper start-up after the interruption. Possible problems include failure to boot properly, the application software's loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT can be controlled directly from your application or from a BIOS call. To control the WDT from with-in the BIOS, please refer to the following discussion.

The Watchdog timer can be started with the standard PC/AT INT15 WDT BIOS function call. The timer resolution will be in seconds and a time-out will initiate a system management interrupt (SMI). The SMI handler will execute a hardware reset. WDT tickle will be a read of port 201h, each read will reset the WDT time-out to the value indicated in by the last INT15 WDT BIOS start function call.

The EnCore 400 BIOS supports the module's watchdog timer in two ways:

- The initial watchdog timer setting – This is specified using the BIOS Setup to determine if the watchdog timer monitors the system boot, and if so, how long the time-out will be (30, 60, or 120) in seconds.

  The initial time-out setting should be long enough to ensure the system can boot and pass control to the application or Operating System. Then, the application or OS must periodically retrigger the timer by reading the I/O Port 201h so the time-out does not occur. If the time-out does occur, the system will be reset.

- Standard ROM-BIOS function – These functions may be used by the OS or the application software to start and stop the watchdog timer function.

To use this WATCHDOG DOS program, simply type the program's name, along with the desired option (listed below), on the DOS command line. Or, you may enter a similar command in an appropriate batch file.

The command choices are:

```
C>WATCHDOG OFF
```

which turns the timer off. To set a specific watchdog time interval, use this syntax:

```
C>WATCHDOG ON=secs
```

This command starts or retriggers the watchdog timer with a time-out of xxx secs (seconds), where xxx has a range of 1 to 255 seconds.

```
C>WATCHDOG ?
```

displays a help screen.

Generally, the watchdog timer should be retriggered from within your application program, rather than with the WATCHDOG utility program.

Ampro provides a WATCHDOG DOS program that you can use from the command line or in a batch program to manage the watchdog timer. This Ampro WATCHDOG DOS program is used to start, stop, or retrigger the EnCore 400 module's watchdog timer from the command line or from within a batch file.

The following simple assembly language routine illustrates how to control the watchdog timer using a standard ROM-BIOS function call provided for this purpose:

```
;-------------------------------------------------------
; Watchdog timer control program
;-------------------------------------------------------
MOV  AH,0C3h     ; Watchdog Timer BIOS function
MOV  AL,nn ; Use "00" to disable, "01" to enable
     ; timer.
MOV   BX,mm      ; Selects time, in seconds
                 ;(00-FFh; 1-255 seconds)
INT   15h
```

Power Interface (J4)

The EnCore 400 requires three regulated DC voltages from the logic baseboard. There is a voltage regulator on the module that supplies 2.5 volts to the CPU. The power supply connector uses a 10-pin header at 0.100" spacing.

The power interface connector (J4) supplies the following voltages directly from the baseboard:

- 3.3V @ 0.5 Amps
- 5.0V @ 1.5 Amps

Table 3-9 provides the power interface signals and pin outs.

Table 3-9. Power Interface Pin/Signal Descriptions (J4)

Pin	Signal	Pin	Signal
1	+5	2	GND
3	+3.3	4	GND
5	+12	6	GND
7	+3.3	8	GND
9	+5	10	GND

Note: The shaded area denotes power or ground.

Chapter 4 BIOS Setup

Introduction

This chapter describes the BIOS Setup menus and the various screens used for configuring the EnCore 400 module. Some features in the Operating System or application software may require configuration in the BIOS Setup screens.

This section assumes the user is familiar with general BIOS Setup and does not attempt to describe the BIOS functions. Refer to the appropriate PC reference manuals for information about the software interface of the onboard ROM-BIOS. If Ampro has added to or modified the standard functions, these functions will be described.

The options provided for the EnCore 400 module are controlled by BIOS Setup. BIOS Setup is used to configure the module, modify the fields in the Setup screens, and save the results in the onboard configuration memory. Configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and the flash memory.

The Setup information is retrieved from configuration memory when the module is powered up or when it is rebooted. Changes made to the Setup parameters, with the exception of the time and date settings, do not take effect until the module is rebooted.

Setup is located in the ROM BIOS and can be accessed, when prompted using the <Del> key, while the module is in the Power-On Self Test (POST) state, just before completing the boot process. The screen displays a message indicating when you can press <Del>, similar to the following message.

```
Hit <Del> if you want to run SETUP
```

The EnCore 400 module's Setup is used to configure items in the BIOS using the following menus:

- Basic CMOS Configuration
- Custom Configuration
- Reset CMOS to Factory Defaults
- Write to CMOS and Exit
- Exit without changing CMOS

Accessing Setup

The BIOS Setup menu offers the choices listed above, and the corresponding items are described in the following topics. To access BIOS Setup:

1. Turn on the monitor and the logic baseboard power supply.
2. Start Setup by pressing the [Del] key, when the following message appears on the boot screen.

```
Hit <Del> if you want to run SETUP
```

BIOS Menus

Table 4-1 summarizes the list of BIOS menus and some of the features available for EnCore 400 module.

Table 4-1. BIOS Setup Menus

BIOS Setup Menu	Item/Topic
Basic CMOS Configuration	Date and Time Drive Assignment Order Boot order Keyboard settings Boot device Memory settings IDE Drive Settings Floppy Drive types
Custom Configuration	PIO settings DMA settings Video Memory settings Video settings Watchdog Timer settings
Reset CMOS to last known values	Option resets CMOS to last known BIOS settings
Reset CMOS to Factory Defaults	Option to reset CMOS
Write to CMOS and Exit	Option to write to CMOS and exit
Exit without change CMOS	Option to exit CMOS

BIOS Setup Opening Screen

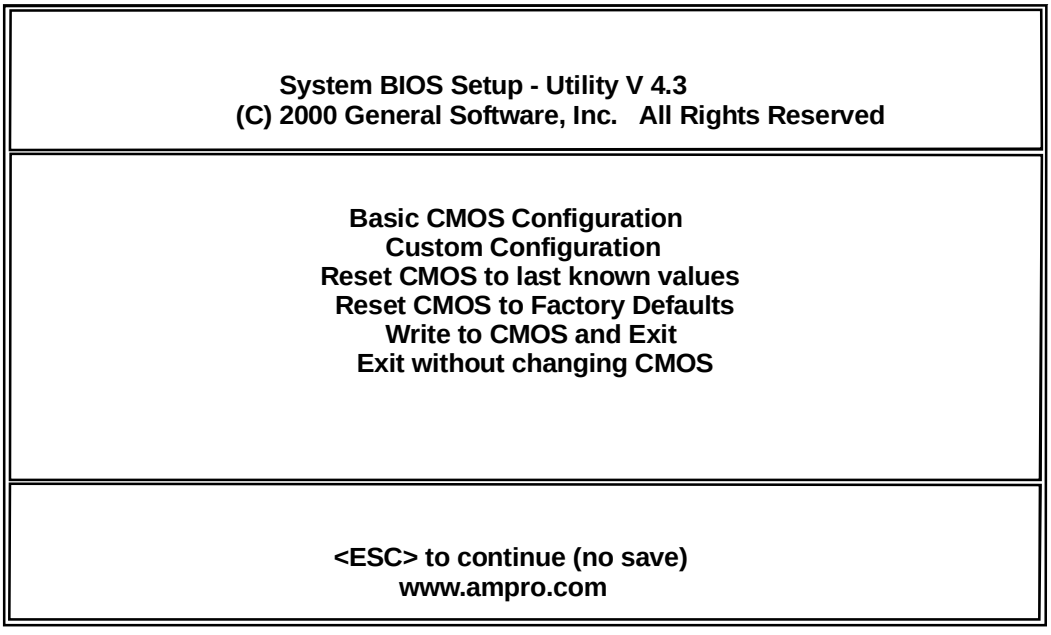

Figure 4-1. BIOS Setup Opening Screen

NOTE	The default values or the typical settings are shown highlighted in the list of options. Refer to the bottom of the BIOS screens for navigation instructions when making selections.

Basic CMOS Configuration

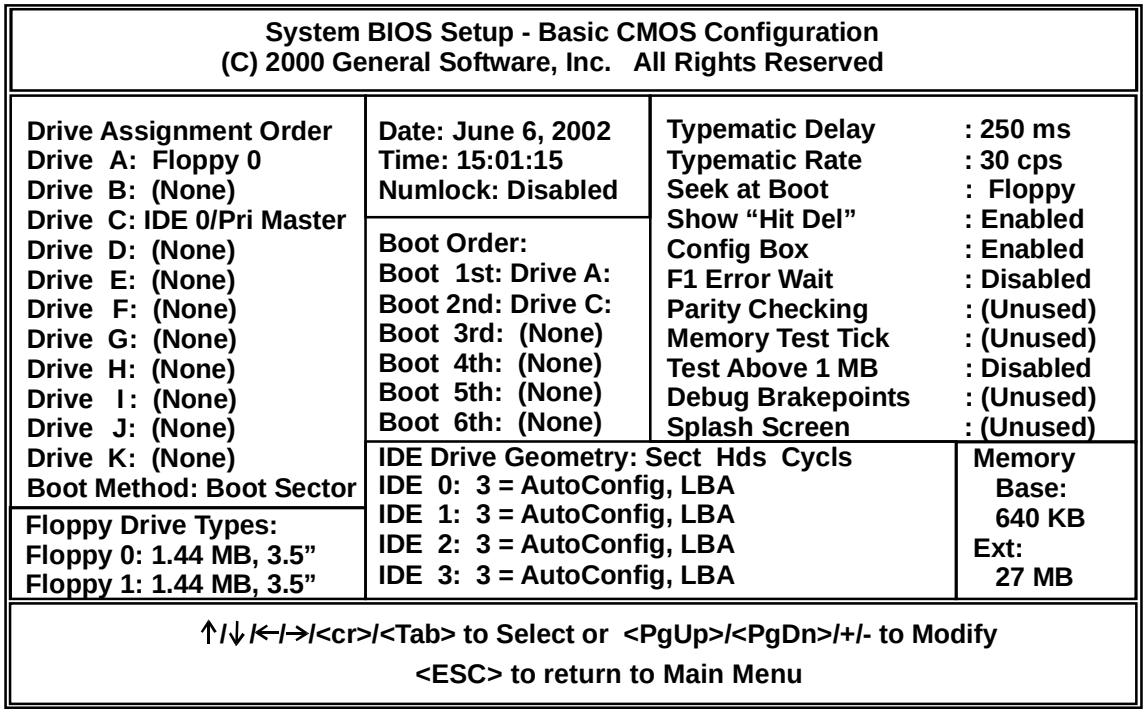

Figure 4-2. BIOS Setup Basic CMOS Configuration Screen

- Left Column Display, Drive Assignment Order – This section provides up to two floppy drives, and up to 9 drives, including a CD-ROM, or one large drive with multiple partitions.
  - Drives A & B – [None], [**Floppy 0**], [Floppy 1], [CD F1/Pri Master], or [CD F1/Pri Slave]
  - Drives C-D – [None], [Floppy 0], [Floppy 1], [CD F1/Pri Master], [CD F1/Pri Slave], [**Ide 0/Pri Master**], [Ide 1/Pri Slave], [CD Hd/Pri Master], or [CD Hd/Pri Slave]

    If a CD-ROM is connected as slave, use [CD Hd/Pri Slave] for the CD-ROM.
  - Drives E-K – [**None**], [Ide 0/Pri Master], [Ide 1/Pri Slave], [CD Hd/Pri Master], or [CD Hd/Pri Slave]
  - Boot Method – [**Boot Sector**] or [Windows CE]
  - Floppy Drive Types – [Not installed], [360kB, 5.25"], [1.2MB, 5.25"], [720kB, 3.5"], [**1.44MB, 3.5"**], or [2.88MB, 3.5"]
- Middle Column Display, Boot Order – Allows you to change the boot order of 6 devices, where the selections are:
  - [None], [Drive A], [Drive B], [Drive C], [Drive D], [Drive E], [Drive F], [Drive G], [Drive H], [Drive I], [Drive J], [Drive K], [High ROM], [DOS-ROM], [Mfg Mode], or [Debugger]

NOTE	If the Boot order is, A, C, D (where D is a CD-ROM), then the BIOS will search for a bootable device in drive A. If a bootable device is not found in drive A, it will continue searching in drive C, then drive D, until it finds a bootable device. If no bootable device is found, the screen will display "No Bootable Device Available" and the boot process will stop for about 5 seconds, allowing you to select from: R – for Reboot, or S – for Setup. If you have not made a selection at the end of 5 seconds, the BIOS will reboot the system and start over, until you intervene in the process.

- Right Column Display
  - Typematic Delay – [Disabled], [**250ms**], [500ms], [750ms], or [1000ms]

    This feature is used for the keyboard and determines the typing delay.
  - Typematic Rate – [**30cps**], [24cps], [20cps], [15cps], [12cps], [10cps], [8cps], or [6cps]

    This feature is used for the keyboard and determines the typing rate.
  - Seek at Boot – [None], [**Floppy**], [Ide], or [Both]

    This feature determines the type of boot device the Setup will search for during the boot process.
  - Show "Hit Del" – [**Enabled**] or [Disabled]

    This feature, if Enabled, will place "Hit Del" on screen during the boot process, to indicate when you may Hit Del to enter the BIOS Setup menus.
  - Config Box – [**Enabled**] or [Disabled]

    This feature, if Enabled, displays the Configuration Summary Box, which list all of the configuration information for the system, at the completion of POST, but before the Operating System is loaded.
  - F1 Error Wait – [Enabled] or [**Disabled**]

    This feature, if Enabled, will display an Error message indicating when an error has occurred and wait for you to respond by hitting the F1 key.
  - Parity Checking – (**Unused**)
  - Memory Test Tick – (**Unused**)
  - Test Above 1MB – [Enabled] or [**Disabled**]

    This feature, if Enabled, will test all of the SDRAM memory above 1MB during POST and will display the results on screen while the memory test is being conducted. However, this slows down the completion of POST sequence. To speed up the POST process, select Disabled for this feature.
  - Debug Breakpoints – (**Unused**)
  - Splash Screen – (**Unused**)
- Middle-Bottom Column, IDE Drive Geometry
  - Ide 0-3: [Not installed], [1=User Type, Set 01 Hds 1 Cyls 0], [2=Autoconfig, Physical], [**3=Autoconfig, LBA**], or [4=Autoconfig, Phoenix]

    This feature, if enabled, determines the IDE hard drive's setup information. However, IDE hard drives only use [3=Autoconfig, LBA] for configuration setup. The only exception would be an older IDE hard drive with an older operating system.

Custom Configuration

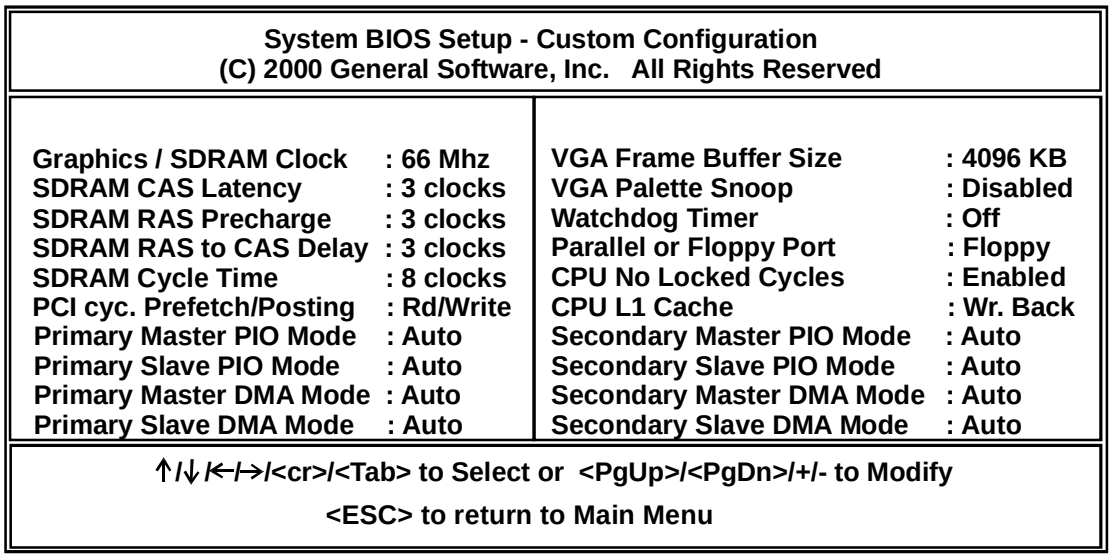

Figure 4-3. BIOS Setup Custom Configuration Screen

- Left Column Display
  - Graphics/SDRAM Clock – [45 MHz], [50 MHz], [55 MHz], [60 MHz], [**66 MHz]**, [75 MHz], [80 MHz], [85 MHz], [90 MHz], [95 MHz], or [100 MHz]
  - SDRAM CAS Latency – [1 clock], [2 clocks], or [**3 clocks**]
  - SDRAM RAS Precharge – [1 clock], [2 clocks], [**3 clocks**], or [4 clocks]
  - SDRAM RAS to CAS Delay – [1 clock], [2 clocks], [**3 clocks**], or [4 clocks]
  - SDRAM Cycle Time – [6 clocks], [7 clocks], [**8 clocks**], or [9 clocks]
  - PCI cyc. Prefetch/Posting – [Disabled], [Write], [Read], or [**Rd/Write**]
  - Primary Master PIO Mode – [0], [1], [2], [3], [4], or [**Auto**]
  - Primary Slave PIO Mode – [0], [1], [2], [3], [4], or [**Auto**]
  - Primary Master DMA Mode – [0], [1], [2], or [**Auto**]
  - Primary Slave DMA Mode – [0], [1], [2], or [**Auto**]
- Right Column Display
  - VGA Frame Buffer – [Unused], [128 kB], [256 kB], [384 kB], [512 kB], [640 kB], [768 kB], [896 kB], [1024 kB], [1152 kB], [1280 kB], [1408 kB], [1536 kB], [1664 kB], [1792 kB], [1920 kB], [2048 kB], [2176 kB], [2304 kB], [2432 kB], [2560 kB], [2688 kB], [2816 kB], [2944 kB], [3072 kB], [3200 kB], [3328 kB], [3456 kB], [3584 kB], [3712 kB], [3840 kB], [3968 kB], or [**4096 kB**]
  - VGA Palette Snoop – [**Disabled**] or [Enabled]
  - Watchdog Timer – [**Off**], [30 sec], [60 sec], or [120 sec]

    This feature, if Enabled by selecting a timer interval, will initiate the Watchdog timer to reset the system if an error occurs and helps assure proper start-up after a failure.
  - Parallel or Floppy Port – [**Floppy**] or [Parallel]

    This feature selects which device will be connected to the shared interface port; the Parallel port or the Floppy port.

- CPU No Locked Cycles – [Disabled] or [**Enabled**]
- CPU L1 Cache – [Disabled] and [Wr. Thru] or [**Wr. Back**]
- Secondary Master PIO Mode – [0], [1], [2], [3], [4], or [**Auto**]
- Secondary Primary Slave PIO Mode – [0], [1], [2], [3], [4], or [**Auto**]
- Secondary Primary Master DMA Mode – [0], [1], [2], or [**Auto**]
- Secondary Primary Slave DMA Mode – [0], [1], [2], or [**Auto**]

Appendix A Technical Support

Ampro Computers, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Ampro provides a comprehensive listing of Frequently Asked Questions on our web site at the Virtual Technician. If you can not find the answers to your questions, please continue in the Virtual Technician and ask for Personal Assistance. Requests for support through the web site are given the highest priority, and usually will be addressed within one working day.

- **Internet** – Provides the most information concerning Ampro products, including reference material and white papers.
  - Ampro Virtual Technician – This service is free and available 24 hours a day through the Ampro Computers World Wide Web site at http://www.ampro.com. However, you must sign in to access this service.

    The Ampro Virtual Technician is a searchable database of Frequently Asked Questions, which will help you with the common questions asked by most customers. This is good source of information to look at first for your technical solutions.
  - Embedded Design Resource Center – This service is also free and available 24 hours a day at the Ampro web site at http://www.ampro.com. However, you must sign in to access this service.

    The Embedded Design Resource Center was created as a resource for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience. This page contains links to White Papers, Specifications, and additional technical information.
- **Personal Assistance** – This is the quickest way to obtain a response to your support questions. Please go to the following location on Ampro's web site to submit your request 24 hours a day, 7 days a week.

Table A-1. USA Technical Support Contact Information

Method	Contact Information
Web Site	http://www.ampro.com
E-mail	support@ampro.com
Standard Mail	Ampro Computers, Incorporated, 5215 Hellyer Avenue, San Jose, CA 95138-1007, USA

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