MicroSys

User's Manual

IP860 Rev. 2

5th edition

Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
Mühlweg 1
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Germany

declare that the product

IP860

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position: General Manager

Edition

	Date:	Ident-Nr.:	Released:
Manual	07.10.02	EW267MA-02AF	

Chapter 12.4 Description of JTAG Pin 11 corrected. Chapter 12.5 added.

Manual	26.03.02	EW267MA-02AE	

Chapter 6.4 SRAM backup description corrected.
Chapter 13.4 RxD and TxD changed in ST23 and ST24 tables.
14.16 Board Revision Register added.

Schematics	05.10.99	EW267SL-02AB	

Table of Contents

1. Introduction

1.1 Short Description

The **IP860** is a product out of the MicroSys' **Single Euro** PowerPC VMEbus line, based on the **MPC8XX Power QUICC** from Motorola.. One configuration is based on Motorola's **MPC860 PowerQUICC** embedded processor, while the other uses an **MPC821 PowerQUICC** communication controller. The MPC860 offers two additional serial communication controllers (SCCs); the MPC821 version has an integrated LCD controller instead. In other respects, the logic design is the same for both versions.

The IP860 offers a 16 bit wide VMEbus shared **SRAM** area, a 32 bit wide **DRAM** bank and a 32 bit wide **FLASH** memory bank.

The board firmware is stored within the Flash memory. Software changes can be done in-system. The **SRAM** as well as the onboard **real time clock** are supported by a service free gold capacitor, and for extended backup time by the 5V standby line of the VMEbus.

A serial **EEPROM** allows the power free storage of board or user specific data.

The board contains **two** piggyback slots according to the VITA Specification Revision 1.0.e.0 for **IP modules**. It was designed to work as an intelligent carrier board for 'IndustryPack' modules in embedded, stand-alone or multiprocessing applications. The various communication functions of the MPC860 are accessible by an additional slot for special I/O modules, which offers all kind of EIA interface standards or network facilities. The **background debug port**, the JTAG test port, and the **I**n-**S**ystem-**P**rogramming port of the onboard logic can be used for board maintenance and software debug purposes.

The VMEbus interface contains a single level arbiter and requester with RWD & ROR option, a programmable 7 level **VMEbus interrupter** and interrupt handler. A memory mapped **mailbox** with local interrupt capability allows for backplane network applications. The two SMC serial interface channels of the MPC860 with RS232 standard are accessible onboard the IP860 via two 6pin Molex connectors.

The IP860 will take a maximum of **64 Mbytes** of **DRAM, 8 Mbytes** of **Flash** memory and up to **1 Mbytes** of **SRAM.**

The complete board is implemented in **CMOS technology**. Main part of the design is working at 3,3V to ensure low power and higher lifetime. IP860 works at power consumption as low as: **5V / 6W @ 50MHz** CPU speed.

The 5 volt board supply voltage is protected by a transient suppresser diode against overvoltage or wrong polarity.

The IP860 conforms to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297.

1.2 Options

- different CPUs (MPC860EN, MPC860T, MPC860SAR or MPC821)

- different DRAM sizes

- different FLASH memory sizes

- different SRAM memory sizes

- different IP compatible modules

- different IExxx communication piggyback boards

- extended temperature range -40°C to + 85°C

1.3 Specifications

The power requirements for the IP860 board are shown in the following table. The given values are valid for the IP860 with 16 Mbyte DRAM. The power consumption of the optionally used IP-Modules and I/O-Module must be added to the given values.

Power Requirements:

+5V, +5%/-2.5%,	1.2A + used I/O modules or IP
+12V, +5%/-2.5%	0.0mA + used I/O modules or IP
-12V, +5%/-2.5%	0.0mA + used I/O modules or IP

Environmental Requirements:

Operating Temperature	0 ° C to +70 ° C
	-40°C to +85°C optional
Relative Humidity	0 to 95 % (non-condensing)
Storage Temperature	-40 ° C to + 85 ° C

The IP860 can be supplied with single 5 volts, if neither the optional IP modules nor the optional I/O module uses the 12 volts supply.

1.4 Related Documentation

The following manual are applicable to the IP860:

- VMEbus Specification Manual ANSI/IEEE STD1014-1987

- IP Modules Standard VITA 4-1995

- MPC860 PowerQUICC User's Manual

- Real-time Clock V3021 User's Manual

1.5 Naming and counting conventions

Mayor differences between a 68K style design and a PowerPC architecture style design include the fact that MSB is bit 0 and the highest interrupt level is 0 not 7.
To keep confusion as little as possible following bit numbering is used in this manual:

All description related to MPC860 and its manual uses Bit 0 for MSB. This way there is no difference between MPC860 documentation and this manual.
Same (MSB Bit 0) is used for complete description of On Board Programming registers, because they are directly accessed by the MPC860 and this way should not differ from its nomenclature.

In schematics all address and data busses use numbering for VME systems. That means that MPC860 bit 0 is connected to board bit 31 (f.e.: CPU-D0 = board-D31, CPU-A31 = board-A0).
All description of the VMEbus interface is using VME naming conventions using bit 0 = LSB.
All description of IP-slot interface is using VITA naming conventions using bit 0 = LSB.

2. Delivery

2.1 Items shipped with this unit

– User's Manual IP860 Hardware

– MicroSys shipping carton

> **ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT**

2.2 Hints for unpacking, handling and storing

– Avoid touching areas if integrated circuitry.

– Unit should only be placed on a static-free conductive surface

– Unit must only be transported using anti-static bags or MicroSys Shipping carton

– Packing should be saved if unit needs to be reshipped or returned

– When the unit needs to be stored, it should be placed in a moistfree, dustfree environment. The storage temperatures and humidity specifications are shown in chapter 1

3. Installation

3.1 Items required for IP860 installation

For installation of the IP860, the following items are required.

– Card cage or housing

– VMEbus motherboard

– Adequate rated power supply

3.2 Points to be observed

Before the unit is inserted into the card cage, the following points should be observed.

– Unit requires +5V (+ 5 %, - 2,5 %),

– Unit requires optional +/-12V (+ 5 %, - 2,5 %),

– Mounted IP-Modules may require +/-12V.

– Be sure voltage is of correct polarity.

– Unit should only be inserted into, and removed from card cage when power is off.

– The IP-Modules must only be inserted or removed during power off.

– The card cage should be well ventilated. The operating temperature should never exceed

it's specified range.

– Check default jumper or switch setting.

GUARANTEE IS VOID IF UNIT IS OPERATED

OUT OF IT'S SPECIFICATIONS!

4. Board Overview

4.1 Features IP860

Board Format:	single eurocard format
Main Processor:	MPC860, Power (QU)ad (I)ntegrated (C)ommunication (C)ontroller
	alt. MPC821 processor
	PowerPC core
	background debug mode
	clock rate up to 50MHz
	programmable memory controller functions
	four general purpose timers
	two independent DMA channels
	bus monitor
	software watchdog
	RISC controller for communication support
	LCD interface (MPC821 only)
	two (S)erial (M)anagement (C)ontrollers
	four (S)erial (C)ommunication (C)ontrollers (only tow with MPC821)
	four baud rate generators
	time slot assignor
	(T)ime (D)ivision (M)ultiplexed channel support
Dynamic RAM:	64/32/16 Mbyte ram area with 32 bit data bus
	fast page DRAM
Static RAM:	two 8 bit organized SO devices
	max. 1 Mbytes capacity
	16 bit data bus width
	data backup with gold capacitor or 5V Standby
Flash Memory:	two 16 bit organized TSOP devices
	4 Mbytes capacity (max. 8 Mbytes)
	32 bit data bus width
	single 5 volt programmable devices
EEPROM:	2 Kbyte I2C serial access device
IP-Module:	8MHz/32MHz Support
	two 16 bit slots for industry pack modules
	8/16 bit data memory cycle support
	8/16 bit data I/O cycle support
	8/16 bit data IAC cycle support
	32 Byte ID read cycle support
	two level interrupt support
Real Time Clock:	RTC-V3021 with time & date function
	backup function with onboard supply
Data backup:	short time backup via service free gold cap
	external backup via VMEbus standby line

Front panel Leds:	one user programmable led status led for processor RUN state
Front panel Keys:	RESET key for complete hardware reset Abort key on level 1
Interrupt handler:	7 level onboard interrupt handler 7 level VMEbus interrupt handler software programmable VMEbus interrupt mask
System controller:	VMEbus single level arbiter on Level 3 VMEbus System Clock Driver VMEbus Reset controller VMEbus BTO VMEbus Auto Slot 1 Detect Function
VMEbus interface:	according to ANSI/IEEE STD1014-1987
VMEbus master:	DTB A16/A24 -D8/D16 VMEbus address modifier support standard and short I/O addressing
VMEbus slave:	DTB A24 -D8/D16 programmable VMEbus shared access base address programmable VMEbus shared access window size
VMEbus mailbox:	DTB A16 -D8 programmable VMEbus shared access base address
VMEbus arbiter:	single level arbiter on level 3
VMEbus requester:	single level 2:1 pass requester **R**elease **W**hen **D**one or **R**elease **O**n **R**equest mode
VMEbus interrupter:	7 level & vector programmable interrupter

4.2 Addressmap IP860

Type	Base	End	MPC860	Select	Size	TA
Boot range (VMEbus)	$0000 0000	$007F FFFF	D0-D15	CS0	Word	external
Boot range (Flash Memory)	$0000 0000	$007F FFFF	D0-D31	CS0	LWRD	internal
DRAM	$0000 0000	$00FF FFFF	D0-D31	CS2	LWRD	internal
Flash Memory	$1000 0000	$107F FFFF	D0-D31	CS1	LWRD	internal
SRAM	$2000 0000	$200F FFFF	D0-D15	CS3	Word	internal
IP-Slot A, I/O-Select	$4000 0000	$4000 007F	D0-D15	CS5	Word	external
IP-Slot A, ID-Select	$4000 0080	$4000 00FF	D0-D15	CS5	Word	external
IP-Slot A, IACK-Vector 0	$4000 0100	$4000 0101	D0-D15	CS5	Word	external
IP-Slot A, IACK-Vector 1	$4000 0102	$4000 0103	D0-D15	CS5	Word	external
IP-Slot A, Memory Select	$4080 0000	$40FF FFFF	D0-D15	CS5	Word	external
IP-Slot B, I/O-Select	$4100 0000	$4100 007F	D0-D15	CS5	Word	external
IP-Slot B, ID-Select	$4100 0080	$4100 00FF	D0-D15	CS5	Word	external
IP-Slot A, IACK-Vector 0	$4100 0100	$4100 0101	D0-D15	CS5	Word	external
IP-Slot A, IACK-Vector 1	$4100 0102	$4100 0103	D0-D15	CS5	Word	external
IP-Slot B, Memory Select	$4180 0000	$41FF FFFF	D0-D15	CS5	Word	external
MPC860 internal RAM	$F100 0000	$F100 FFFF	D0-D31	---	LWRD	internal
Shared Access Addr.Reg.	$FC00 0000	$FC00 0001	D0-D7	CS4	Byte	internal
Mailbox Address Register	$FC00 0002	$FC00 0003	D0-D7	CS4	Byte	internal
VMEbus Int.Mask Register	$FC00 0004	$FC00 0005	D0-D7	CS4	Byte	internal
VMEbus Int.Status Register	$FC00 0006	$FC00 0007	D0-D7	CS4	Byte	internal
Local Int.Mask Register	$FC00 0008	$FC00 0009	D0-D7	CS4	Byte	internal
Local Int.Status Register	$FC00 000A	$FC00 000B	D0-D7	CS4	Byte	internal
Board Control Register	$FC00 000C	$FC00 000D	D0-D7	CS4	Byte	internal
Board Status Register	$FC00 000E	$FC00 000E	D0-D7	CS4	Byte	internal
VMEbus Interrupter Reg.	$FC00 0010	$FC00 0011	D0-D7	CS4	Byte	internal
VMEbus Int.Vector Reg.	$FC00 0012	$FC00 0013	D0-D7	CS4	Byte	internal
Clear Mailbox Int.Register	$FC00 0014	$FC00 0015	---	CS4	Byte	internal
Real Time Clock	$FC00 0016	$FC00 0017	D0-D7	CS4	Byte	internal
Mailbox	$FC00 0018	$FC00 0019	D0-D7	CS4	Byte	internal
Watchdog	$FC00 001A	$FC00 001B	---	CS4	Byte	internal
Board Revision Register	$FC00 001E	$FC00 001F	D0-D7	CS4	Byte	internal
VMEbus Standard Access	$FE00 0000	$FEFF FFFF	D0-D15	CS6	Word	external
VMEbus Short I/O Access	$FF00 0000	$FF7F FFFF	D0-D15	CS7	Word	external
VME IACK Access	$FF80 0000	$FF8F FFFF	D0-D15	CS7	Word	external

(LWRD = 32bit, Word = 16bit, Byte = 8bit)

The given values refer to the MicroSys factory initialization of the MPC860. Base address variations can be easily done by modifying the according CS registers of the MPC860. All subdecoded values cannot be changed by the user.

Select Line	Start	End	TA	Purpose
CS0 decoding range	$0000 0000	$007F FFFF	internal external	Boot range VMEbus or Flash Memory
CS1 decoding range	$1000 0000	$107F FFFF	internal	Flash Memory
CS2 decoding range	$0000 0000	$00FF FFFF	internal	DRAM
CS3 decoding range	$2000 0000	$200F FFFF	internal	SRAM
CS4 decoding range	$FC00 0000	$FC00 FFFF	internal	Control Register
CS5 decoding range	$4000 0000	$41FF FFFF	external	IP-Slot A & B
CS6 decoding range	$FE00 0000	$FEFF FFFF	external	VME Std.Access, (A24)
CS7 decoding range	$FF00 0000	$FFFF FFFF	external	VME Short Access, (A16) VME-IACK-Access
MPC860 internal	$F100 0000	$F100 FFFF		reserved

4.3 Endian Mode

All elements of the IP860 board work in big endian mode.

5. MPC860 PowerQUICC

The IP860 is controlled either by the communication processor MPC860 or the MPC821 from Motorola. The processor is comprised of three modules. The PowerPC CPU core, the system integration block and the communications processor. The external bus is supported with the dynamic bus sizing feature for 8 and 16 bit devices. The MPC860 clock is supplied by an external clock circuitry using 1:1 clock mode. For detailed information about the PowerQUICC, please refer to the MPC860 user's manual.

The following signals are supplied and controlled by the PowerQUICC and must be correctly programmed to ensure proper operation of the board.

1.) Boot Flash: CS0 chip select
       32 bit port size on data lines D0 to D31
       decoding range max. 512 MByte
       140ns access time, i.e. 6 waitstates at 50MHz
       internal TA generation

2.) Boot VMEbus: CS0 chip select
       16 bit port size on data lines D0 to D15
       decoding range max. 512 Mbytes
       TA generation from VMEbus

3.) FLASH Memory: CS1 chip select
       32 bit port size on data lines D0 to D31
       decoding range 512 Mbytes, A0-A6
       140ns access time, i.e. 6 waitstates at 50MHz
       internal TA generation

4.) DRAM : CS2 chip select
       QUICC internal address multiplex mode
       32 bit port size on data lines D0 to D31
       decoding range 512 Mbytes, A0-A6
       two 4Mx16 DRAMs, no parity
       or two 16Mx16 DRAMs, no parity
       60ns t(RAS) access time
       4096 refresh cycles within 64msec.
       internal TA generation

5.) SRAM Area: CS3 chip select
       16 bit port size on data lines D0 to D15
       decoding range 512 Mbytes, A0-A6
       70ns access time, i.e. 3 waitstates at 50MHz
       internal TA generation on MPC860 access
       shared access via VMEbus

6.) Board-Registers: CS5 chip select
8 bit port size on data lines D0 to D7
decoding range 512 Mbytes, A0-A6
2 waitstate read/write access
internal TA generation

7.) IP Modules: CS5 chip select
16 bit port size on data lines D0 to D15
decoding range 512 Mbytes, A0-A6
external TA generation

8.) VME A24 Access: CS6 chip select
16 bit port size on data lines D0 to D15
decoding range 512 Mbytes, A0-A6
external TA generation

9.) VME A16 Access: CS7 chip select
16 bit port size on data lines D0 to D15
decoding range 512 Mbytes, A0-A6
external TA generation

10.) VME-IACK-Cyc: CS7 chip select
16 bit port size on data lines D0 to D15
decoding range 512 Mbytes, A0-A6
external TA generation

11.) QUICC Module: Base Address Register at $F100 0000

12.) QUICC Clock: 50 MHz crystal oscillator

13.) LCD interface: (MPC821 only)
Support for both active and passive LCD panels

14.) QUICC ports: MPC860 provides 6 serial ports based on 4 SCCs and 2 SMCs.
These serial ports can be physically translated to various standards.
Special I/O-modules are available.

MPC821 provides 4 serial ports based on 2 SCCs and 2 SMCs.
Additional an LCD interface is available.

IP860 board can be used with both processors.
Use of the ports is selectable.

Port	available signals on MPC860	available signals on MPC821	EN	821	T	SAR
PA15	RxD1		x	x	x	x
PA14	TxD1		x	x	x	x
PA13	RxD2		x	x	x	x
PA12	TxD2		x	x	x	x
PA11	L1TxDB					x
PA10	L1RxDB					x
PA9	L1TxDA					x
PA8	L1RxDA					x
PA7	CLK1, L1RCLKA		x	x	x	x
PA6	CLK2		x	x	x	x
PA5	CLK3, L1TCLKA		x	x	x	x
PA4	CLK4		x	x	x	x
PA3	CLK5		x	x	x	x
PA2	CLK6, L1RCLKB		x	x	x	x
PA1	CLK7		x	x	x	x
PA0	CLK8		x	x	x	x
PB31	SPISEL*,REJECT1*		x	x	x	
PB30	SPICLK		x	x	x	
PB29	SPIMOSI		x	x	x	
PB28	SPIMISO, BRGO4		x	x	x	x
PB27	I2CSDA					
PB26	I2CCL					
PB25	SMTXD1					
PB24	SMRXD1					
PB23	SMSYS1*, SDACK1		x			
PB22	SMSYN2*, SDACK2		x			
PB21	SMTXD2, L1CLKOB		x	x	x	x
PB20	SMRXD2, L1CLKOA		x			x
PB19	RTS1*, L1ST1		x	x		
PB18	RTS2*, L1ST2		x	x		
PB17	L1RQB, L1ST3		x	x		x
PB16	L1RQA, L1ST4		x	x		x
PB15	BRGO3		x	x	x	x
PB14	RSTRT1*		x	x		

Port	available signals on MPC860	available signals on MPC821	EN	821	T	SAR
PC15	DREQ1, RTS1*, L1ST1		x	x	x	x
PC14	DREQ2, RTS2*, L1ST2		x	x	x	x
PC13	L1RQB, L1ST3					x
PC12	L1RQA, L1ST4					x
PC11	CTS1*		x	x	x	x
PC10	CD1		x	x	x	x
PC9	CTS2*		x	x	x	x
PC8	CD2		x	x	x	x
PC7	CTS3*,L1TSYNCB,SDACK2		x			
PC6	CD3, L1RSYNCB		x			
PC5	CTS4*,L1TSYNCA,SDACK1		x			
PC4	CD4, L1RSYNCA		x			
PD15	L1TSYNCA	LD8		x	x	x
PD14	L1RSYNCA	LD7		x	x	x
PD13	L1TSYNCB	LD6		x	x	x
PD12	L1RSYNCB	LD5		x	x	x
PD11	RxD3	LD4	x	x	x	x
PD10	TxD3	LD3	x	x	x	x
PD9	RxD4	LD2	x	x	x	x
PD8	TxD4	LD1	x	x	x	
PD7	RTS3*	LD0	x	x	x	x
PD6	RTS4*	LCD_AC, LOE	x	x	x	x
PD5	REJECT2	FRAME/VSYNC		x	x	x
PD4	REJECT3	LOAD/HSYNC		x	x	x
PD3	REJECT4	SHIFT/CLK		x	x	x
Spare4					x	
Spare3					x	
Spare2					x	
Spare1					x	
IRQ7					x	

☞ **For detailed chip information see**

Technical manual MPC860/821

6. Memory access

6.1 Boot possibilities

IP860 board may boot either from the onboard Flash memory or via an external VMEbus memory. The boot source can be selected by the jumper **ST14 pin 7-8**. If this link is open, the local flash memory must contain the valid boot firmware, otherwise the VMEbus is requested and the MPC860 accesses the address $00000100 within the standard VMEbus address range.

The boot area is controlled via the CS0 select line. The boot data port size is automatically configured for the 32 bit wide Flash memory or the 16 bit wide VMEbus.

After a power up reset, a manual reset or a hardware reset from the VMEbus, the onboard processor requests for the reset vector by driving the CS0 line along with the access address $00000100 active.

Boot-ROM Addressmap:

Address:	$100	first address after reset MSWord of pointer to programm start
	$102	LSWord of pointer to programm start
	$104	
	$106	

☞ **For detailed information about the boot specification please see,**
Technical manual MPC860/821

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6.2 SDRAM

The IP860 is able to carry either 16 Mbyte or 64 Mbyte of synchronous dynamic ram. The SDRAM is directly controlled by the MPC860 internal memory controller. The ram block consists of two 4Mx16 or two 16Mx16 organized SDRAM devices.

The MPC860 controls the DRAM bank via its control lines according to the following table. The ram data port is 32 bits wide and no parity check is performed. The DRAM area cannot be shared with other VMEbus masters.

MPC860	SDRAM	Description
CS2	CS	chip select line
GPL_A0#	A10/AP	address/auto precharge line
GPL_A1#	RAS	row address select line
GPL_A2#	CAS	column address select line
GPL_A3#	WE	write enable
BS_A(3-0)#	U/LDQM	byte enable lines
CLKOUT	CLK	clock line

☞ **For detailed information about the SDRAM chip specification, please refer to the according SDRAM data sheet.**

6.3 Flash Memory

The Flash memory area of the IP860 consists of two 3,3 volt TSOP/II devices, which allows for a total capacity of 4 Mbyte or 8 Mbyte. The data bus is 32 bits wide and no parity check is performed.

The IP860 can be either booted via the local flash memory or an external VMEbus memory. The boot select line CS0 is used for both purposes. No burst access must be performed on the CS0 access range. After the boot sequence has been performed via the CS0 line, the local flash memory can be accessed via CS1, the standard VMEbus range via the CS6 select line of the MPC860.

Any write access to the flash memory area affects both devices, because there are no separate byte or word write lines. The write cycle sequence is under full software/chip control and depends on the used chip types.

The flash memory can be protected by software and by hardware against unintended programming. After power up any write to the flash area is inhibited by hardware. The 'enable flash write' bit within the (B)oard (C)ontrol (R)egister at location CS4+$0C must be set to high to allow any write access to the flash area. All function bits of the BCR can be read back for verification.

BCR	CS4+$0C	D0	D1	D2	D3	D4	D5	D6	D7
function		LSLE	WDOG	FLWE	RWDN	---	---	---	USER
reset state		0	0	0	0	0	0	0	0
enable flash write				1					
disable flash write				0					

LSLE	IP-Slot long select enable	high = enable
WDOG	watchdog trigger port	high = enable
FLWE	flash write enable	high = write enable
RWDN	VMEbus requester release when done	high = RWDN
USER	user led control	high = led on

If the soldering link ST5 is closed, the flash contents is protected by hardware against any write accesses, no matter of the state of the FLWE bit.

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The (B)oard (S)status (R)egister at location CS4+$0E reflects the real state of write protect switch and the logically 'anded' flash ready/busy lines of both devices.

BSR	CS4+$0E	D0	D1	**D2**	**D3**	D4	D5	D6	D7
function		---	---	**FLWE**	**FLRY**	IPND	BTFL	VERS	ARBE
enable flash write				**1**					
disable flash write				**0**					
flash ready					**1**				
flash busy					**0**				

FLWE	flash write enable	high = write enable
FLRY	flash ready	high = ready
IPND	VMEbus interrupt pending	high = pending
BTFL	Boot flag	high = local
VERS	VMEbus enable always reset out line function	high = disable
ARBE	VMEbus arbiter enable	high = disable

☞ **For detailed chip information see**
Technical manual of Flash memory products.

6.4 Static RAM Area

The IP860 features two SRAM devices with either 128Kx8 or 512Kx8 capacity. This allows for a total SRAM capacity of 256 Kbyte or 1 Mbyte at a 16 bit wide data bus. If the smaller devices are installed, the soldering link ST9 must be set to position 1-2. The local decoding size and the base address depend on the programming of the CS3 select line of the MPC860. The data port is 16 bits wide and no parity check is performed. The whole SRAM area can be shared with other VMEbus masters. The onboard CS3 address decoding does **NOT** need to match with the address decoding for the VMEbus shared access address. The VMEbus access address is programmed within the (S)hared (A)ccess (R)egister at location CS4+$0. An additional VMEbus access enable bit is contained within the (M)ailbox (A)ccess (R)egister at location CS4+$02. The acknowledge generation for the SRAM bank is performed by external hardware.

The contents of the SRAM area is protected against data loss by a backup circuitry if solder link ST28 is set to position 1-2. The backup feature of the IP860 may be disabled by changing the solder link ST28 to position 2-3. The backup power is supplied either from a service free gold capacitor for short time backup, or, in case a long time backup is required, via the VMEbus standby line on ST1, row B, pin 31. The backup power is supplied to the SRAM area as well as to the onboard real time clock.

☞ **For detailed information about the SRAM chip specification,**

please refer to the according SRAM data sheet.

6.5 VMEbus Shared RAM Decoding

The whole SRAM area can be shared with other VMEbus masters. The VMEbus base address and the window size are software programmable within the (S)hared ram (A)cces (R)egister at location CS4+$0. The SAR contains 6 compare and 2 mask bits for the according VMEbus address lines. The shared ram access is only performed within the VMEbus standard access range if the enable bit within the (M)ailbox (A)ccess (R)egister at location CS4+$2 is set to high. The compare bits must match the desired binary access address image of the according VMEbus lines. The mask bits allow to ignore the given address bits, in case they are set to high. If a mask bit is set to high, the according compare bit is 'don't care'. Both registers are cleared after reset, i.e. the VMEbus access address range is set to $000000-$03FFFF, but the shared access is disabled. All programmable bits of both registers can be read back for verification. The local CS3 address decoding of the MPC860 for the SRAM area does not affect the shared access address in any way and may have any address location.

SAR	CS4+$00	D0	D1	D2	D3	D4	D5	D6	D7
function		CA23	CA22	CA21	CA20	CA19	CA18	MA19	MA18
reset state		0	0	0	0	0	0	0	0

CA(23-18)	shared ram address compare bits	state = VMEbus address bit
MA(19-18)	shared ram address mask bits	high = mask, low = compare

MAR	CS4+$02	D0	D1	D2	D3	D4	D5	D6	D7
function		CA15	CA14	CA13	CA12	CA11	---	---	EVSR
reset state		0	0	0	0	0	0	0	0

CA(15-11)	mailbox address compare bits	state = VMEbus address bit
EVSR	enable VMEbus shared ram	high = enable

Any shared ram access from the VMEbus side must be performed with the proper address modifier combination for a VMEbus standard user or supervisor data access.

7. Board Control

7.1 Reset Logic

During power up or power down sequences, the power monitor activates the board reset line and holds the IP860 in a defined state. The reset line will be active at least 200ms after the supply voltage reaches 4.65 volts. Below that voltage, the reset line will be continuously low. The reset key performs an equivalent reset sequence with an approximate reset time of 200ms. If the board is configured as system controller, the VMEbus reset line driver will be activated as well. The board reset function controls all onboard devices and logic with the exception of the board clock, the IP-Clock and VMEbus clock generation.

7.1.1 Reset Sources

MPC860 Reset Signals	Reset Source	Comment
PORESET	Power monitor & Reset Key	Power On reset
HRESET	Watchdog, Power monitor & VMESYSRES	Hardware reset
SRESET	JTAG/Debug port	Software reset

In addition the MPC860 may drive the HRESET and/or the SRESET. Both lines are open collector and might be driven by several sources.

HRESET resets the whole IP860 and, if the board is system controller or the link ST4 is intact, the whole VME-system. In debug mode the BDM-port is reset.

SRESET generated by the MPC860 will not affect any logic on IP860.

7.1.2 Reset Configuration

The MPC860 uses three reset configurations:

1.) Power On Reset: The MODCK1 and MODCK2 pins configure the clock source for the SPLL external 1:1 mode.
(MODCLK1 = 1 and MODCLK2 = 0)

2.) Hardware Reset: The hard reset configuration is sampled from the databus.
(RSTCONF signal is low)

MPC860 data line	Name	Reset Value	Description
D0	EARB	1	External arbitration
D1	IP	1	Initial interrupt prefix
D2	BBE	1 0	Boot device is burstable on boot from flash memory Boot device is not burstable on boot from VMEbus
D3	BDIS	0	Memory controller is enabled after reset
D4, 5	BPS	0, 0 1, 0	Boot port size is 32 bit on boot from flash memory Boot port size is 16 bit on boot from VMEbus selection is done by ST14 7-8
D7, 8	ISB	1, 0	Initial internal space base select set to $FF00 0000
D9, 10	DBGC	1, 1	enable AT0-3
D11, 12	DBPC	0, 0 0, 1	Debug port JTAG port

Only listed data lines are driven on HRESET for configuration. All other pins are driven low using low value pull-down resistors inside the MPC860.

ST14 7-8	open	boot from Flash memory
ST14 7-8	close	boot from VMEbus

Attention ! **Do not make any other connections on Connector ST14 !**

3.) Software Reset: During SRESET the background debug port is configured.
This occurs under the control of the development tool connected to the JTAG/Debug port.

7.2 Backup Feature

The backup feature of the IP860 is used to protect the **RTC** as well as the **SRAM** area. Both devices are connected to the MAX-691A, which controls the backup supply and the power up and down sequences to avoid unintended write pulses. The backup power is supplied by a service free gold capacitor. The RTC as well as the SRAM area cannot be disconnected from the backup power.

The **gold capacitor** allows for a service free short time backup without any battery or other time or temperature degrading parts. If the backup time should be extended, the backup power can be supplied via the VMEbus standby line on connector ST1A, pin 31. The external supply voltage should not exceed 5,25 volts and not fall below 2.5 volts to ensure correct data retention.

The power consumption table of all backup connected devices:

device:	max. current:	total:
MAX691A	5uA	5uA
RTC-V3021	5uA @ 2volts	5uA
KM684000ALG-5L	50uA @ 3volts	100uA

7.3 Watchdog Timer

The IP860 features a fixed rate hardware timer for watchdog purposes, which can be enabled by software. Once enabled, it only can be disabled by a hardware reset. The time out rate is set to 1.6 seconds and within that time at least one retrigger write access must be performed to reset the timer. The watchdog is enabled via the (B)oard (C)ontrol (R)egister at location CS4+$0C and re-triggered by the (W)atchdog (R)etrigger (R)egister at the location CS4+$1A. The time out sequence can be modified by additional hardware components on the SMD-0805 locations ST1 and ST2.

The timer rate is calculated according to the following table:

SMD-0805		watchdog timeout period		reset timeout period
ST1	ST2	normal	after power up	
ext.cap	low	(600/47pF x C)ms	(2.4/47pF x C)ms	(800/47pF x C)ms
low	open	100ms	1.6sec	200ms
open	open	1.6sec	1.6sec	200ms

BCR	**CS4+$0C**	D0	**D1**	D2	D3	D4	D5	D6	D7
function		LSLE	**WDOG**	FLWE	RWDN	---	---	---	USER
reset state		0	**0**	0	0	0	0	0	0
watchdog disabled			**0**						
watchdog enabled			**1**						

LSLE	IP-Slot long select enable	high = enable
WDOG	watchdog trigger port	high = enable
FLWE	flash write enable	high = write enable
RWDN	VMEbus requester release when done	high = RWDN
USER	user led control	high = led on

The watchdog must be re-triggered by accessing the (W)atchdog (T)rigger (R)egister at location CS4+$1A periodically within time-out period by a write command with any data contents. The default time-out period is set to 1,6 sec and can be . A time-out performs a hardware reset via the HWRST* line.

7.4 The Bus Timers

The IP860 provides 2 different bus timers for local and VMEbus accesses to insure that the current cycle will be terminated properly, in case the addressed device does not exist. The onboard bus timer with a time constant of about 16µs cannot be disabled and is contiguously active for any onboard access. The VMEbus timer has a time out rate of 32µs and is activated only, if the board is configured as system controller. If the IP860 is not system controller, the VMEbus timer function must be provided by the current system controller. Otherwise the IP860 may block the whole VMEbus system, if a non existing device will be accessed on the VMEbus. The timer rates can be modified within certain limits on request by a factory reprogramming of the IPC ispLSI.

8. Interrupt Structure

The IP860 offers a bit maskable 7 level VMEbus interrupt handler and a 5 source onboard interrupt structure. The 7 VMEbus interrupt levels work in vector controlled mode only, while the onboard interrupts do not support any vector. The interrupt priority structure of the VMEbus must be realized by software, i.e. by the use of mask and status register bits for each VMEbus interrupt level. The interrupt priorisation of all local interrupt sources can be freely handled according to the users demands.

Level	Source	Comment	Priority
IRQ0	reserved	not used	high
IRQ1	Abort-Key	IRAB	
IRQ2	reserved	not used	
IRQ3	VMEbus interrupt level 7-1	VIR7 - VIR1	
IRQ4	IP-module A IRQ0/1	IRA1, IRA0	
IRQ5	IP-module B IRQ0/1	IRB1, IRB0	
IRQ6	VMEbus-Mailbox & VMEbus-Sysfail	IRMB, VSYF	
IRQ7	reserved	not used	low

Each interrupt level can be individually enabled or disabled within the MPC860. Multiple interrupt sources on a single level can enabled within the according interrupt mask register for local or VMEbus interrupt sources. After reset, all mask registers are cleared an all interrupt sources are disabled. The actual state of each interrupt source can be detected within the two interrupt status registers for local and VMEbus interrupt sources. The interrupt status is not affected by the according enable bit and will be valid at any time.

8.1.1 The VMEbus Interrupt Handler

Each VMEbus interrupt level can be enabled or disabled by software via (V)MEbus (I)nterrupt (E)nable register at location CS4+$04. After a hardware reset all bits of this register are set to zero and all VMEbus interrupt levels are disabled. **To enable** a VMEbus interrupt level the according bit must be **set to high**. The register contents can be read back for verification.

VIE	**CS4+$04**	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		VIER7	VIER6	VIER5	VIER4	VIER3	VIER2	VIER1	VSFE
reset state		0	0	0	0	0	0	0	0
VME-Sysfail enable		x	x	x	x	x	x	x	1
VME-IRQ1 enable		x	x	x	x	x	x	1	x
VME-IRQ2 enable		x	x	x	x	x	1	x	x
VME-IRQ3 enable		x	x	x	x	1	x	x	x
VME-IRQ4 enable		x	x	x	1	x	x	x	x
VME-IRQ5 enable		x	x	1	x	x	x	x	x
VME-IRQ6 enable		x	1	x	x	x	x	x	x
VME-IRQ7 enable		1	x	x	x	x	x	x	x

All VMEbus interrupt lines share the MPC860 interrupt line IRQ3.

The current state of each VMEbus interrupt line can be checked within (V)MEbus (I)nterrupt (S)tatus register at location CS4+$05. The low active status of each interrupt line is valid at any time, no matter if the according interrupt line is enabled or not.

VIS	**CS4+$06**	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		VIRQ7	VIRQ6	VIRQ5	VIRQ4	VIRQ3	VIRQ2	VIRQ1	VSYF
VME-Sysfail active		x	x	x	x	x	x	x	1
VME-IRQ1 active		x	x	x	x	x	x	1	x
VME-IRQ2 active		x	x	x	x	x	1	x	x
VME-IRQ3 active		x	x	x	x	1	x	x	x
VME-IRQ4 active		x	x	x	1	x	x	x	x
VME-IRQ5 active		x	x	1	x	x	x	x	x
VME-IRQ6 active		x	1	x	x	x	x	x	x
VME-IRQ7 active		1	x	x	x	x	x	x	x

The necessary VMEbus acknowledge procedure must be performed by a **read** access within the address range from $FF800000 to $FF8FFFFF of **CS7** decoded area. This range works as a 16 bit device with an **external** acknowledge. The data byte transferred on the data line D7 to D0 during the acknowledge cycle can be used to distinguish between different interrupt sources on the same VMEbus interrupt level. The upper byte from D15 to D8 does not contain valid data during the **byte sized** acknowledge read cycle on odd VMEbus addresses. In order to meet the VMEbus specifications, the necessary acknowledge cycles must be performed according to following table.

VMEbus Interrupt Acknowledge Access Address Overview:

IACK for level	VA3	VA2	VA1	Access Address	Command
VME-IRQ1	0	0	1	$FF80 0003	Byte Read
VME-IRQ2	0	1	0	$FF80 0005	Byte Read
VME-IRQ3	0	1	1	$FF80 0007	Byte Read
VME-IRQ4	1	0	0	$FF80 0009	Byte Read
VME-IRQ5	1	0	1	$FF80 000B	Byte Read
VME-IRQ6	1	1	0	$FF80 000D	Byte Read
VME-IRQ7	1	1	1	$FF80 000F	Byte Read

8.1.2 The Onboard Interrupt Handler

There are five local interrupt sources onboard the IP860. Each source can be enabled or disabled individually by software within the (L)ocal (I)nterrupt (E)nable register at location CS4+$08. The current status of all local interrupt sources can be checked within (L)ocal (I)nterrupt (S)tatus register at location CS4+$0A. After a hardware reset all bits of the enable register are set to zero and all local interrupt sources are disabled. **To enable** an interrupt source the according bit must be **set to high**. The register contents can be read back for verification.

LIE	CS4+$08	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		IEAB	---	---	IEMB	IEB1	IEB0	IEA1	IEA0
reset state		0	0	0	0	0	0	0	0
IP-A-IRQ0 enable		x	x	x	x	x	x	x	1
IP-A-IRQ0 disable		x	x	x	x	x	x	x	0
IP-A-IRQ1 enable		x	x	x	x	x	x	1	x
IP-A-IRQ1 disable		x	x	x	x	x	x	0	x
IP-B-IRQ0 enable		x	x	x	x	x	1	x	x
IP-B-IRQ0 disable		x	x	x	x	x	0	x	x
IP-B-IRQ1 enable		x	x	x	x	1	x	x	x
IP-B-IRQ1 disable		x	x	x	x	0	x	x	x
Mailbox IRQ enable		x	x	x	1	x	x	x	x
Mailbox IRQ disable		x	x	x	0	x	x	x	x
Abort Key enable		1	x	x	x	x	x	x	x
Abort Key disable		0	x	x	x	x	x	x	x

The current state of each local interrupt source can be checked within the (L)ocal (I)nterrupt (S)tatus register at location CS4+$0A. The status of each interrupt line is valid at any time, no matter if the according interrupt line is enabled or not.

LIS	**CS4+$0A**	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		IRAB	---	---	IRMB	IRB1	IRB0	IRA1	IRA0
IP-A-IRQ0 active		x	x	x	x	x	x	x	1
IP-A-IRQ1 active		x	x	x	x	x	x	1	x
IP-B-IRQ0 active		x	x	x	x	x	1	x	x
IP-B-IRQ1 active		x	x	x	x	1	x	x	x
Mailbox IRQ active		x	x	x	1	x	x	x	x
Abort Key active		1	x	x	x	x	x	x	x

8.1.3 The VMEbus Interrupter

The IP860 supports an interrupt generation on all 7 VMEbus interrupt levels. The vector must be loaded into the write only (V)MEbus (I)nterrupt (V)ector register located at CS4+$12. A read attempt of the VIV will not destroy the register contents. The desired level can be programmed via the (V)MEbus (I)nterrupt (C)ontrol register at location CS4+$10 according to the following table. The VIC register can be read back for verification.

The interrupt sequence is started by a state change from high to low of the STVI signal within the VIC register. Only if the STVI line is set to low the current state of the interrupt sequence can be checked within the (B)oard (S)tatus (R)egister at location CS4+$0E. If the bit is read high, the VMEbus interrupt is still pending and it has not been acknowledged by a VMEbus interrupt handler. The pending bit is forced immediately to low if the STVI line is released to a high state. A new interrupt sequence can only be started by a new transition of the STVI line from high to low. A contiguous low level of the STVI line will not cause several interrupts to be emitted. If level 0 is selected within the VIC register, the complete sequence can be processed without any active VMEbus interrupt. This might be of advantage for selftest purposes or to initialize the pending bit to a desired state.

VIC	CS4+$10	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		STRB	STRA	IP32	---	STVI	IL3	IL2	IL1
reset state		0	0	0	0	0	0	0	0
Start VME Interrupter		x	x	x	x	1->0	x	x	x
Interrupter level bits		x	x	x	x	x	binary code level		
IP-Clock 8MHz		x	x	0	x	x	x	x	x
IP-Clock 32MHz		x	x	1	x	x	x	x	x
IP-Strobe Line A = 0		x	0	x	x	x	x	x	x
IP-Strobe Line A = 1		x	1	x	x	x	x	x	x
IP-Strobe Line B = 0		0	x	x	x	x	x	x	x
IP-Strobe Line B = 1		1	x	x	x	x	x	x	x

VIV	CS4+$12	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		VIV0	VIV1	VIV2	VIV3	VIV4	VIV5	VIV6	VIV7

The contents of the VIV register is not defined after a power up reset and may have any state !

Note: Bitnumbering from MPC860 and VMEbus is opposite!

BSR	CS4+$0E	D0	D1	D2	D3	**D4**	D5	D6	D7
function		---	---	FLWE	FLRY	**IPND**	BTFL	VERS	ARBE
VMEbus IRQ pending						**1**			
VMEbus IRQ finished						**0**			

FLWE	flash write enable	high = write enable
FLRY	flash ready	high = ready
IPND	VMEbus interrupt pending	high = pending
BTFL	Boot flag	high = local
VERS	VMEbus enable always reset out line function	high = disable
ARBE	VMEbus arbiter enable	high = disable

Bit map of the VMEbus interrupter level:

VIC	IL3	IL2	IL1
disable:	0	0	0
Level 1:	0	0	1
Level 2:	0	1	0
Level 3:	0	1	1
Level 4:	1	0	0
Level 5:	1	0	1
Level 6:	1	1	0
Level 7:	1	1	1

VIV	CS4+$12	D0	D1	D2	D3	D4	D5	D6	D7
write only		MSB - LSB							
VME-Data Lines		VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0

Programming example:

```
                          ┌─────────────┐
                          │  check:     │
                          │  STVI       │
                          └─────────────┘
                          ↙            ↘
               ┌─────────┐          ┌─────────┐
               │  low    │          │  high   │
               └─────────┘          └─────────┘
                    ↙                     │
         ┌──────────────────┐            │
    ┌───→│  check:          │            │
    │    │  IPND            │            │
    │    └──────────────────┘            │
    │       ↙          ↘                 │
    │  ┌────────┐   ┌────────┐          │
    │  │  high  │   │  low   │──────────┤
    │  └────────┘   └────────┘          │
    │       │                           ↓
    │  ┌──────────────┐          ┌──────────────┐
    └──│  increment   │          │  load vector │
       │  time out    │          └──────────────┘
       └──────────────┘          ┌──────────────┐
              │                   │  set level   │
              ↓                   └──────────────┘
       ┌──────────────┐          ┌──────────────┐
       │  error       │          │ set STVI high│
       │  exit        │          └──────────────┘
       └──────────────┘          ┌──────────────┐
                                 │ set STVI low │
                                 └──────────────┘
                                        │
                                        ↓
                                 ┌──────────────┐
                                 │  exit        │
                                 └──────────────┘
```
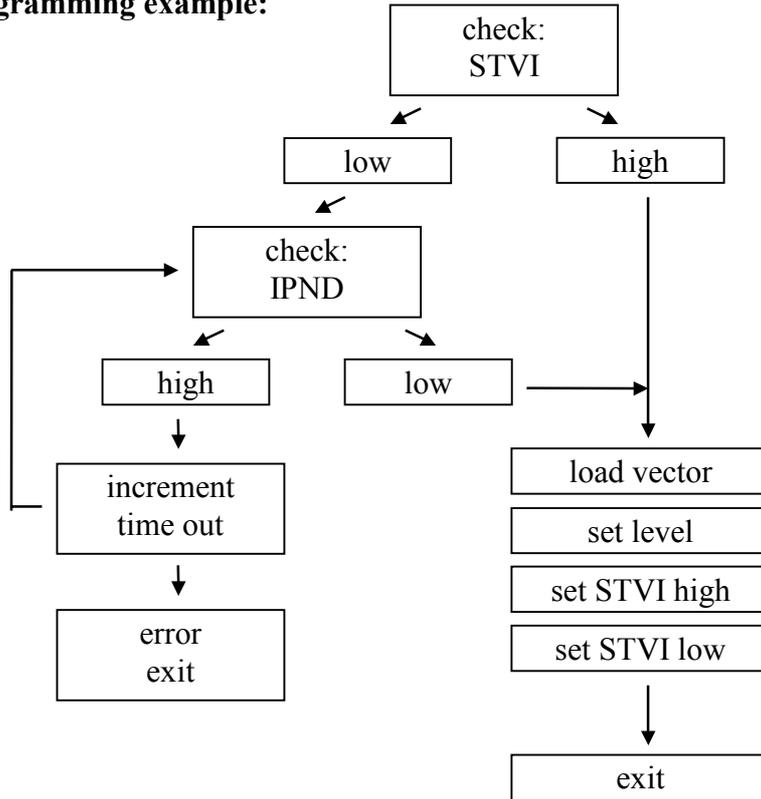
9. The VMEbus Interface

The VMEbus interface of the IP860 is designed according to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297. The VMEbus connector ST1 rows A, B and C contain all standard VMEbus lines, necessary for A16/A24, D8/D16 master/slave boards. All unused daisy chain lines are linked through, i.e. no external bypass links are necessary. The address modifier signals AM5 to AM0 are part of the VMEbus specification and serve to differentiate between certain memory areas. All address modifier lines are necessary for the shared access decoding logic. The IP860 accepts slave data accesses within the VMEbus standard and VMEbus short access area.

The following AM-Codes are accepted by the IP860:

AM5	AM4	AM3	AM2	AM1	AM0	Access	
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low   H = logical high

The following AM-Codes are generated by the IP860:

AM5	AM4	AM3	AM2	AM1	AM0	Access	
H	H	H	H	H	L	Standard Supervisory Prog.	(3E)
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	H	L	Standard User Prog.	(3A)
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low   H = logical high

9.1 Pin Assignment of the VMEbus Connector ST1

Pin	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	UDS*	BR0*	SYSRESET*
13	LDS*	BR1*	LWORD*
14	RW*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	not connected	A17
22	IACKOUT*	not connected	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	5VSTB	+12V
32	+5V	+5V	+5V

(signals enclosed in brackets are not used and left open)

9.2 VMEbus Requester

The IP860 contains a single level 2:1 pass requester with (**R**)elease (**W**)hen (**D**)one or a single level (**R**)elease (**O**)n (**R**)equest mode. The RWD requester releases the VMEbus mastership after the completion of each bus cycle and it has to request for it for every following VMEbus cycle. The ROR method releases the VMEbus only, if the current VMEbus cycle have been completed and any other device in the VMEbus system requests for the bus mastership. If there are no other requests, the ROR requester remains being busmaster even if it does not access the VMEbus.

The **RWD** method is enabled by setting the corresponding bit in the (B)oard (C)ontrol (R)egister.

BCR	CS4+$0C	D0	D1	D2	**D3**	D4	D5	D6	D7
function		LSLE	WDOG	FLWE	**RWDN**	---	---	---	USER
reset state		0	0	0	**0**	0	0	0	0
Release On Request					**0**				
Release When Done					**1**				

LSLE	IP-Slot long select enable	high = enable
WDOG	watchdog trigger port	high = enable
FLWE	flash write enable	high = write enable
RWDN	VMEbus requester release when done	high = RWDN
USER	user led control	high = led on

9.3 The VMEbus Arbiter

The IP860 is equipped with a single level VMEbus requester on level 3. This allows the board to work as VMEbus controller as well as a bus slave in any combination.

The VMEbus arbiter features the auto-slot-1-detection according to the VME64 specification, if the link ST7 is not installed. **In case the IP860 is booted from VMEbus, the auto-slot-1-detection is not recommended, because the detection takes at least 40ms, which forces the MPC860 into time out**. If ST7 is installed, the VMEbus arbiter function is always enabled. This link or the auto-slot-1-detection activates all other system controller functions according to following table.

VMEbus Signal	Slot 1 Function	Driver Type	not Slot 1 Function
System Clock	Output	Totem Pole	Tristate
System Reset	Input/Output	Open Drain	Input
Bus Error	Input/Output	Open Drain	Input
Bus Grant In 3	Input/Output	Totem Pole	Input

Please make sure, that only **one** system controller is enabled within a VMEbus system at a time, usually located in the leftmost slot. The use of more that one system controller will lead to improper operation and may cause permanent damage.

The actual slot state of the IP860 can be detected within the (B)oard (S)tatus (R)egister at location CS4+$0E. If the according bit is read to low, the IP860 has either detected slot 1 or the link ST7 is installed to enable the VMEbus arbiter.

BSR	CS4+$0E	D0	D1	D2	D3	D4	D5	D6	**D7**
function		---	---	FLWE	FLRY	IPND	BTFL	VERS	**ARBE**
not VMEbus slot 1									**1**
VMEbus slot 1									**0**

FLWE	flash write enable	high = write enable
FLRY	flash ready	high = ready
IPND	VMEbus interrupt pending	high = pending
BTFL	Boot flag	high = local
VERS	VMEbus enable always reset out line function	high = disable
ARBE	VMEbus arbiter enable	high = disable

9.3.1 Preparations for VMEbus Multiprocessing

In case a VMEbus system should be configured for more than one VMEbus master, the user must verify, that only **one** system controller is enabled in the whole system. The system controller is usually located in the leftmost slot and drives the bus grant in lines of slot 1. It supplies the system with the system clock, the system reset, and optionally the bus error and the bus clear information. All these lines, with the exception of the system reset and the bus error signal, are totem pole outputs and **must** be controlled **only** by the system controller within the VMEbus system. The system reset and the bus error lines are driven by open collector circuits and might be driven by more than one board.

9.4 VMEbus-Reset

The VMEbus reset line will be automatically driven by the IP860 as system controller, i.e. the link ST7 is closed. In case this link is open and the auto-slot-1 function is used, the reset line will only be driven if the link ST4 is closed. Because the VMEbus reset line must be driven by open collector circuits, it is allowed to be driven by more than one board within the system. If the ST4 is closed, the reset line will always be driven, even if the auto-slot-1 function has detected the slave status.

9.5 VMEbus Mailbox Feature

The IP860 offers a bi-directional 8 bit register for processor communication. This register might be used for purposes, like process communication and synchronization in multiprocessor applications. Therefore, the individual interrupt generation on each VMEbus board without using the limited VMEbus interrupt lines is a basic feature for an effective system structure. A local interrupt o level 6 will be generated, if a write access within the VMEbus short I/O range to the mailbox access address is performed. The mailbox area within the short I/O range covers 1KByte address space. If a read access is performed to the given address, no interrupt will be caused. The mailbox consists of a read only and a write only register for each side, the VMEbus and the local CPU. Any 8 bit value, written by the local CPU to the access address CS4+$18, can be read on the VMEbus side at the programmed access address. The data, written on the VMEbus side of the mailbox, can be read by the local CPU at the access address CS4+$18 and, if enabled, an interrupt is caused. The VMEbus side of the mailbox accepts short I/O user or supervisor data accesses only. The contents of the mailbox is not defined after power up and may have any value.

The mailbox data structure:

local side	D0	D1	D2	D3	D4	D5	D6	D7
VMEbus	VMED7	VMED6	VMED5	VMED4	VMED 3	VMED2	VMED 1	VMED0

The VMEbus short I/O access address must be loaded into the (M)ailbox (A)ddress (R)egister located at CS4+$02.

MAR	CS4+$02	D0	D1	D2	D3	D4	D5	D6	D7
function		CA15	CA14	CA13	CA12	CA11	---	---	EVSR
reset state		0	0	0	0	0	0	0	0

CA(15-11)	mailbox address compare bits	state = VMEbus address bit
EVSR	enable VMEbus shared ram	high = enable

The interrupt source must be enabled within the MPC860 and the (L)ocal (I)nterrupt (E)nable register at location CS4+$08.

LIE	CS4+$08	D0	D1	D2	**D3**	D4	D5	D6	D7
register bit name		IEAB	---	---	**IEMB**	IEB1	IEB0	IEA1	IEA0
reset state		0	0	0	**0**	0	0	0	0
IP-A-IRQ0 enable		x	x	x	x	x	x	x	1
IP-A-IRQ0 disable		x	x	x	x	x	x	x	0
IP-A-IRQ1 enable		x	x	x	x	x	x	1	x
IP-A-IRQ1 disable		x	x	x	x	x	x	0	x
IP-B-IRQ0 enable		x	x	x	x	x	1	x	x
IP-B-IRQ0 disable		x	x	x	x	x	0	x	x
IP-B-IRQ1 enable		x	x	x	x	1	x	x	x
IP-B-IRQ1 disable		x	x	x	x	0	x	x	x
Mailbox IRQ enable		x	x	x	**1**	x	x	x	x
Mailbox IRQ disable		x	x	x	**0**	x	x	x	x
Abort Key enable		1	x	x	x	x	x	x	x
Abort Key disable		0	x	x	x	x	x	x	x

The current interrupt status of the mailbox can be detected within the (L)ocal (I)nterrupt (S)tatus register at location CS4+$0A.

LIS	CS4+$0A	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		IRAB	---	---	IRMB	IRB1	IRB0	IRA1	IRA0
IP-A-IRQ0 active		x	x	x	x	x	x	x	1
IP-A-IRQ1 active		x	x	x	x	x	x	1	x
IP-B-IRQ0 active		x	x	x	x	x	1	x	x
IP-B-IRQ1 active		x	x	x	x	1	x	x	x
Mailbox IRQ active		x	x	x	1	x	x	x	x
Abort Key active		1	x	x	x	x	x	x	x

10. IndustryPack Option

The IP860 offers two (I)ndustry(P)ack module slots according to the VITA Specification Revision 1.0.e.0 for IP modules. The front end of the IP module slots is connected to two 50 pin SCSI/2 connectors. The IP860 supports all kind of single or double IP modules with 8 or 16 bit wide data bus and a module clock rate of 8 MHz or 32 MHz. IO-Cycles are supported without DMA mode. All interrupt sources of each module slot are forwarded to the onboard interrupt handler. Both module A interrupt lines use the local level 4 and both interrupt lines of module B use level 5. The interrupt priority of the two lines of each slot must be handled by software.

The IP-Module interrupt sources must be enabled within the (L)ocal (I)nterrupt (E)nable register located at CS4+$08.

LIE	CS4+$08	D0	D1	D2	D3	**D4**	**D5**	**D6**	**D7**
register bit name		IEAB	---	---	IEMB	**IEB1**	**IEB0**	**IEA1**	**IEA0**
reset state		0	0	0	0	**0**	**0**	**0**	**0**
IP-A-IRQ0 enable		x	x	x	x	x	x	x	**1**
IP-A-IRQ0 disable		x	x	x	x	x	x	x	**0**
IP-A-IRQ1 enable		x	x	x	x	x	x	**1**	x
IP-A-IRQ1 disable		x	x	x	x	x	x	**0**	x
IP-B-IRQ0 enable		x	x	x	x	x	**1**	x	x
IP-B-IRQ0 disable		x	x	x	x	x	**0**	x	x
IP-B-IRQ1 enable		x	x	x	x	**1**	x	x	x
IP-B-IRQ1 disable		x	x	x	x	**0**	x	x	x
Mailbox IRQ enable		x	x	x	1	x	x	x	x
Mailbox IRQ disable		x	x	x	0	x	x	x	x
Abort Key enable		1	x	x	x	x	x	x	x
Abort Key disable		0	x	x	x	x	x	x	x

The current interrupt status of the IP-Module interrupt lines can be detected within the (L)ocal (I)nterrupt (S)tatus register at location CS4+$0A.

LIS	CS4+$0A	D0	D1	D2	D3	**D4**	**D5**	**D6**	**D7**
register bit name		IRAB	---	---	IRMB	**IRB1**	**IRB0**	**IRA1**	**IRA0**
IP-A-IRQ0 active		x	x	x	x	x	x	x	**1**
IP-A-IRQ1 active		x	x	x	x	x	x	**1**	x
IP-B-IRQ0 active		x	x	x	x	x	**1**	x	x
IP-B-IRQ1 active		x	x	x	x	**1**	x	x	x
Mailbox IRQ active		x	x	x	1	x	x	x	x
Abort Key active		1	x	x	x	x	x	x	x

The strobe function of each slot can be controlled by the (V)MEbus (I)nterrupt (C)ontrol register at location CS4+$10. The error report lines of both slots are not supported and tied to high. All slot lines not used or input to the IP860, are tied to a high level by 10K pull-up resistors. The module using the connectors ST21, ST16 and ST18 will have the extension A in the following description. The IP module with the extension 'B' uses the connectors ST22, ST17 and ST19. The DSUB connectors ST21 and ST22, which contain the I/O interface signals are located on an IPAxx adapter board, which allows different I/O connection facilities.

VIC	CS4+$10	**D0**	**D1**	D2	D3	D4	D5	D6	D7
register bit name		**STRB**	**STRA**	IP32	---	STVI	IL3	IL2	IL1
reset state		**0**	**0**	0	0	0	0	0	0
Start VME Interrupter		x	x	x	x	1->0	x	x	x
Interrupter level bits		x	x	x	x	x	binary code level		
IP-Clock 8MHz		x	x	0	x	x	x	x	x
IP-Clock 32MHz		x	x	1	x	x	x	x	x
IP-Strobe Line A = 0		x	**0**	x	x	x	x	x	x
IP-Strobe Line A = 1		x	**1**	x	x	x	x	x	x
IP-Strobe Line B = 0		**0**	x	x	x	x	x	x	x
IP-Strobe Line B = 1		**1**	x	x	x	x	x	x	x

The component mounting height underneath IP module area is realized below 3mm (0.11inch) to allow for a good air flow between the carrier board and the I-Packs.

Each slot is supplied with ID-, I/O- and memory select lines, controlled by the CS5 select line of the MPC860 with external TA generation according to following table.

Attention: Following D0-D15 and A0-A31 correspond to MPC860 bit ordering (bit 0 = MSB). PD15-PD0 and PA23- PA0 correspond to VITA conventions for IP modules.

The MPC860 internal decoding must be programmed within the CS5 select registers according to the following addressing limitations:

- The address lines A0 to A6 must be programmed as base address
- IP-Module A is selected, if the address line A7 is decoded low.
- IP-Module B is selected, if the address line A7 is decoded high.
- Both Memory-Select ranges decode the address line A8 always as high.
- Both I/O- & ID-Select ranges decode the address line A8 always as low.
- Both I/O-Select ranges decode the address line A24 always as low.
- Both ID-Select ranges decode the address line A24 always as high.

Address map of IP-Module-A

Select Line	Start address	End address	Data Lines	Address Lines	Function
I/O	$40000000	$4000007F	D0-D15 (CPU) PD15-PD0	A25-A30 (CPU) PA6-PA1	read/write
ID	$40000080	$400000FF	D8-D15 (CPU) PD7-PD0	A26-A30 (CPU) PA5-PA1	read only
IACK-Vector 0	$4000 0100	$4000 0101	D8-D15 (CPU) PD7-PD0	A30 (CPU) PA1	read only
IACK-Vector 1	$4000 0102	$4000 0103	D8-D15 (CPU) PD7-PD0	A30 (CPU) PA1	read only
Memory	$40800000	$40FFFFFF	D0-D15 (CPU) PD15-PD0	A9-A30 (CPU) PA22-PA1	read/write

Address map of IP-Module- B

Select Line	Start address	End address	Data Lines	Address Lines	Function
I/O	$41000000	$4100007F	D0-D15 (CPU) PD15-PD0	A25-A30 (CPU) PA6-PA1	read/write
ID	$41000080	$410000FF	D8-D15 (CPU) PD7-PD0	A26-A30 (CPU) PA5-PA1	read only
IACK-Vector 0	$4100 0100	$4100 0101	D8-D15 (CPU) PD7-PD0	A30 (CPU) PA1	read only
IACK-Vector 1	$4100 0102	$4100 0103	D8-D15 (CPU) PD7-PD0	A30 (CPU) PA1	read only
Memory	$41800000	$41FFFFFF	D0-D15 (CPU) PD15-PD0	A9-A30 (CPU) PA22-PA1	read/write

10.1 IP Slot Specific Parameters:

The data lanes of the IP slots are handled via both data strobes according to following table:

IP data lanes	IP data strobe	IP A1	CPU A30	CPU A31	CPU Address	CPU data lanes
PD15-PD8	LDS	0	0	0	$0	D0-D7
PD7-PD0	UDS	0	0	1	$1	D8-D15
PD15-PD8	LDS	1	1	0	$2	D0-D7
PD7-PD0	UDS	1	1	1	$3	D8-D15

10.2 Pin assignment of logical interface ST18 and ST19

DSUB Connector Pin: **Signal Name:**

Pin		Pin		Signal	Signal
1		26		Ground	Ground
	2		27	Clock	+5V/1A
3		28		Reset	R/W*
	4		29	D0	ID-Select*
5		30		D1	DMA-Request 0* (pull up)
	6		31	D2	Memory-Select*
7		32		D3	DMA-Request 1* (pull up)
	8		33	D4	Int.-Select*
9		34		D5	DMA-Acknowledge* (pull up)
	10		35	D6	I/O-Select*
11		36		D7	(reserved 0) (pull up)
	12		37	D8	A1
13		38		D9	DMA-End* (pull up)
	14		39	D10	A2
15		40		D11	(Error*) (pull up)
	16		41	D12	A3
17		42		D13	IRQ0* (pull up)
	18		43	D14	A4
19		44		D15	IRQ1* (pull up)
	20		45	LDS*	A5
21		46		UDS*	Strobe
	22		47	-12V	A6
23		48		+12V	Acknowledge* (pull up)
	24		49	+5V/1A	(reserved 1) (pull up)
25		50		Ground	Ground

Signals within brackets are not used !

An '*' indicates a low active signal.

The layout of the pin numbers within this table corresponds with the physical placement of the pins on the 50 pin IP connectors.

10.3 Pin assignment of I/O connectors ST17/18 to ST21/22

The 50 pin DSUB I/O connectors ST17 and ST18 of both modules are connected one to one to the 50 DIN 41651 connectors ST21 and ST22, i.e. DSUB pin 1 connects wrap connector pin 1 and DSUB pin 50 connects wrap connector pin 50.

Physical Layout of
DSUB Connector ST5/ST6

Physical Layout of
Flatcable connector ST7/ST8

1		26	
	2		27
3		28	
	4		29
5		30	
	6		31
7		32	
	8		33
9		34	
	10		35
11		36	
	12		37
13		38	
	14		39
15		40	
	16		41
17		42	
	18		43
19		44	
	20		45
21		46	
	22		47
23		48	
	24		49
25		50	

1	26
2	27
3	28
4	29
5	30
6	31
7	32
8	33
9	34
10	35
11	36
12	37
13	38
14	39
15	40
16	41
17	42
18	43
19	44
20	45
21	46
22	47
23	48
24	49
25	50

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11. Special Function

11.1 Real Time Clock

The IP860 is equipped with the RTC-V3021, which features time and date. The RTC is protected against data loss by a backup circuitry. The backup power can be either supplied from a service-free gold capacitor for short time backup or, for extended backup times, by the VMEbus standby line on ST1B pin 31.

The RTC-V3021 can be accessed by the (R)eal (T)ime (C)lock register at location CS4+$16. The RTC works with a four wire interface and a transfer protocol for serial devices. Each of the four control lines can be individually programmed within the RTC register. The data out value is driven to the RTC device only if CS and WR are set active. In all other cases, the data read on the D-I/O line is driven by the RTC or set to high by a pull-up resistor. The register contents can be read back for verification and it is cleared during power up and hardware reset.

RTC	CS4+$16	D0	D1	D2	D3	D4	D5	D6	D7
function		---	---	---	---	CS	RD	WR	D-I/O
reset state		0	0	0	0	0	0	0	1

CS	chip select line	high = active
RD	read line	high = active
WR	write line	high = active
D-I/O	data input / output line	state = data value

For detailed programming information and chip description, please refer to RTC-V3021 User's Manual !

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11.2 Serial EEPROM

The IP860 offers a 2 Kbyte EEPROM for storing system or board parameters. The device is handled via the SDA and SCL lines of the MPC860 on its port pins PB[26] and PB[27].

☞ **For detailed programming information and chip description, please refer to Data Sheet XICOR X24C16 !**

12. Communication Ports

12.1 Serial Communication ports

The six serial ports of the IP860 are based on 4 SCCs and 2 SMCs of the MPC860. In case the MPC821 processor is used, 2 SCCs are replaced by the LCD interface.

The two SMCs are directly accessible with RS232 EIA interface standard via two 6 pin molex connectors behind the front panel. All SCC port pins of the MPC860 are directly available in TTL level on the 50 pin DSUB I/O extension connector ST20. By a signal conditioning module out of the IE36x series, these lines can be transferred to nearly any EIA standard, f.e. RS232, RS422, RS485, 10BaseT or AUI. The IE36x module replaces the IP-Module-A, which can not be used in this case.

12.2 The I/O-Extension Connector

Depending on the processor (MPC860 or MPC821) the connection is different due to the different use of processor IO-ports.

Pin		860EN	821	860T	860SAR
1		GND	GND	GND	GND
	2	VCC	VCC	VCC	VCC
3		PA15	PA15	PA15	PA15
	4	PA14	PA14	PA14	PA14
5		PC11	PC11	PC11	PC11
	6	PC15	PC15	PC15	PC15
7		PC10	PC10	PC10	PC10
	8	PA13	PA13	PA13	PA13
9		PA12	PA12	PA12	PA12
	10	PC9	PC9	PC9	PC9
11		PC14	PC14	PC14	PC14
	12	PC8	PC8	PC8	PC8
13		PB31	PB31	PB31	PA11
	14	PB30	PB30	PB30	PA10
15		PB29	PB29	PB29	PA9
	16	PB28	PB28	PB28	PB28
17		PB19	PB19	Spare4	PC13
	18	PB18	PB18	Spare3	PC12
19		PB17	PB17	Spare2	PB17
	20	PB16	PB16	Spare1	PB16
21		PB15	PB15	PB15	PB15
	22	PB14	PB14	IRQ7	PA8
23		- 12V	- 12V	- 12V	- 12V
	24	+ 12V	+ 12V	+ 12V	+ 12V
25		GND	GND	GND	GND

Pin		860EN	821	860T	860SAR
26		GND	GND	GND	GND
	27	VCC	VCC	VCC	VCC
28		PD11	PD11	PD11	PD11
	29	PD10	PD10	PD10	PD10
30		PC7	PD15	PD15	PD15
	31	PD7	PD7	PD7	PD7
32		PC6	PD14	PD14	PD14
	33	PD9	PD9	PD9	PD9
34		PD8	PD8	PD8	PB20
	35	PC5	PD13	PD13	PD13
36		PD6	PD6	PD6	PD6
	37	PC4	PD12	PD12	PD12
38		PA7	PA7	PA7	PA7
	39	PA6	PA6	PA6	PA6
40		PA5	PA5	PA5	PA5
	41	PA4	PA4	PA4	PA4
42		PA3	PA3	PA3	PA3
	43	PA2	PA2	PA2	PA2
44		PA1	PA1	PA1	PA1
	45	PA0	PA0	PA0	PA0
46		PB20	PD3	PD3	PD3
	47	PB21	PB21	PB21	PB21
48		PB22	PD4	PD4	PD4
	49	PB23	PD5	PD5	PD5
50		GND	GND	GND	GND

12.3 PLSI programming port

The programmable logic onboard the IP860 can be modified or updated via a PC controlled programming interface. The ISP programming port contains the necessary lines for serial a programming of all ispLSI devices.

Pin	Name	Type	Description
1	VCC		+5V
2	ISPSDO	out	data out from ispLSI daisy chain
3	ISPSDI	in / PU	serial data in
4	ISPEN	in / PU	programming enable to ispLSI
5	---		nc
6	ISPMODE	in / PD	mode pin for ispLSI
7	GND		
8	ISPCLK	in / PD	serial clock, (second function BOOTselect with jumper to pin 7)

No connection **MUST** be made by the user to these programming signals. Otherwise a non user recoverable malfunction or permanent damage might be caused. The programming port can only be used together with a special ispLSI programming interface.

12.4 Debug port

The IP860 offers a debug port for JTAG access and background debugging for the MPC860 processor. All signals are accessible via the 15 pin Molex connector ST26.

Pin	Name	Type	Description
1	VFLS0	pullup	MPC860 debug signal, Visible Instruction Queue Flush Status 0
2	BRST*	pullup	debug reset input controls MPC860 SRESET line
3	GND		ground line
4	TCK	pulldown	JTAG clock input / debug clock input
5	GND		ground line
6	VFLS1	pullup	MPC860 debug signal, Visible Instruction Queue Flush Status 1
7	HRST*	pullup	MPC860 HRESET output line
8	TDI	pulldown	JTAG data input / debug serial data input
9	VDD		3,3V supply voltage
10	TDO		JTAG data output / debug serial data output
11	JTAG	pullup	JTAG enable input, if high, JTAG function is selected, if connected to ground BDM port function is enabled
12	TCK	pulldown	JTAG clock input
13	TMS	pullup	JTAG mode select input
14	TRST*	pullup	JTAG reset input
15	GND		ground line

12.5 Adapter Cable for BDM Interface

Pin 15 — Connection Pin 11 to Pin15

10 wire Ribbon Cable

Pin 1 — Pin 1

15 Pin Molex Connector — 10 Pin male Ribbon Connector
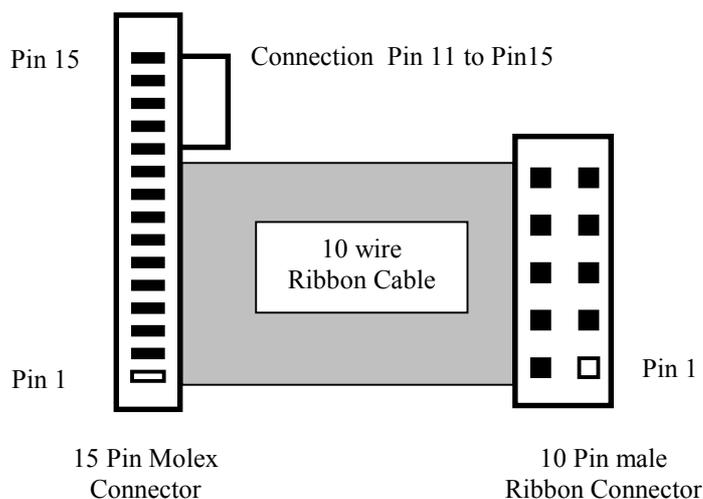
13. Front panel

The front panel realized with this board is based on the IPA02 board. It connects the 50 lines of each module to two 50 pin SCSI/2 connectors for flat cable mounting. Additionally, the IPA02 offers a reset switch with integrated led and an abort key with integrated led. Other cable connectors can be realized by different IPAxx adapter boards.

13.1 Front Panel Layout
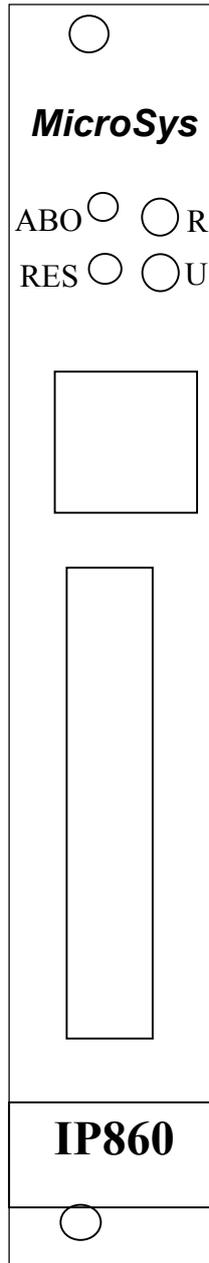
13.2 Front Panel Leds

Led1: USER

This led is activated if data bit D7 within the BCR at location CS4+$0C is set to high. After power up or hardware reset, the register is cleared and the led is switched off.

Led2: RUN

This led is switched on by TS transitions of the MPC860, i.e. it indicates active external CPU cycles. If the MPC860 works completely inside its internal cache memory, the run led will go off.

13.3 Front Panel Switches

RESet**:**

The reset key performs a hardware reset for the whole board, and if the board is system controller or the soldering link ST4 is set, to the whole VMEbus system.

ABOrt**:**

The Abort key performs an interrupt on level 1 within the MPC860 interrupt structure.

13.4 Front Panel Connectors

The standard IPA02 front end of the IP860 is fitted out with several connectors, which are partly hidden behind the front panel. The direct accessible 50 pin connector ST22 refers to the I/O interface connector ST17 of IP-Slot B. The hidden 50 pin connector ST22 refers to either the I/O interface connector ST16 of the IP-Slot A or the I/O extension piggyback, which fits into connector ST18 and ST20. The two hidden Molex connectors ST23 and ST24 are used for the two serial SMC I/O ports of the MPC860.

Pin assignment of the Molex connector ST23:

Pin:	Signal:	Description:	
1	TXD0	SMC channel 0 transmit data	RS232 EIA Standard
2	RXD0	SMC channel 0 receive data	RS232 EIA Standard
3	GND	ground	
4	nc		
5	nc		
6	nc		

Pin assignment of the Molex connector ST24:

Pin:	Signal:	Description:	
1	TXD1	SMC channel 1 transmit data	RS232 EIA Standard
2	RXD1	SMC channel 1 receive data	RS232 EIA Standard
3	GND	ground	
4	nc		
5	nc		
6	nc		

Pin assignment of RJ45 connector ST25:

Pin:	Signal:	Description:	IP Connector ST16
1	TX+	10BaseT TX(+)-signal	IOA4 (44)
2	TX-	10BaseT TX(-)-signal	IOA3 (43)
3	RX+	10BaseT RX(+)-signal	IOA8 (48)
4	---	connected to pin 5, 75R resistor to Shield	
5	---	connected to pin 4	
6	RX-	10BaseT RX(-)-signal	IOA7 (47)
7	---	connected to pin 8, 75R resistor to Shield	
8	---	connected to pin 7	

Note!

The above described network signals are only valid if an IE363 TP module
is mounted!
If any different IE or IP module is mounted on IP slot A (ST16, ST18 and ST20)
the pins 1, 2, 3 and 6 of connector ST25 are defined by the mounted module!

14. Register Set Overview

14.1 Shared Access Register

SAR	CS4+$00	D0	D1	**D2**	**D3**	D4	D5	D6	D7
function		CA23	CA22	CA21	CA20	CA19	CA18	MA19	MA18
reset state		0	0	0	0	0	0	0	0

CA(23-18)	shared ram address compare bits	state = VMEbus address bit
MA(19-18)	shared ram address mask bits	high = mask, low = compare

14.2 Mailbox Access Register

MAR	CS4+$02	D0	D1	D2	D3	D4	D5	D6	D7
function		CA15	CA14	CA13	CA12	CA11	---	---	EVSR
reset state		0	0	0	0	0	0	0	0

CA(15-11)	mailbox address compare bits	state = VMEbus address bit
EVSR	enable VMEbus shared ram	high = enable

14.3 VMEbus Interrupt Enable Register

VIE	CS4+$04	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		VIER7	VIER6	VIER5	VIER4	VIER3	VIER2	VIER1	VSFE
reset state		0	0	0	0	0	0	0	0
VME-Sysfail enable		x	x	x	x	x	x	x	1
VME-IRQ1 enable		x	x	x	x	x	x	1	x
VME-IRQ2 enable		x	x	x	x	x	1	x	x
VME-IRQ3 enable		x	x	x	x	1	x	x	x
VME-IRQ4 enable		x	x	x	1	x	x	x	x
VME-IRQ5 enable		x	x	1	x	x	x	x	x
VME-IRQ6 enable		x	1	x	x	x	x	x	x
VME-IRQ7 enable		1	x	x	x	x	x	x	x

14.4 VMEbus Interrupt Status Register

VIS	CS4+$06	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		VIRQ7	VIRQ6	VIRQ5	VIRQ4	VIRQ3	VIRQ2	VIRQ1	VSYF
VME-Sysfail active		x	x	x	x	x	x	x	1
VME-IRQ1 active		x	x	x	x	x	x	1	x
VME-IRQ2 active		x	x	x	x	x	1	x	x
VME-IRQ3 active		x	x	x	x	1	x	x	x
VME-IRQ4 active		x	x	x	1	x	x	x	x
VME-IRQ5 active		x	x	1	x	x	x	x	x
VME-IRQ6 active		x	1	x	x	x	x	x	x
VME-IRQ7 active		1	x	x	x	x	x	x	x

14.5 Local Interrupt Enable Register

LIE	CS4+$08	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		IEAB	---	---	IEMB	IEB1	IEB0	IEA1	IEA0
reset state		0	0	0	0	0	0	0	0
IP-A-IRQ0 enable		x	x	x	x	x	x	x	1
IP-A-IRQ0 disable		x	x	x	x	x	x	x	0
IP-A-IRQ1 enable		x	x	x	x	x	x	1	x
IP-A-IRQ1 disable		x	x	x	x	x	x	0	x
IP-B-IRQ0 enable		x	x	x	x	x	1	x	x
IP-B-IRQ0 disable		x	x	x	x	x	0	x	x
IP-B-IRQ1 enable		x	x	x	x	1	x	x	x
IP-B-IRQ1 disable		x	x	x	x	0	x	x	x
Mailbox IRQ enable		x	x	x	1	x	x	x	x
Mailbox IRQ disable		x	x	x	0	x	x	x	x
Abort Key enable		1	x	x	x	x	x	x	x
Abort Key disable		0	x	x	x	x	x	x	x

14.6 Local Interrupt Status Register

LIS	CS4+$0A	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		IRAB	---	---	IRMB	IRB1	IRB0	IRA1	IRA0
IP-A-IRQ0 active		x	x	x	x	x	x	x	1
IP-A-IRQ1 active		x	x	x	x	x	x	1	x
IP-B-IRQ0 active		x	x	x	x	x	1	x	x
IP-B-IRQ1 active		x	x	x	x	1	x	x	x
Mailbox IRQ active		x	x	x	1	x	x	x	x
Abort Key active		1	x	x	x	x	x	x	x

14.7 Board Control Register

BCR	CS4+$0C	D0	D1	D2	D3	D4	D5	D6	D7
function		LSLE	WDOG	FLWE	RWDN	---	---	---	USER
reset state		0	0	0	0	0	0	0	0
user led on		x	x	x	x	x	x	x	1
user led off		x	x	x	x	x	x	x	0
release when done		x	x	x	1	x	x	x	x
release on request		x	x	x	0	x	x	x	x
enable flash write		x	x	1	x	x	x	x	x
disable flash write		x	x	0	x	x	x	x	x
watchdog enabled		x	1	x	x	x	x	x	x
watchdog disabled		x	0	x	x	x	x	x	x
IP long select enable		1	x	x	x	x	x	x	x
IP short select enable		0	x	x	x	x	x	x	x

LSLE	IP-Slot long select enable	high = enable
WDOG	watchdog trigger port	high = enable
FLWE	flash write enable	high = write enable
RWDN	VMEbus requester release when done	high = RWDN
USER	user led control	high = led on

14.8 Board Status Register

BSR	CS4+$0E	D0	D1	D2	D3	D4	D5	D6	D7
function		---	---	FLWE	FLRY	IPND	BTFL	VERS	ARBE
auto-slot-1 enable		x	x	x	x	x	x	x	1
VMEbus Slot 1 enable		x	x	x	x	x	x	x	0
VMEbus Reset on Slot 1		x	x	x	x	x	x	1	x
VMEbus Reset enable		x	x	x	x	x	x	0	x
VMEbus boot enable		x	x	x	x	x	1	x	x
local flash boot enable		x	x	x	x	x	0	x	x
VMEbus IRQ pending		x	x	x	x	1	x	x	x
VMEbus IRQ ready		x	x	x	x	0	x	x	x
flash ready		x	x	x	1	x	x	x	x
flash busy		x	x	x	0	x	x	x	x
enable flash write		x	x	1	x	x	x	x	x
disable flash write		x	x	0	x	x	x	x	x

FLWE	flash write enable	high = write enable
FLRY	flash ready	high = ready
IPND	VMEbus interrupt pending	high = pending
BTFL	Boot flag	high = local
VERS	VMEbus enable always reset out line function	high = disable
ARBE	VMEbus arbiter enable	high = disable

14.9 VMEbus Interrupt Control Register

VIC	**CS4+$10**	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		STRB	STRA	IP32	---	STVI	IL3	IL2	IL1
reset state		0	0	0	0	0	0	0	0
Start VME Interrupter		x	x	x	x	1->0	x	x	x
Interrupter level bits		x	x	x	x	x	binary code level		
IP-Clock 8MHz		x	x	0	x	x	x	x	x
IP-Clock 32MHz		x	x	1	x	x	x	x	x
IP-Strobe Line A = 0		x	0	x	x	x	x	x	x
IP-Strobe Line A = 1		x	1	x	x	x	x	x	x
IP-Strobe Line B = 0		0	x	x	x	x	x	x	x
IP-Strobe Line B = 1		1	x	x	x	x	x	x	x

14.10 VMEbus Interrupt Vector Register

VIV	**CS4+$12**	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		VIV0	VIV1	VIV2	VIV3	VIV4	VIV5	VIV6	VIV7

14.11 Clear Mailbox Interrupt Register

CMI	**CS4+$14**	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		---	---	---	---	---	---	---	---

14.12 Real Time Clock Register

RTC	CS4+$16	D0	D1	D2	D3	D4	D5	D6	D7
function		---	---	---	---	CS	RD	WR	D-I/O
reset state		0	0	0	0	0	0	0	1

CS	chip select line	high = active
RD	read line	high = active
WR	write line	high = active
D-I/O	data input / output line	state = data value

14.13 Local Mailbox Read Register

LMR	CS4+$18	D0	D1	D2	D3	D4	D5	D6	D7
VMEbus side		VD7	VD6	VD5	VD4	VD 3	VD2	VD 1	VD0

14.14 Local Mailbox Write Register

LMW	CS4+$18	D0	D1	D2	D3	D4	D5	D6	D7
VMEbus side		VD7	VD6	VD5	VD4	VD 3	VD2	VD 1	VD0

14.15 Watchdog Retrigger Register

WRR	CS4+$1A	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		---	---	---	---	---	---	---	---

14.16 Board Revision Register

WRR	CS4+$1E	D0	D1	D2	D3	D4	D5	D6	D7
register bit name		MEM2	MEM1	MEM0	CLK2	CLK1	CLK0	REV1	REV0

REV bits contain hardware revision

CLK bits show CPU clock frequency
   000 = 50MHz, 001 = 80MHz, 010 = 66MHz

MEM bits show SDRAM size
   000 = 16MB, 001 = 32MB, 010 = 64MB

e.g.   0x22 = 32MB, 50MHz, Rev. 2

15. Summary of Jumper & Switches

Described function is valid, when jumper is set or link is closed!

| Size:	Name:	Default	Position:	Function:
1x2	ST1	#	open close	MAX691A OSC IN open MAX691A OSC IN on GND
1x2	ST2	#	open close	MAX691A OSC SEL open MAX691A OSC SEL on GND
1x2	ST3	#	open close	IPC clock source 64 MHz oscillator IPC clock source 2 x system clock
1x2	ST4	#	open close	enable VMEbus reset line driver if ST7 is closed enable VMEbus reset line driver always
1x2	ST5	#	open close	Flash write enabled Flash write protected
1x2	ST7	#	close open	IP860 is VMEbus Controller *) IP860 is **not** VMEbus Controller
1x3	ST9	 #	1-2 2-3	SRAM Pin 30 = PA18 SRAM Pin 30 = VCC
1x3	ST10	#	1-2 2-3	SMRXD (port B20) connected to RS232 SMRXD (port B20) connected to Centronics
1x8	ST14	#	open 7-8	boot from onboard Flash boot from VMEbus
1x3	ST15	#	1-2 2-3	16 Mbyte DRAM 64 Mbyte DRAM
1x3	ST27	#	1-2 2-3	16 Mbyte DRAM 64 Mbyte DRAM
1x3	ST28	#	1-2 2-3	SRAM Pin 32 = VCB (Backup enabled) SRAM Pin 32 = VCC (Backup disabled)

*) ST7 must be set when booting from VMEbus!

Jumper setting for different processor types

Jumper		860EN	821	860T	860SAR
ST8		close	---	---	---
ST38		---	---	---	---
ST39		close	close	close	---
ST29		close	close	---	---
ST30		---	---	close	---
ST31		---	---	---	close
ST32		close	close	---	---
ST33		---	---	close	---
ST34		---	---	---	close
ST35		close	close	---	---
ST36		---	---	close	---
ST37		---	---	---	close

Appendices

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![MicroSys logo — Made for Professionals]
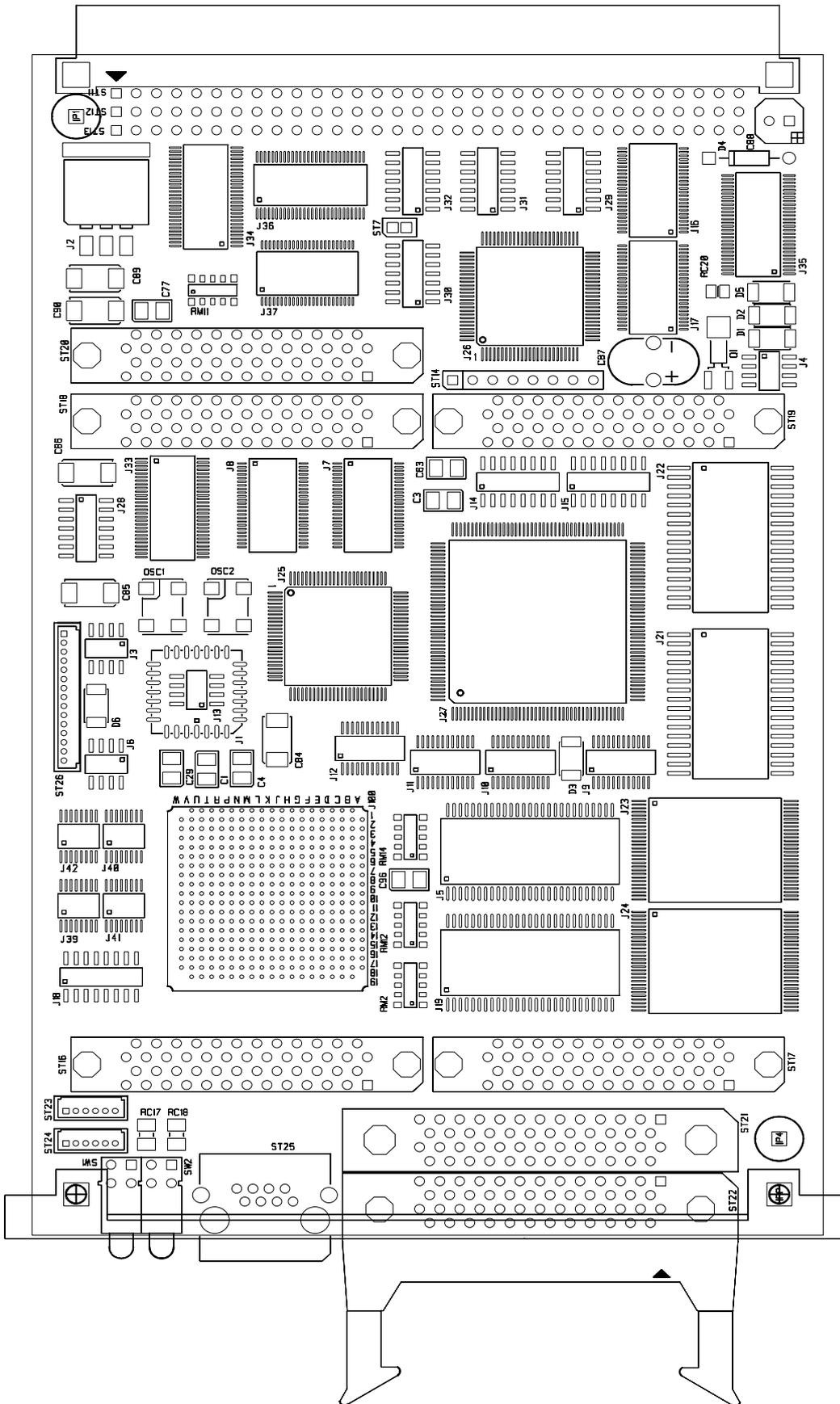
# Appendix B: Layout IP860 Solder Side
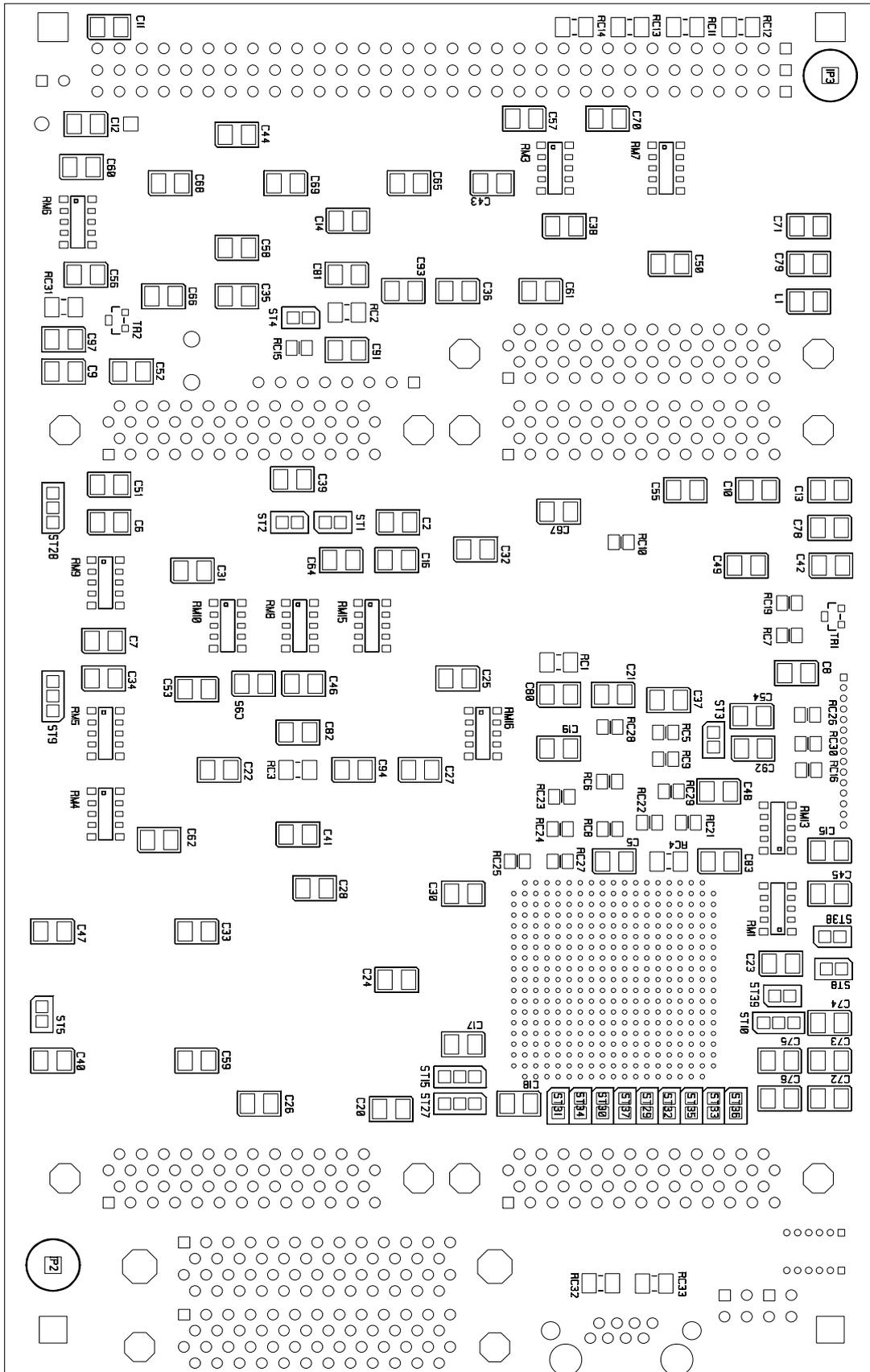
Appendix C: The IE361/IE363 Extension Boards

The IP860 supports a lot of port signals for the SCC, Ethernet and parallel ports which are available on connector ST20. The special interface boards IE36X are designed to buffer these signals and connect them to the output connectors ST16 and ST21. These adapter boards can be mounted on the second IP slot on IP860.

The IE361 piggyback offers 4 sockets for MicroSys I/O modules to buffer the 4 SCC channels of the MPC860 processor with various serial line drivers (e.g. RS232, RS422 or RS485) and a centronics compatible interface.

The IE363 is similar to the IE361 piggyback, but has a built in Ethernet twisted pair interface for the SCC1. A version for AUI Ethernet is also available. The centronics interface and the I/O module connectors for the serial channels SCC2 to SCC4 are the same as on IE361.

Mounting I/O Modules on IE36X

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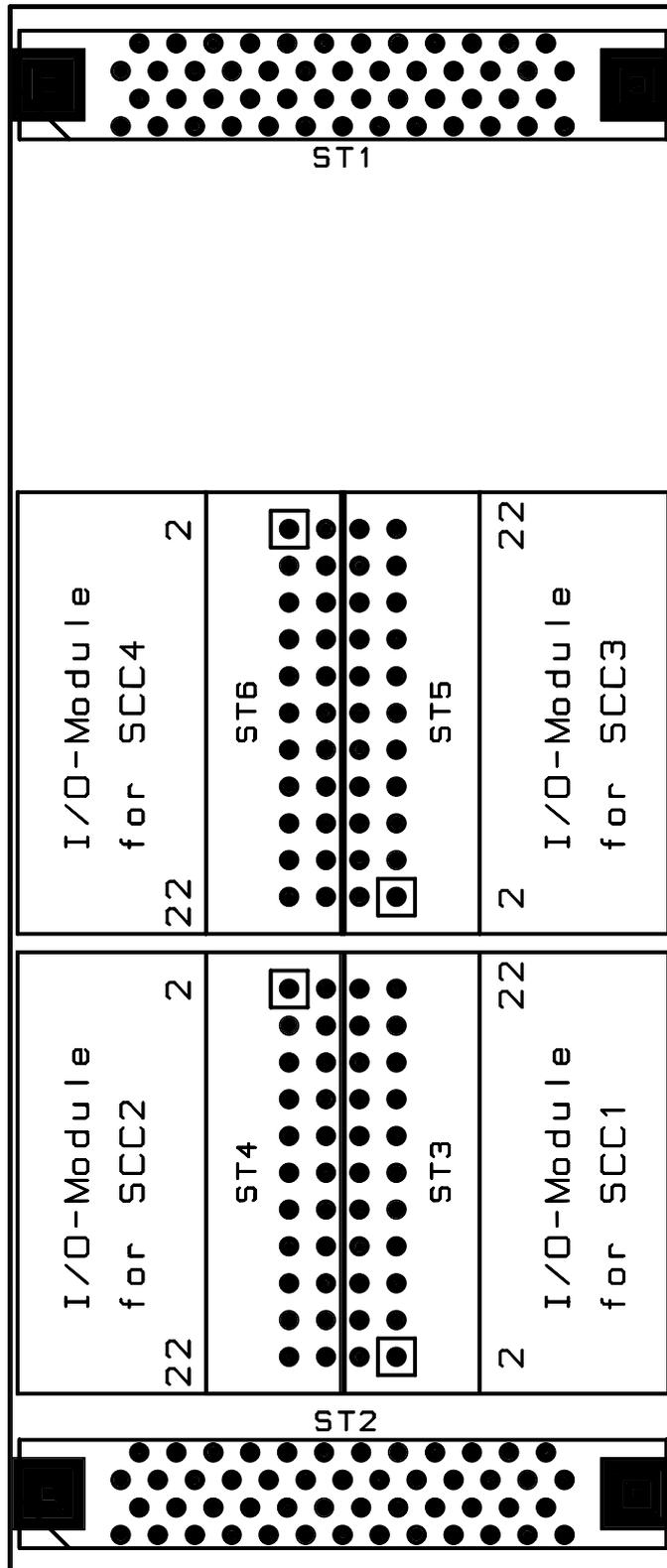
Pin Configuration of ST21 with IE361

Pin	Signal	Signal	Pin	
1	Strobe	D0	2	
3	D1	D2	4	
5	D3	D4	6	**Centronics**
7	D5	D6	8	
9	D7	ACK	10	
11	Busy	GND	12	
13	GND		14	
15		CTS4	16	**SCC4** (RS232)
17	TxD4	RTS4	18	
19	RxD4		20	
21	DCD4	GND	22	
23			24	
25	CTS3	TxD3	26	**SCC3** (RS232)
27	RTS3	RxD3	28	
29		DCD3	30	
31	GND		32	
33		CTS2	34	**SCC2** (RS232)
35	TxD2	RTS2	36	
37	RxD2		38	
39	DCD2	GND	40	
41			42	
43	CTS1	TxD1	44	**SCC1** (RS232)
45	RTS1	RxD1	46	
47		DCD1	48	
49	+12V	GND	50	not used

Example for RS422 pin configuration (also for IE363)

Pin	Signal	Signal	Pin	
13	GND	CTS4+14		
15	TxD4+CTS4-		16	**SCC4** (RS422)
17	TxD4-	RTS4-	18	
19	RxD4-	RTS4+20		
21	RxD4+	GND	22	
23	CTS3+TxD3+24			
25	CTS3-	TxD3-	26	**SCC3** (RS422)
27	RTS3-	RxD3-	28	
29	RTS2+RxD3+	30		

Pin Configuration of ST21 with IE363 (TP-Interface)

Pin	Signal	Signal	Pin	
1	Strobe	D0	2	
3	D1	D2	4	
5	D3	D4	6	**Centronics**
7	D5	D6	8	
9	D7	ACK	10	
11	Busy	GND	12	
13	GND		14	
15		CTS4	16	**SCC4**
17	TxD4	RTS4	18	
19	RxD4		20	
21	DCD4	GND	22	
23			24	
25	CTS3	TxD3	26	**SCC3**
27	RTS3	RxD3	28	
29		DCD3	30	
31	GND		32	
33		CTS2	34	**SCC2**
35	TxD2	RTS2	36	
37	RxD2		38	
	DCD2	----	40	
41	----	----	42	
43	TxD-	TxD+	44	**TP-Interface**
45	----	----	46	
47	RxD-	RxD+	48	
49	+12V	----	50	

Pin Configuration of ST7 with IE363 (AUI-Interface)

Pin	Signal	Signal	Pin	
39		GND	40	(Pin 40 = Pin 1 of 15pin DSUB)
41	COL-	COL+	42	
43	TxD-	TxD+	44	**AUI-Interface**
45	GND	GND	46	
47	RxD-	RxD+	48	
49	+12V	GND	50	

Layout IE363 Component side
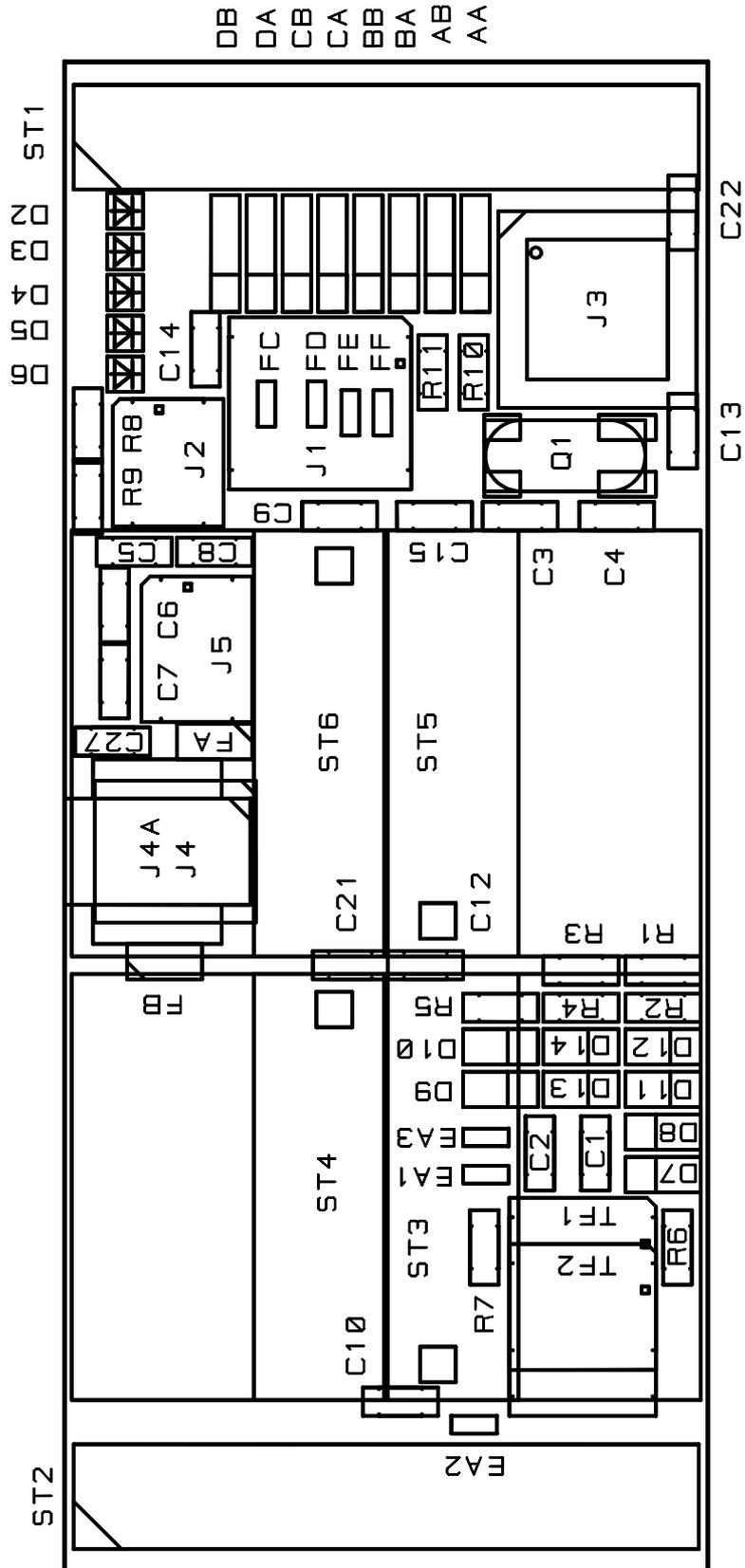
Jumpers and LEDs on IE36X

Size	Jumper	Position		Function	
1x3	AA	1-2		RxC connected to SCC1 I/O module pin 10	
	AA	2-3	*	CTS connected to SCC1 I/O module pin 10	
1x3	AB	1-2		TxC connected to SCC1 I/O module pin 14	IE361 only
	AB	2-3	*	RTS connected to SCC1 I/O module pin 14	
1x3	BA	1-2		RxC connected to SCC2 I/O module pin 10	
	BA	2-3	*	CTS connected to SCC2 I/O module pin 10	
1x3	BB	1-2		TxC connected to SCC2 I/O module pin 14	
	BB	2-3	*	RTS connected to SCC2 I/O module pin 14	
1x3	CA	1-2		RxC connected to SCC3 I/O module pin 10	
	CA	2-3	*	CTS connected to SCC3 I/O module pin 10	
1x3	CB	1-2		TxC connected to SCC3 I/O module pin 14	
	CB	2-3	*	RTS connected to SCC3 I/O module pin 14	
1x3	DA	1-2		RxC connected to SCC4 I/O module pin 10	
	DA	2-3	*	CTS connected to SCC4 I/O module pin 10	
1x3	DB	1-2		TxC connected to SCC4 I/O module pin 14	
	DB	2-3	*	RTS connected to SCC4 I/O module pin 14	
1x2	EA1	1-2		connects GND to AUI	**)
1x2	EA2	1-2		connects GND to AUI	**)
1x2	EA3	1-2		connects GND to AUI	**)

* means default setting

**) installed on AUI Version
**) not installed on Twisted
Pair Version

LEDs:

D2	LED red	Twisted pair link polarity	
D3	LED green	Twisted pair link integrity	
D4	LED red	Collision	IE363 only
D5	LED green	Receive data	
D6	LED yellow	Transmit data	