Chapter 3

Sequential Logic Design
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Figure 3.2 Bistable operation of cross-coupled inverters
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Figure 3.4 Bistable states of SR latch
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<table>
<thead>
<tr>
<th>Case</th>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>$\bar{Q}$</th>
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<tbody>
<tr>
<td>IV</td>
<td>0</td>
<td>0</td>
<td>$Q_{prev}$</td>
<td>$\bar{Q}_{prev}$</td>
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<tr>
<td>I</td>
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<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>II</td>
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</tr>
<tr>
<td>III</td>
<td>1</td>
<td>1</td>
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<table>
<thead>
<tr>
<th>CLK</th>
<th>D</th>
<th>$Q_{prev}$</th>
<th>Q</th>
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<tbody>
<tr>
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</tbody>
</table>

$Q = CLK \cdot D + \overline{CLK} \cdot Q_{prev}$

N1 = $CLK \cdot D$

N2 = $CLK \cdot Q_{prev}$
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\[ T_c = 9.5 \text{ ns} \]
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Figure M 02
UNN Figure 1