Chapter 4

Hardware Description Languages
Figure 4.1 Simulation waveforms
Figure 4.2 Synthesized circuit
Figure 4.3  inv synthesized circuit
Figure 4.4 gates synthesized circuit
Figure 4.5 and8 synthesized circuit
Figure 4.6 mux2 synthesized circuit
Figure 4.7 mux4 synthesized circuit
Figure 4.8 fulladder synthesized circuit
Figure 4.9  tristate synthesized circuit
Figure 4.10 Example simulation waveforms with delays (from the ModelSim simulator)
Figure 4.11  mux4 synthesized circuit
Figure 4.12  mux2 synthesized circuit
Figure 4.13  mux2_8 synthesized circuit
Figure 4.14 flop synthesized circuit
Figure 4.15 flopr synthesized circuit (a) asynchronous reset, (b) synchronous reset
Figure 4.16 flopenr synthesized circuit
Figure 4.17 Synchronizer circuit
Figure 4.18 sync synthesized circuit
Figure 4.19  latch synthesized circuit
Figure 4.20  sevenseg synthesized circuit
Figure 4.21 decoder3_8 synthesized circuit
Figure 4.22 priority CKT synthesized circuit
Figure 4.23 priority_casez synthesized circuit
Figure 4.24  syncbad synthesized circuit
Figure 4.25 priority_casez synthesized circuit
Figure 4.26  patternMoore synthesized circuit
Figure 4.27  patternMealy synthesized circuit
Figure 4.28 and23 synthesized circuit
Figure 4.29 mux4_12 synthesized circuit
Figure 4.30 andN synthesized circuit
0800. Anton started.

1000. Shoppe - Anton.  

1300. MP - MC.  

1800. PO - 2.13067645.  

1900. Relay 6.2 in OSS field speed test - now tack.  

1525. Started cosine tape (Sine check).  

1545. Started multi adder test.  

1545. Relay 70 Panel F. (Moth) in relay.  

First actual case of bug being found.  

1700. Crowd down.
UNN Figure 1