Chapter 8

Memory Systems

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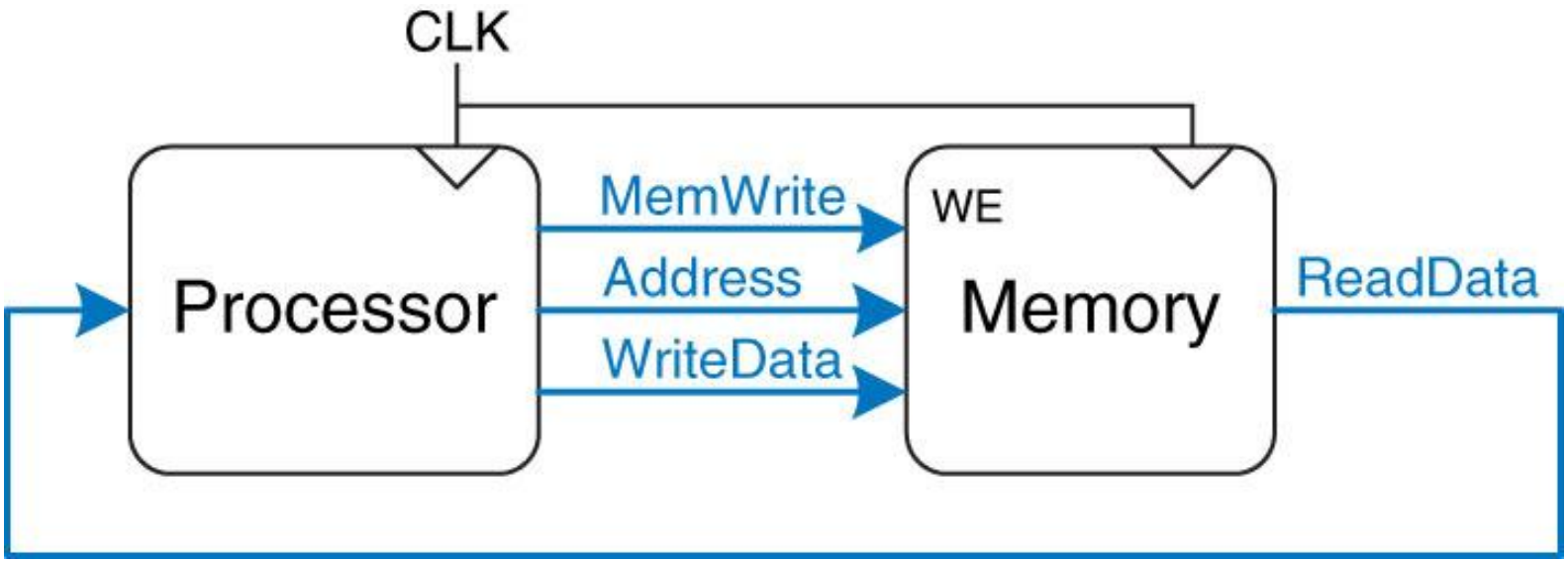

Figure 8.1 The memory interface

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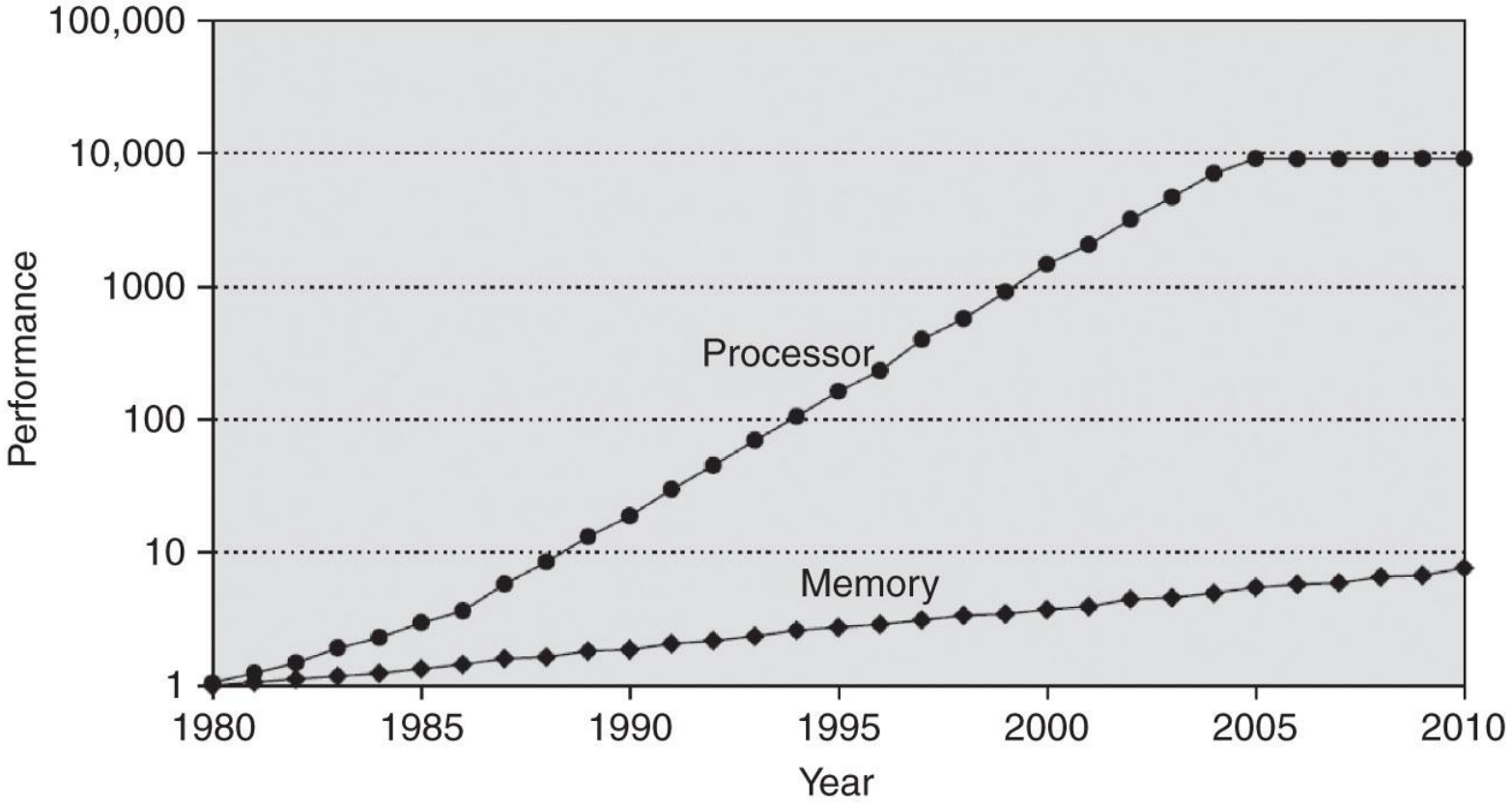

Figure 8.2 Diverging processor and memory performance
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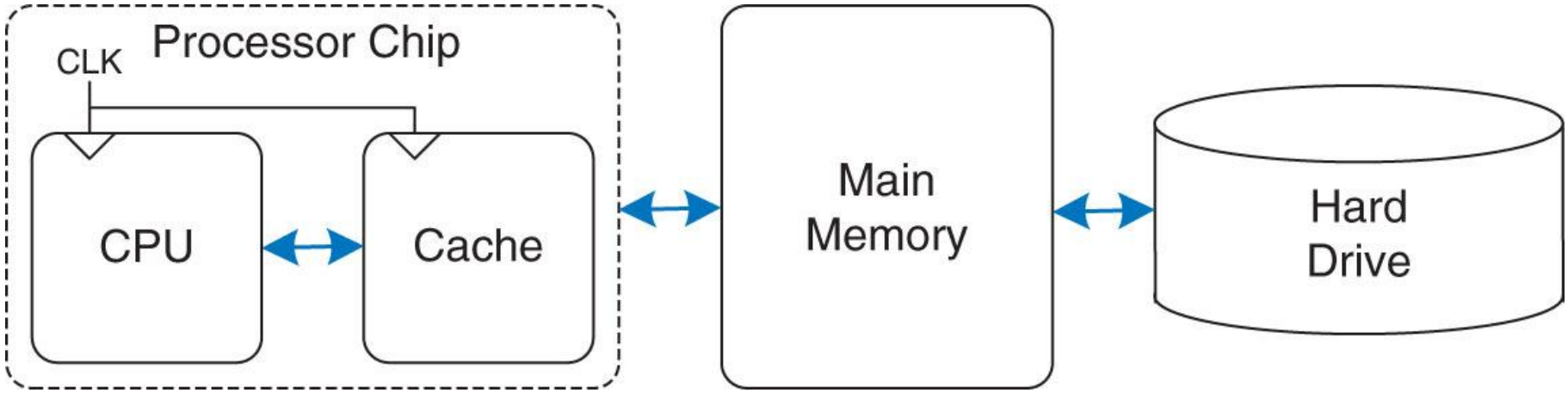

Figure 8.3 A typical memory hierarchy

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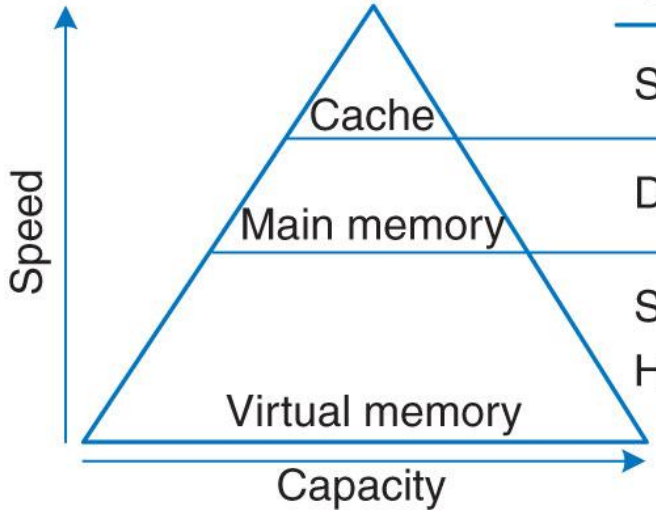

Technology	Price / GB	Access Time (ns)	Bandwidth (GB/s)
SRAM	$10,000	1	25+
DRAM	$10	10–50	10
SSD	$1	100,000	0.5
HDD	$0.1	10,000,000	0.1

Figure 8.4 Memory hierarchy components, with typical characteristics in 2012

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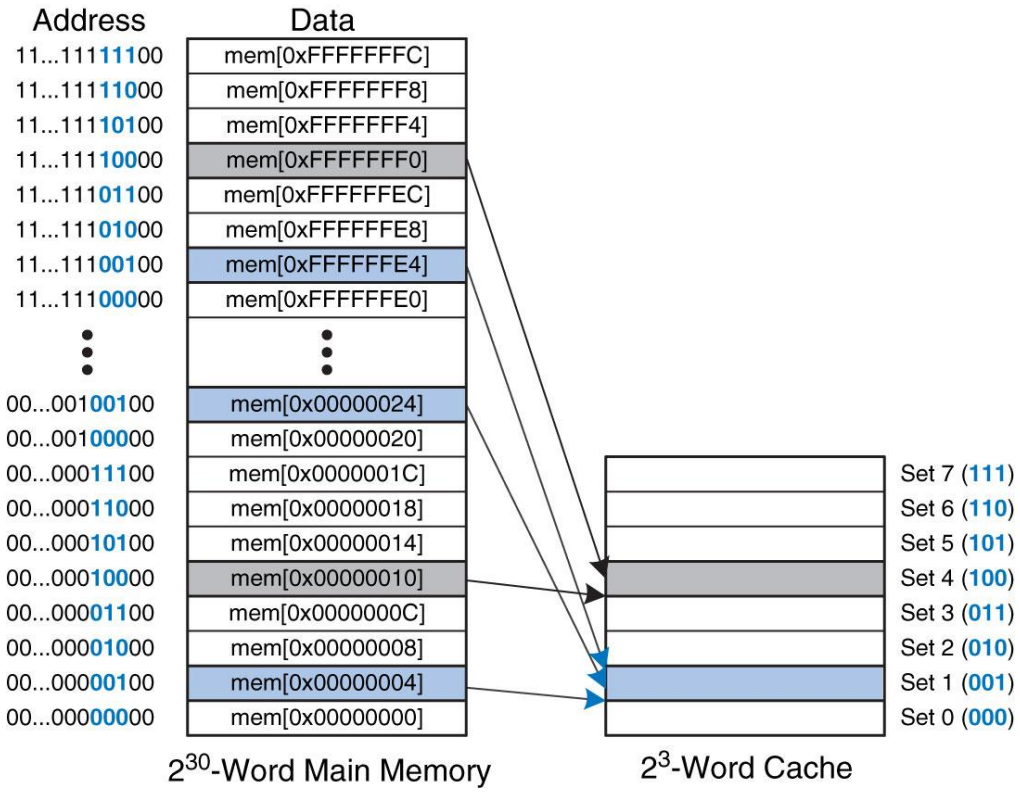

Figure 8.5 Mapping of main memory to a direct mapped cache

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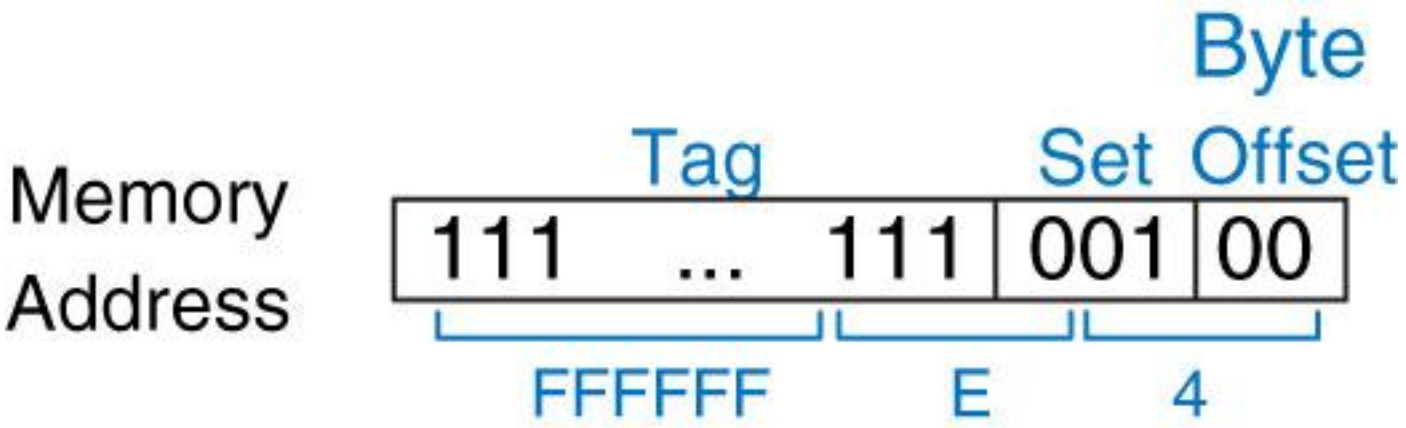

Figure 8.6 Cache fields for address 0xFFFFFFE4 when mapping to the cache in Figure 8.5

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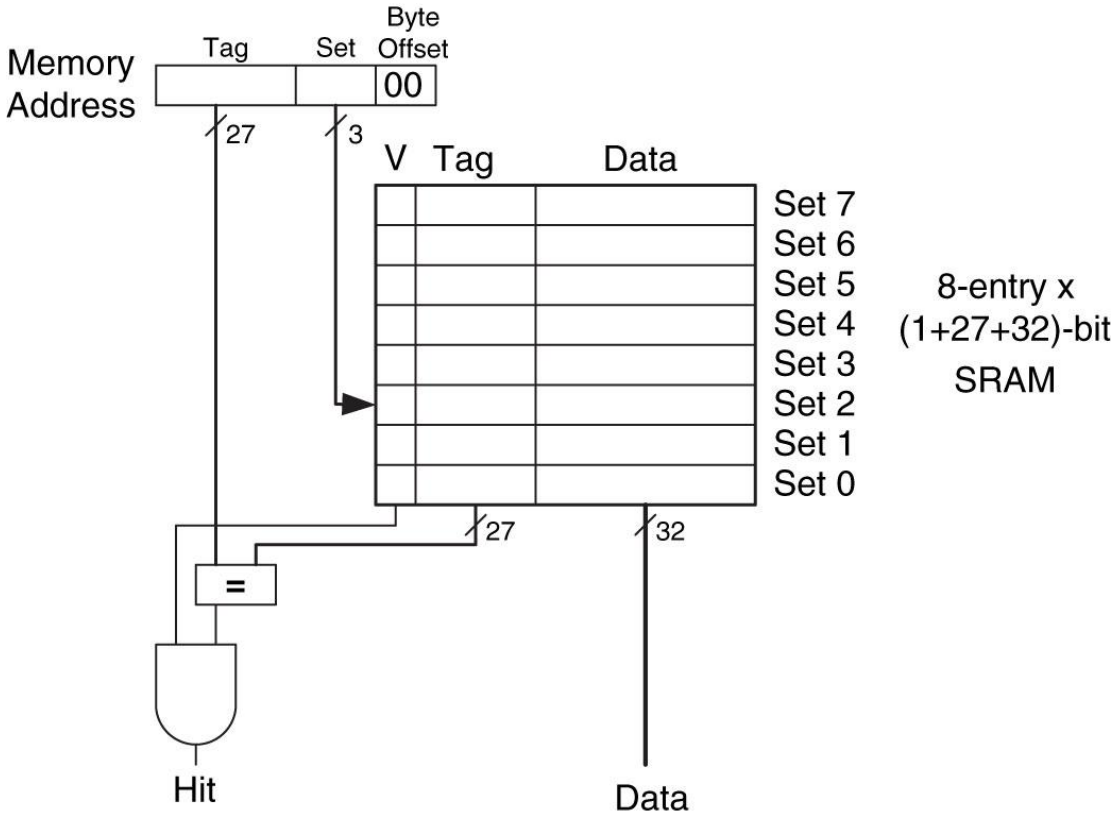

Figure 8.7 Direct mapped cache with 8 sets

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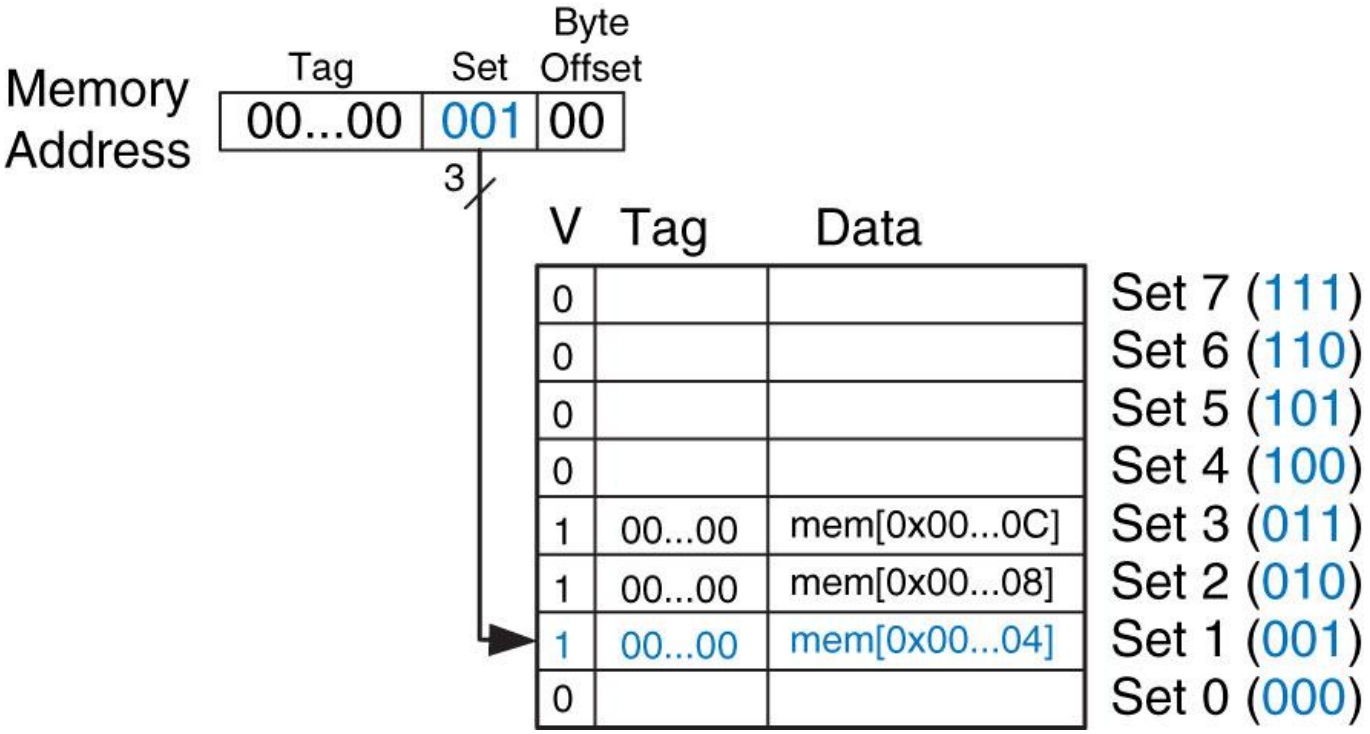

Figure 8.8 Direct mapped cache contents

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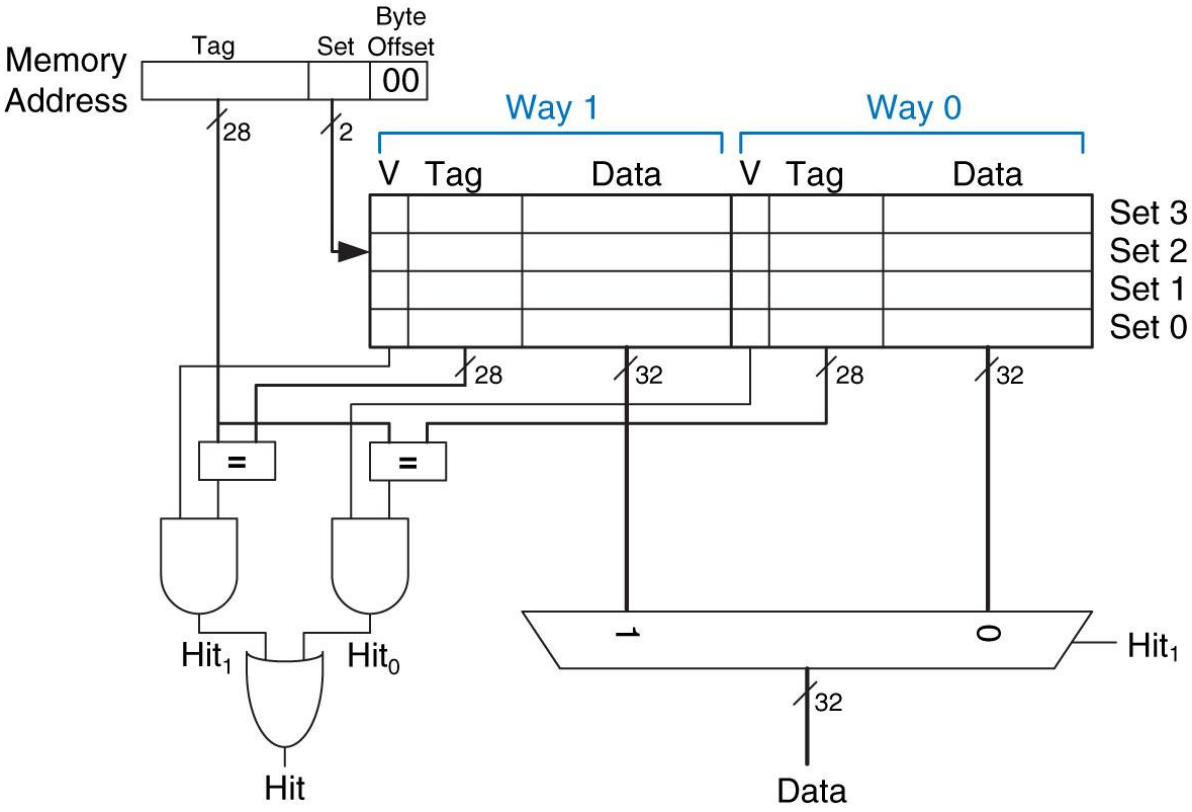

Figure 8.9 Two-way set associative cache

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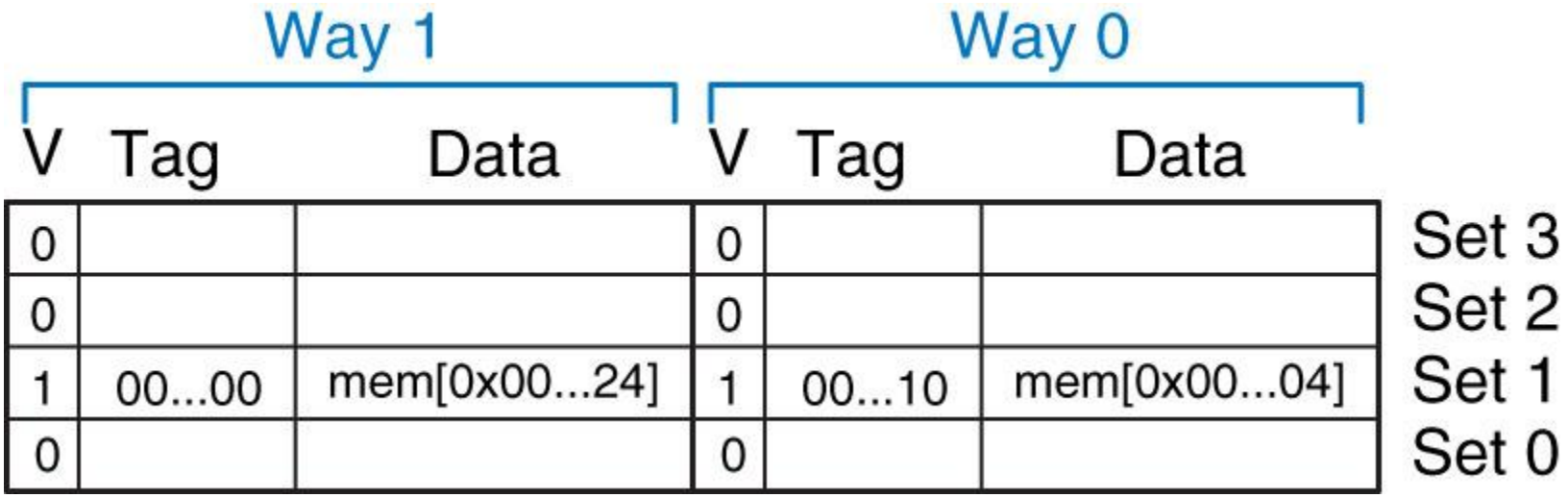

Figure 8.10 Two-way set associative cache contents

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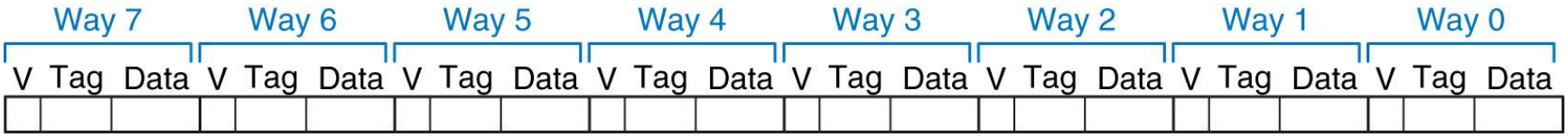

Figure 8.11 Eight-block fully associative cache

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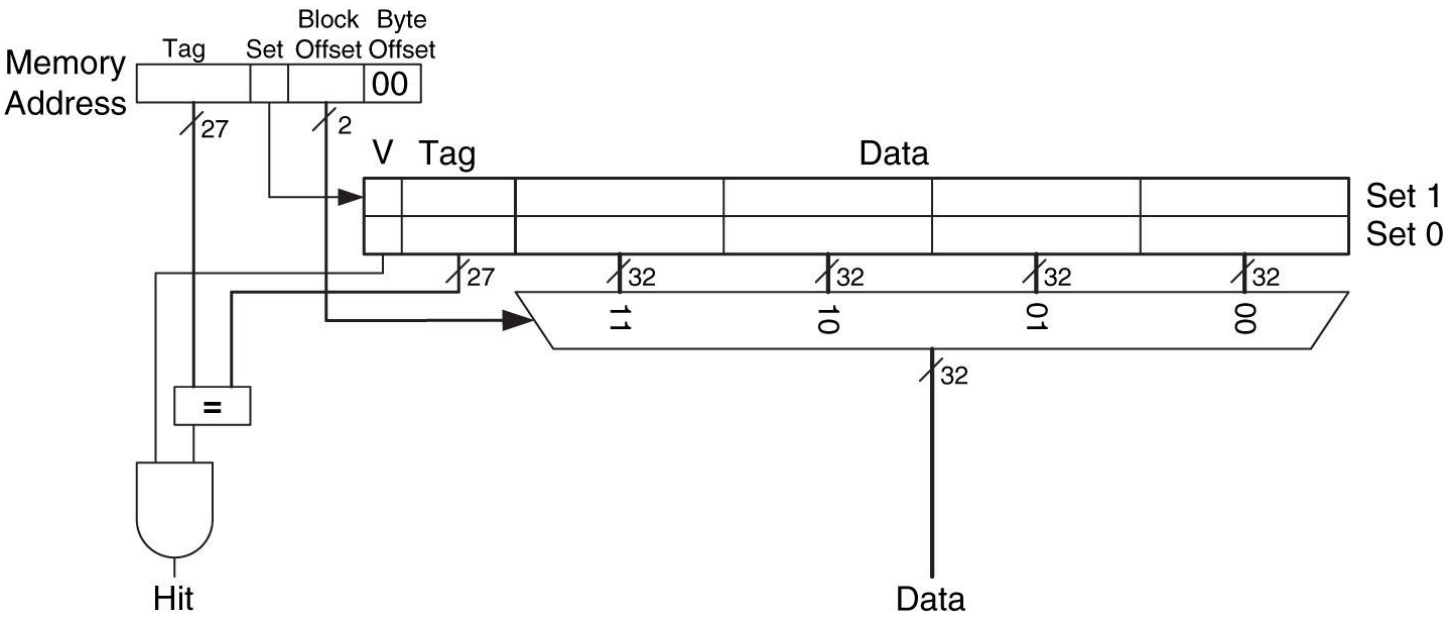

Figure 8.12 Direct mapped cache with two sets and a four-word block size

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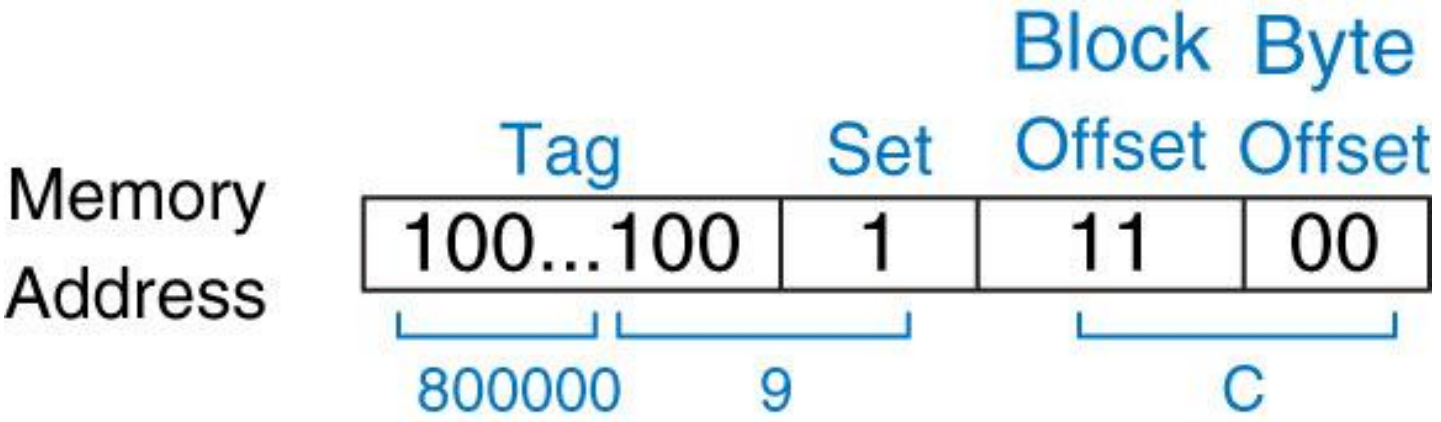

Figure 8.13 Cache fields for address 0x8000009C when mapping to the cache of Figure 8.12

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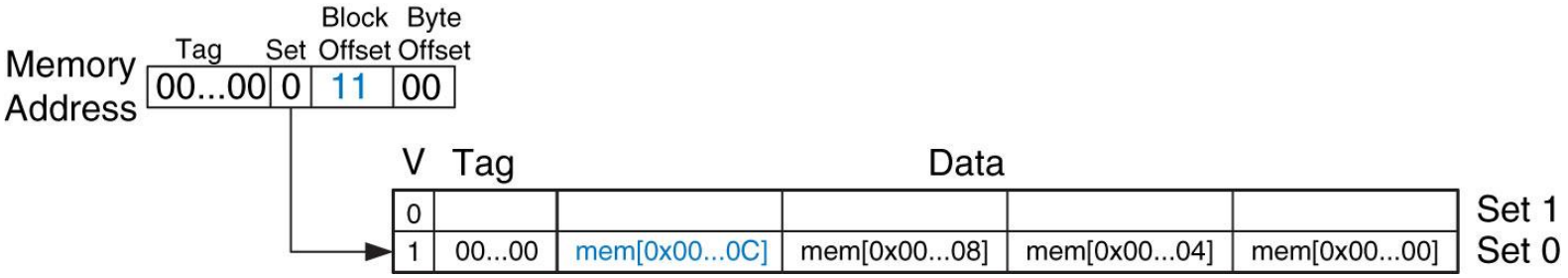

Figure 8.14 Cache contents with a block size *b* of four words

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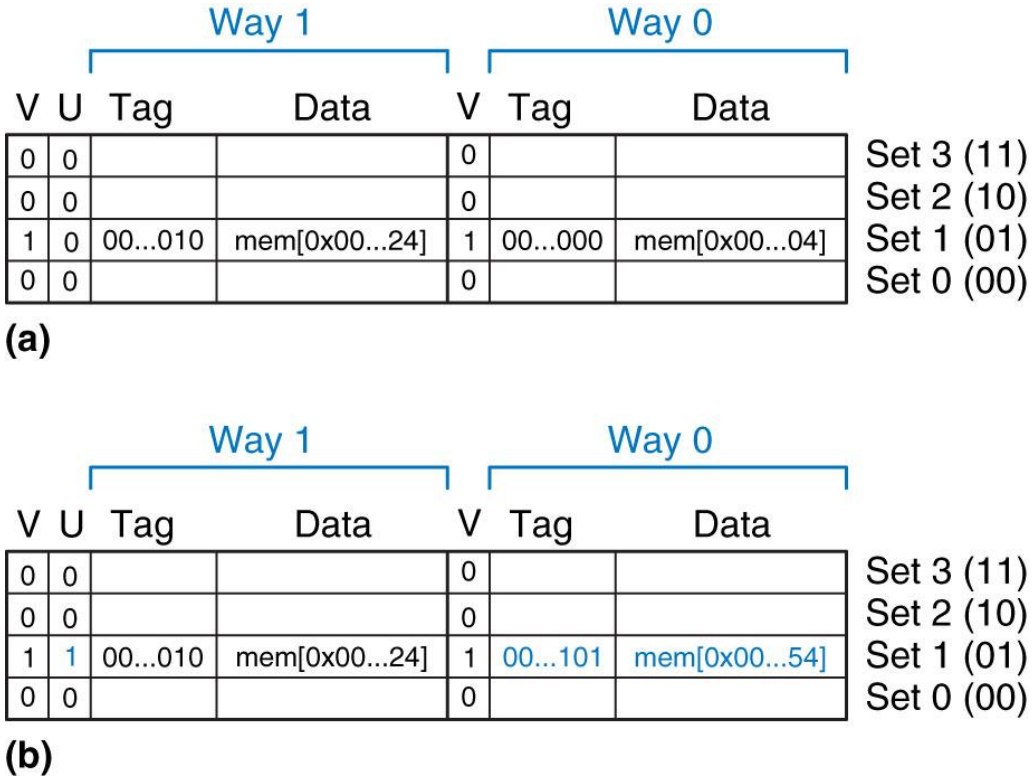

Figure 8.15 Two-way associative cache with LRU replacement

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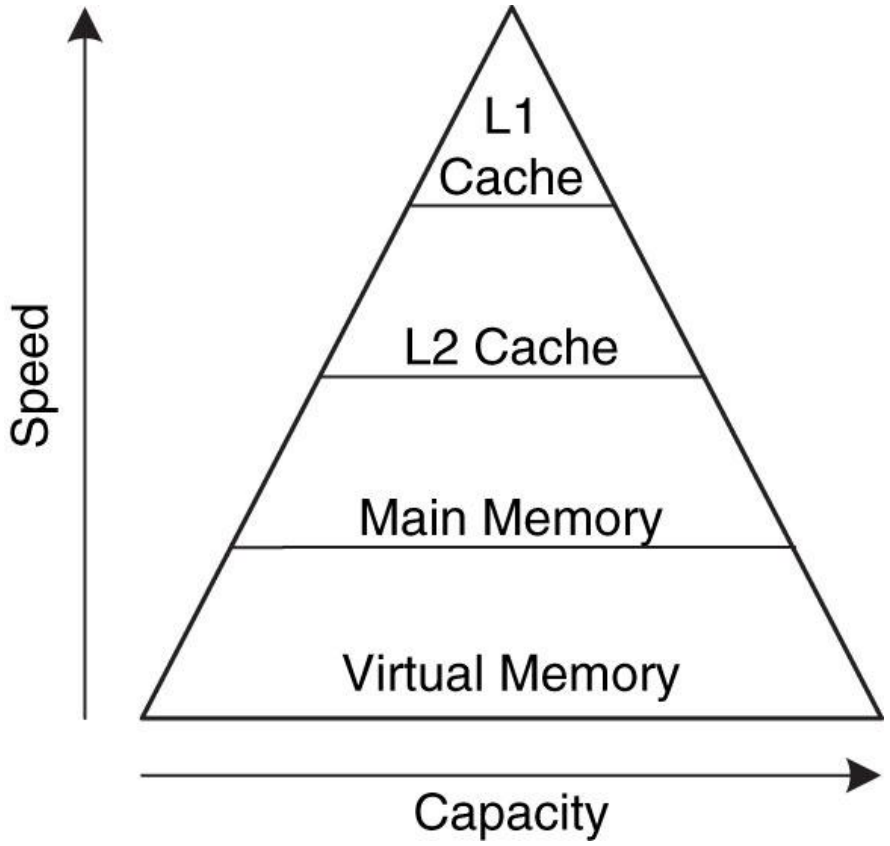

Figure 8.16 Memory hierarchy with two levels of cache

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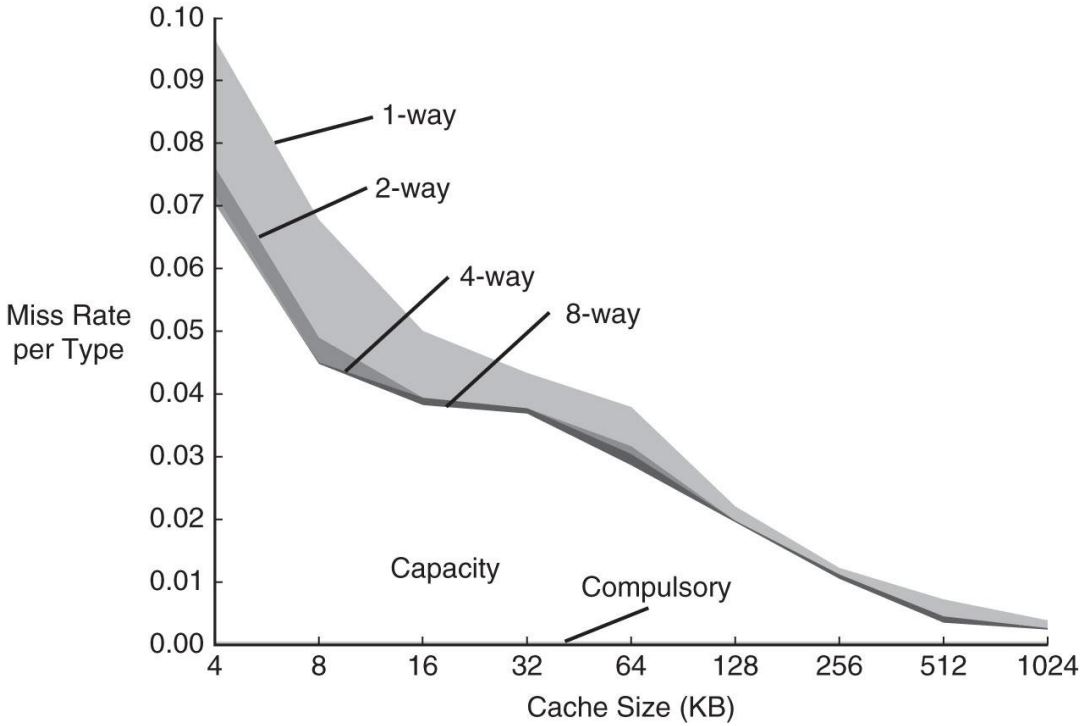

Figure 8.17 Miss rate versus cache size and associativity on SPEC2000 benchmark
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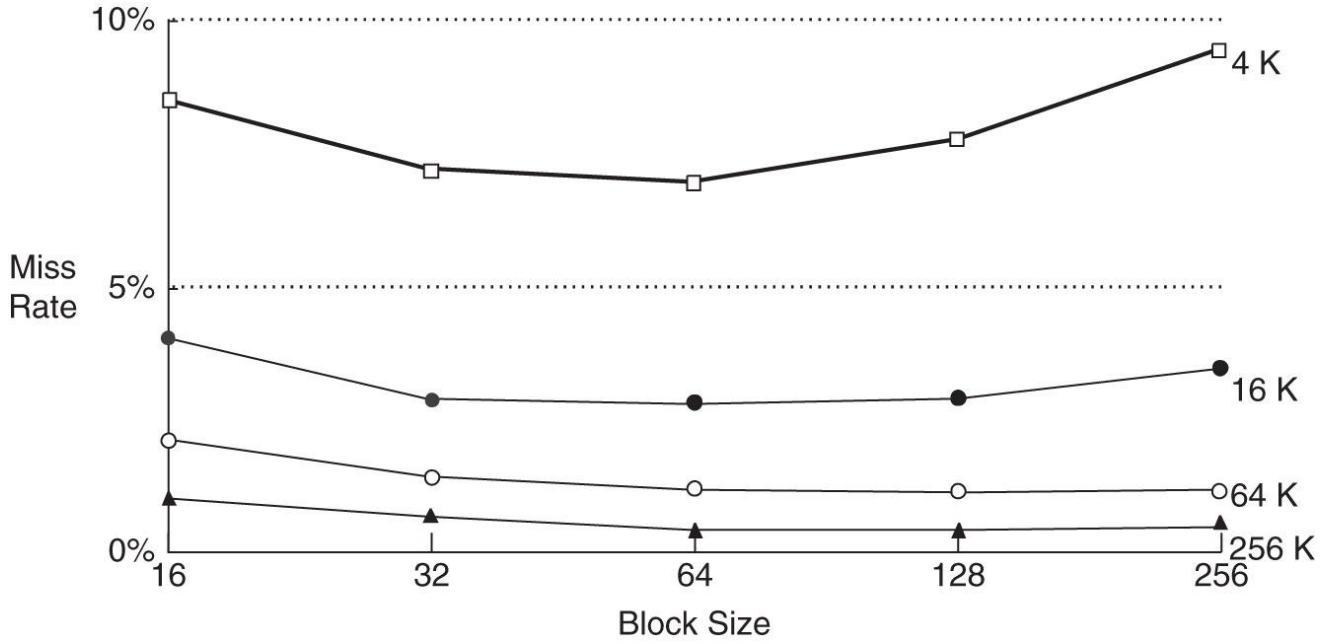

Figure 8.18 Miss rate versus block size and cache size on SPEC92 benchmark
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Figure 8.19 Hard disk

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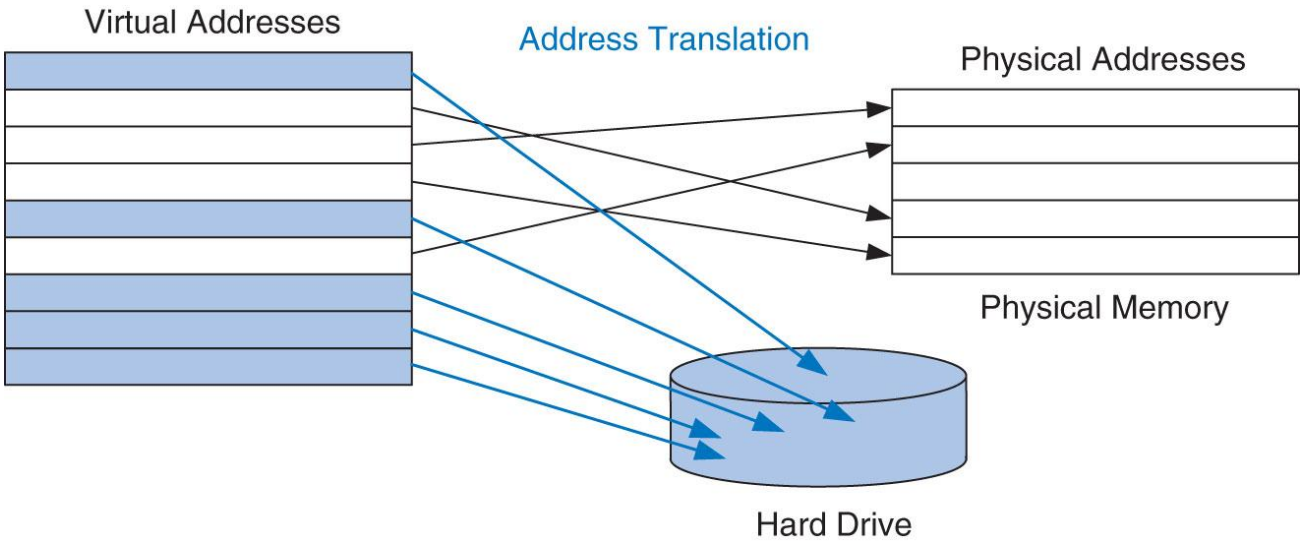

Figure 8.20 Virtual and physical pages

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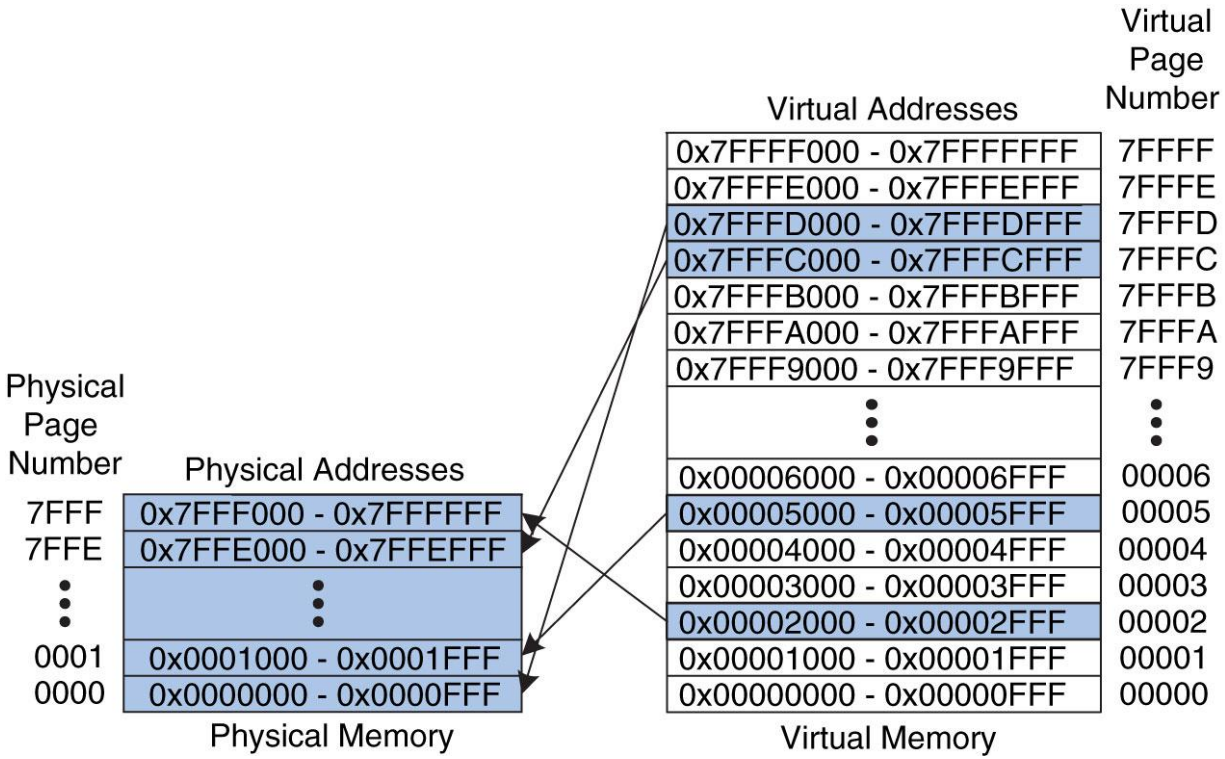

Figure 8.21 Physical and virtual pages

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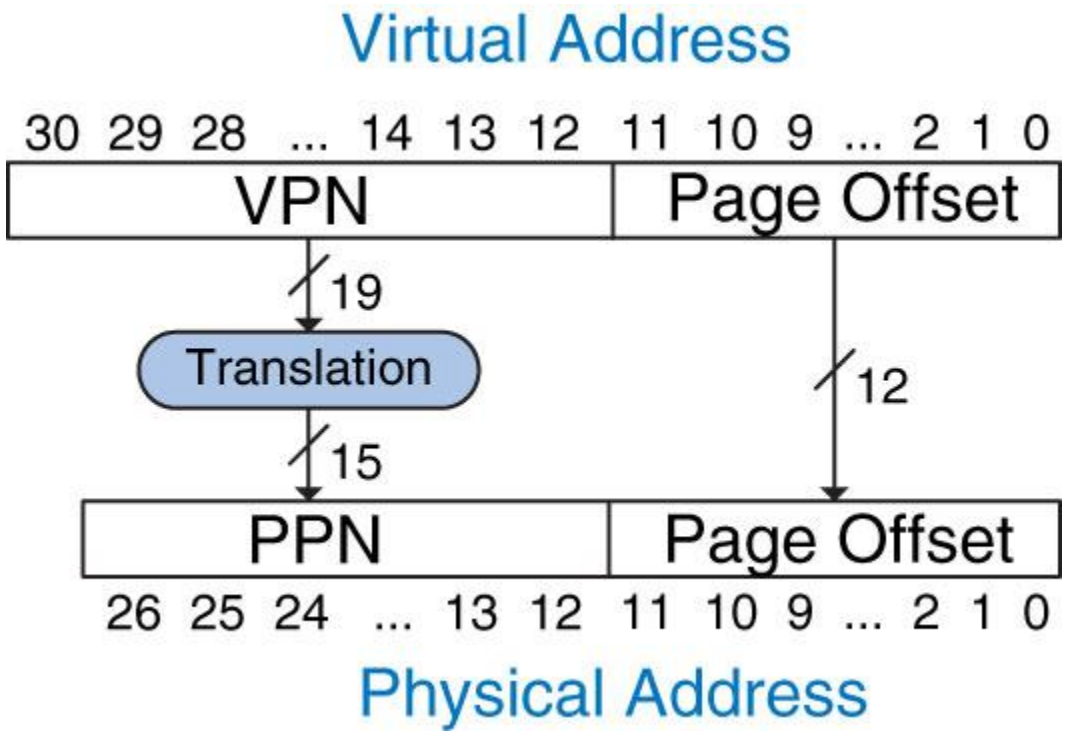

Figure 8.22 Translation from virtual address to physical address

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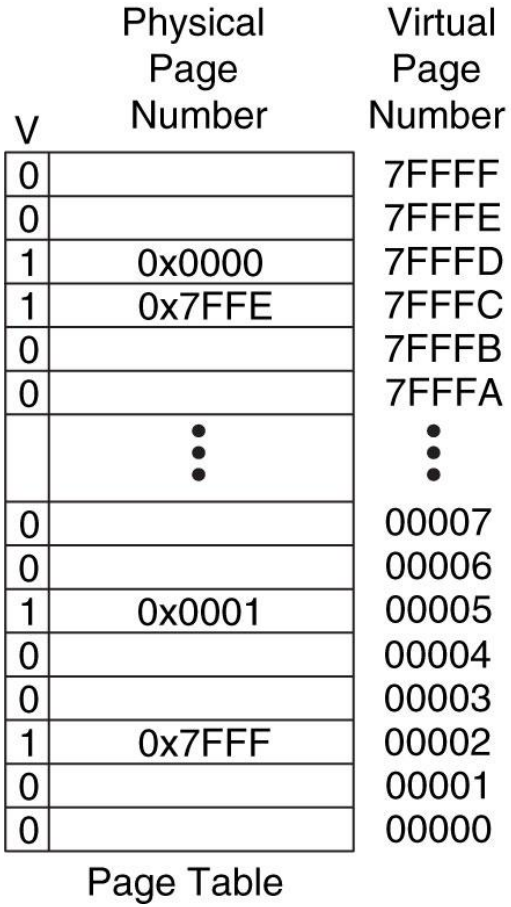

Figure 8.23 The page table for Figure 8.21

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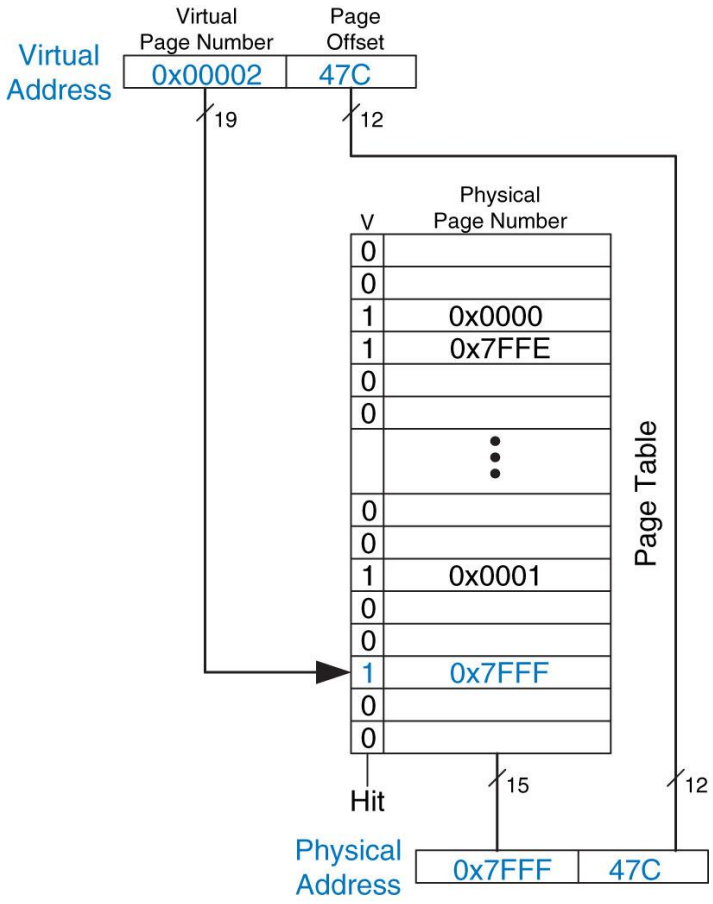

Figure 8.24 Address translation using the page table

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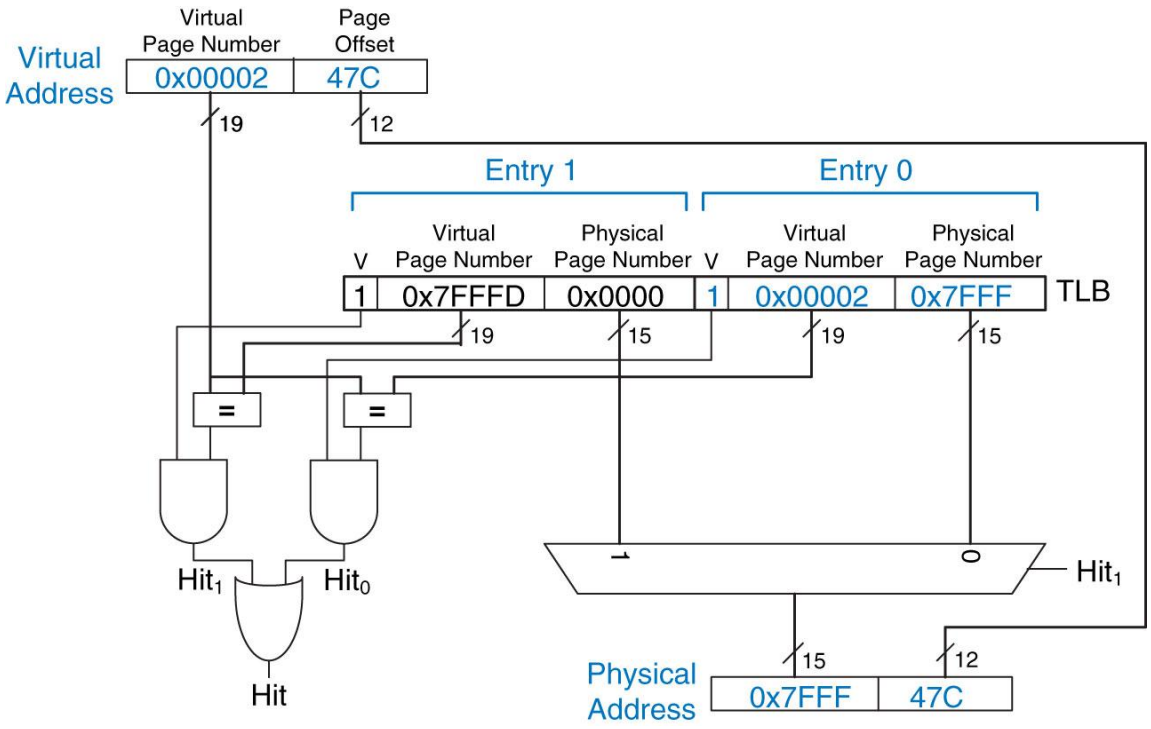

Figure 8.25 Address translation using a two-entry TLB

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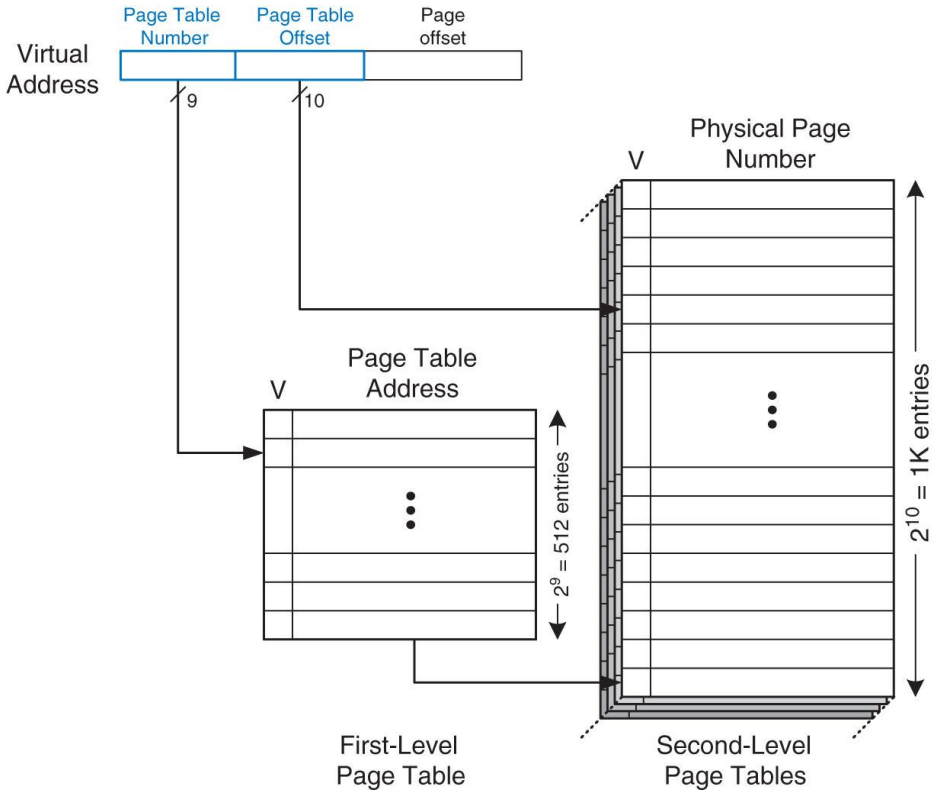

Figure 8.26 Hierarchical page tables

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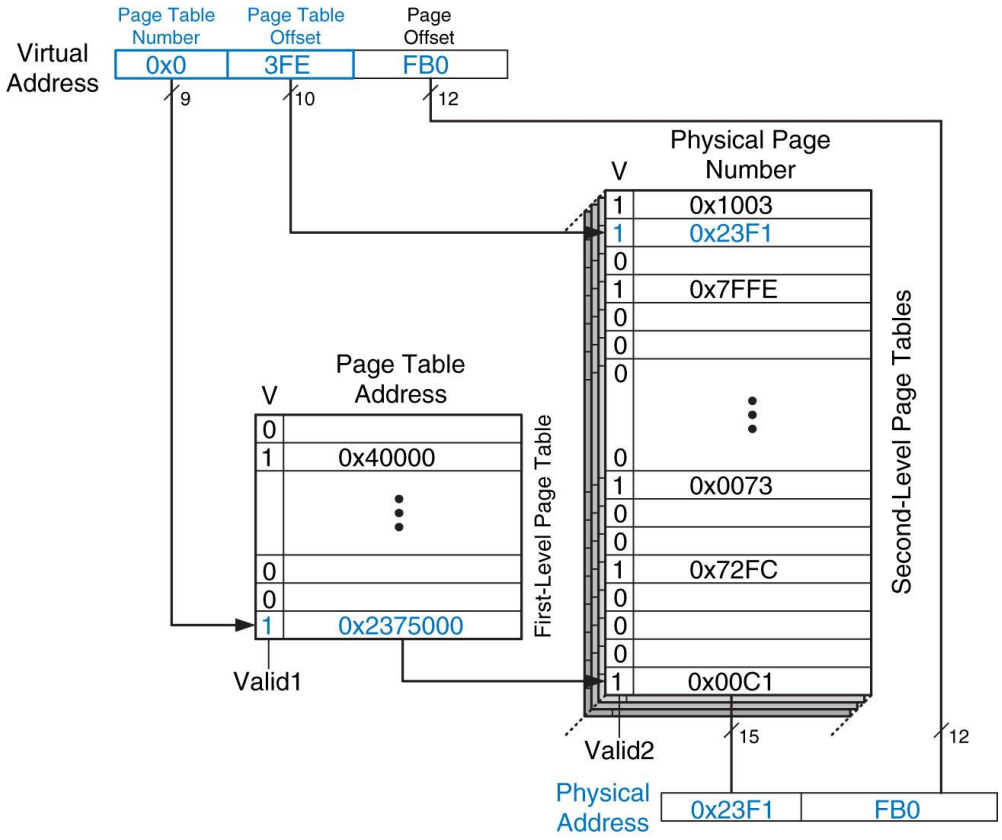

Figure 8.27 Address translation using a two-level page table

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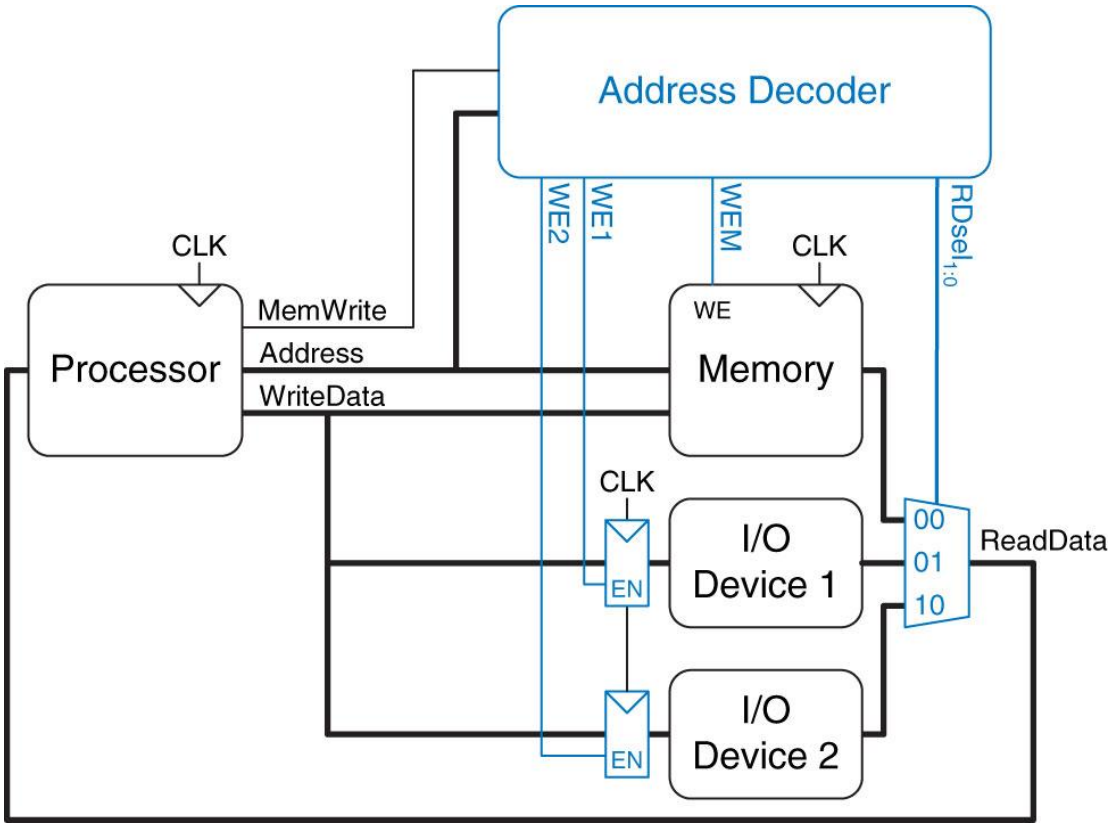

Figure 8.28 Support hardware for memory-mapped I/O

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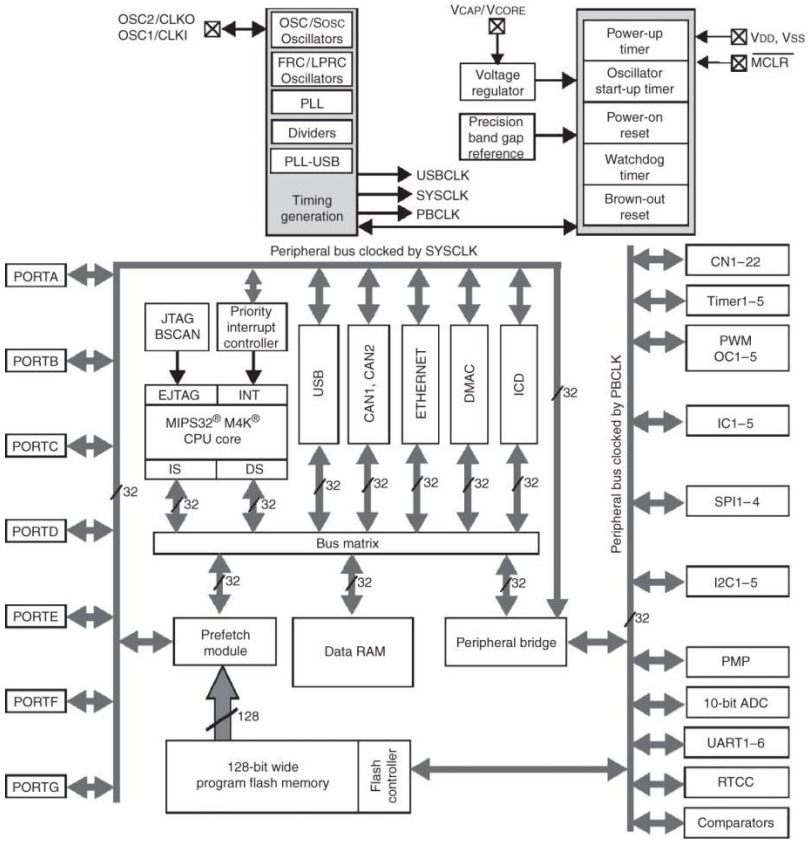

Figure 8.29 PIC32MX675F512H block diagram
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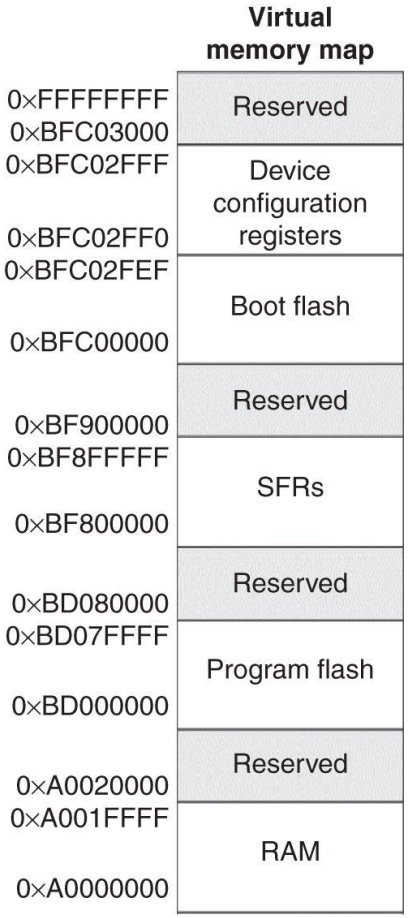

Figure 8.30 PIC32 memory map
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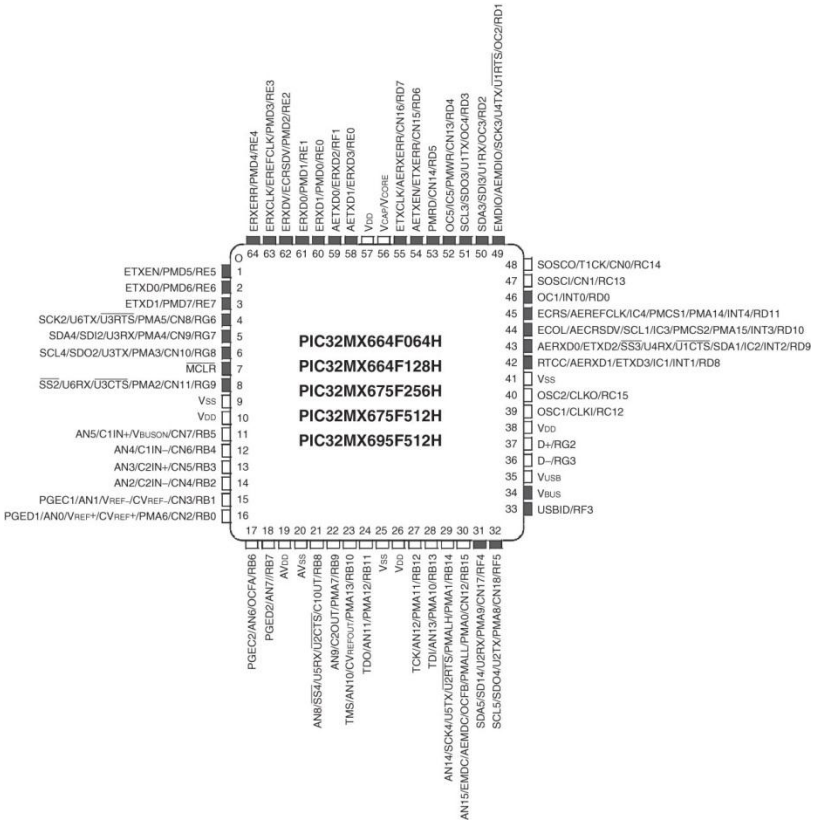

Figure 8.31 PIC32MX6xxFxxH pinout. Black pins are 5 V-tolerant.
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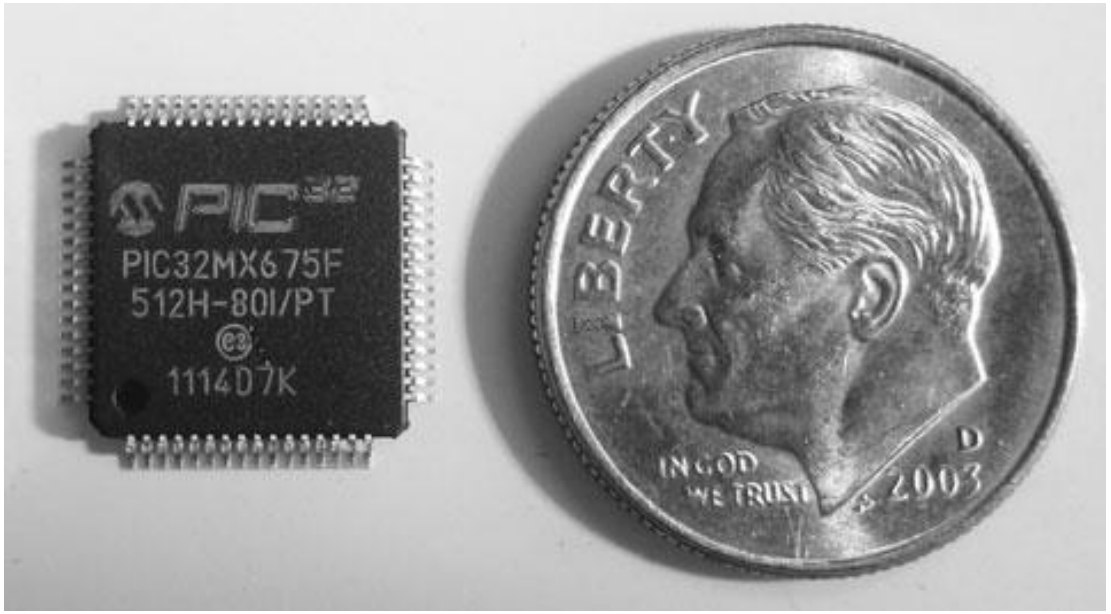

Figure 8.32 PIC32 in 64-pin TQFP package

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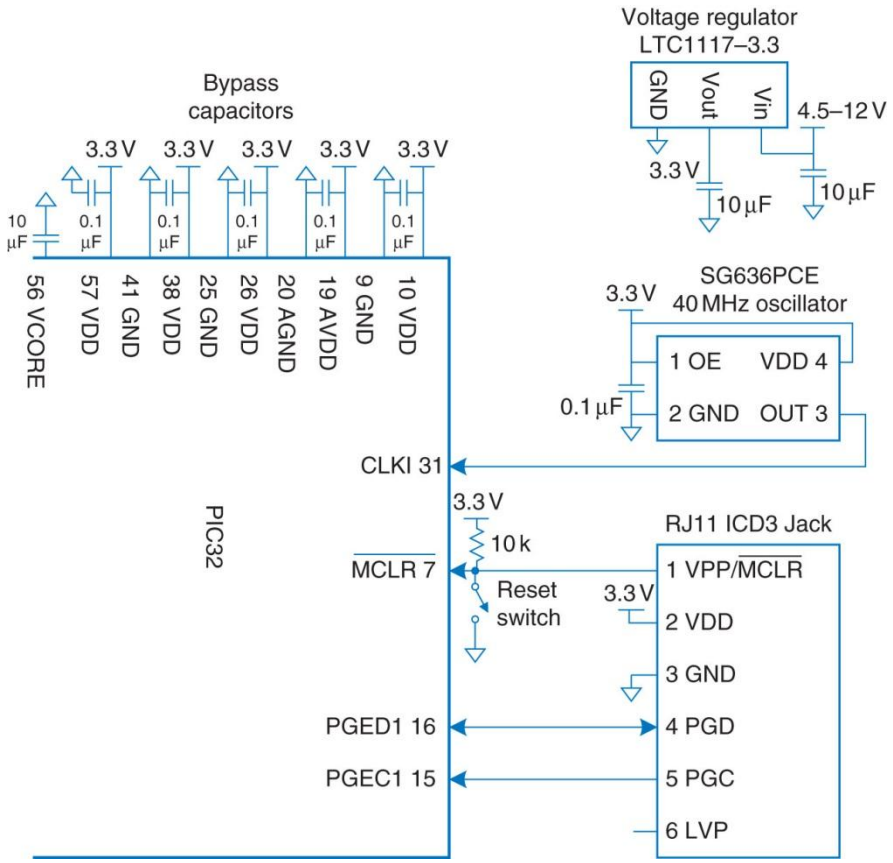

Figure 8.33 PIC32 basic operational schematic

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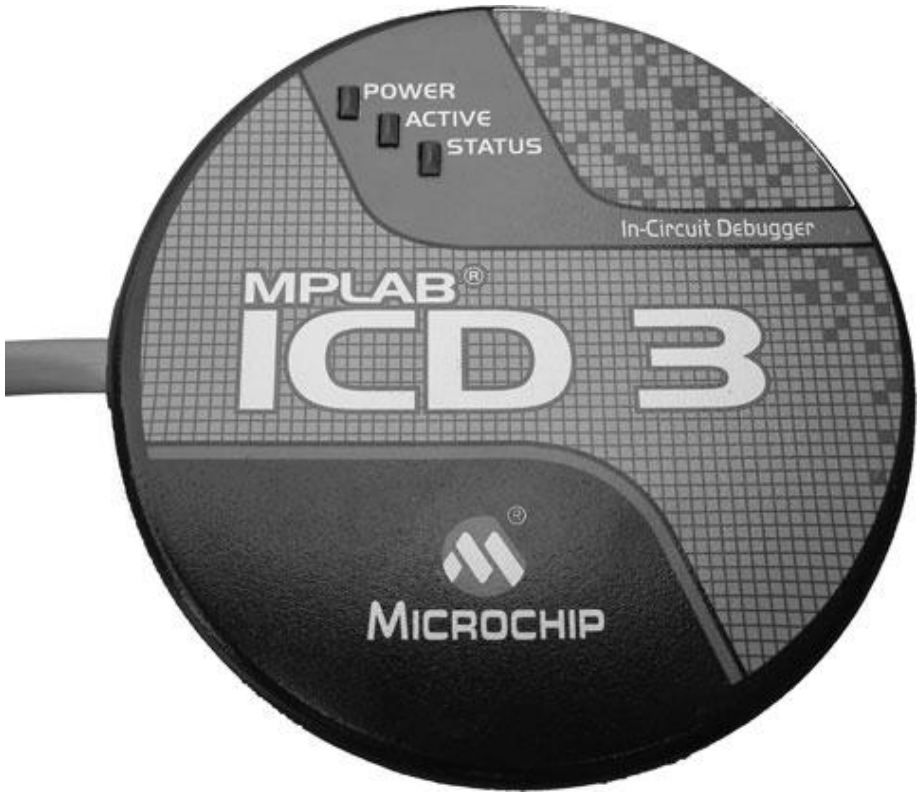

Figure 8.34 Microchip ICD3

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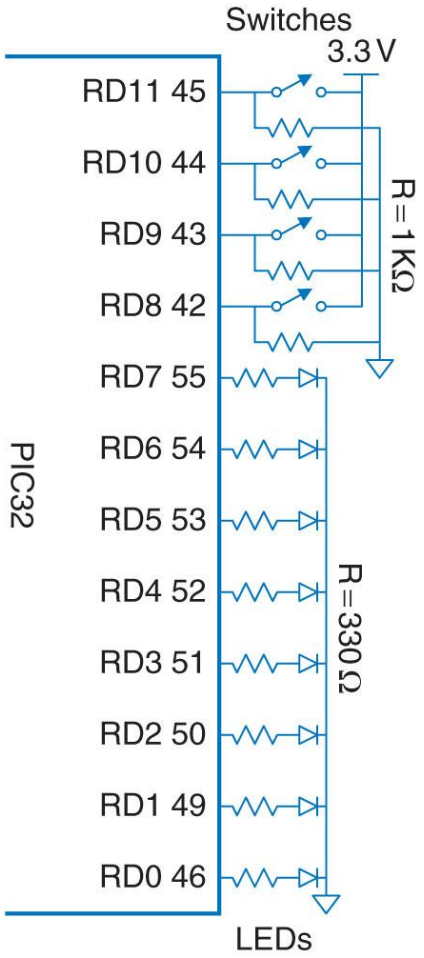

Figure 8.35 LEDs and switches connected to 12-bit GPIO port D

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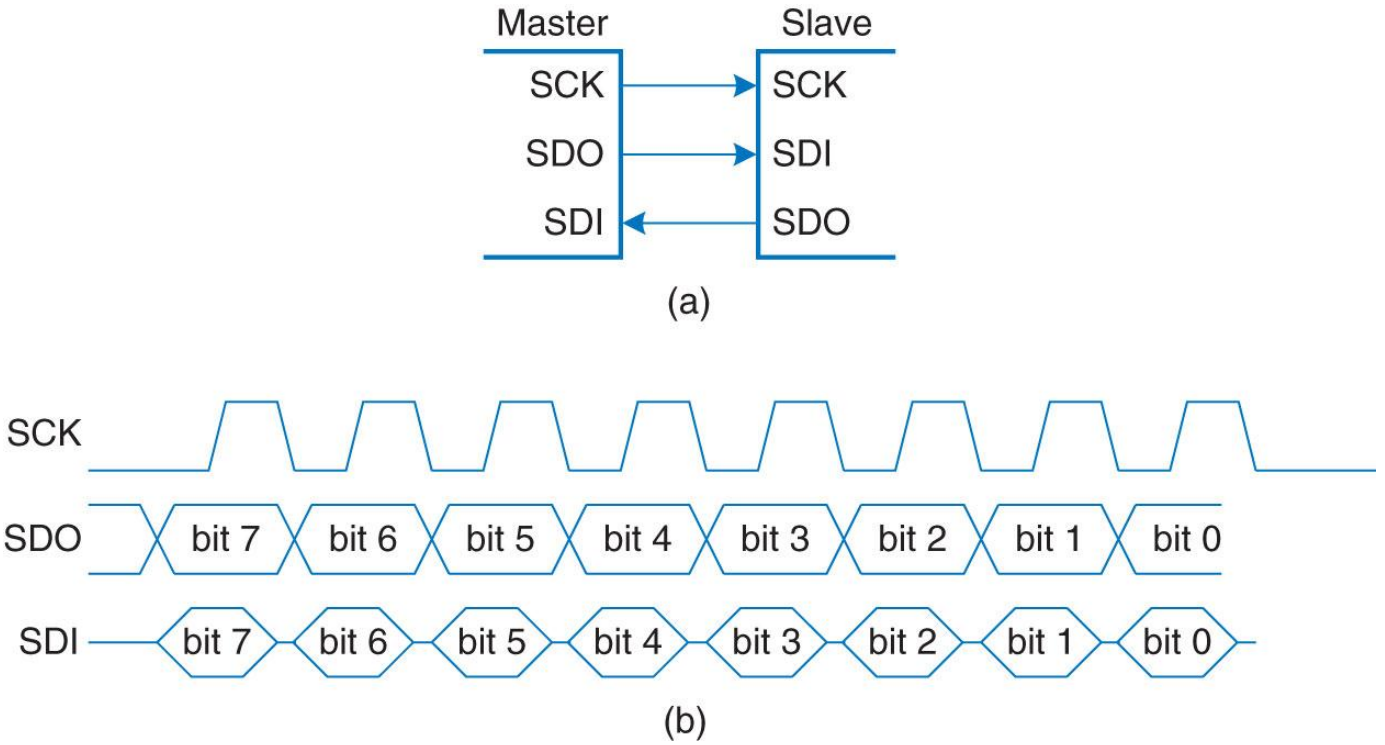

Figure 8.36 SPI connection and master waveforms

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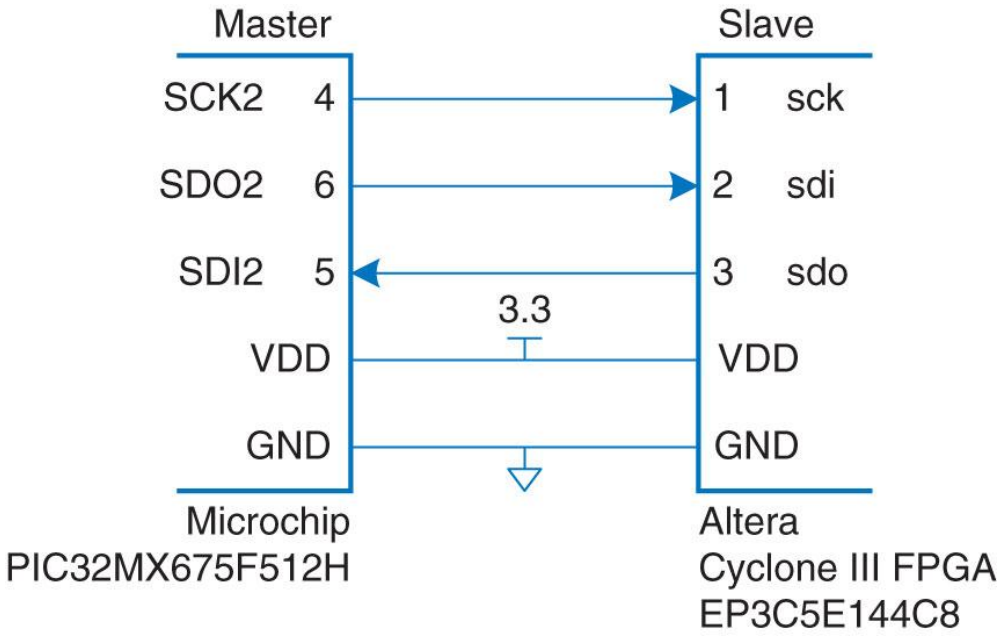

Figure 8.37 SPI connection between PIC32 and FPGA

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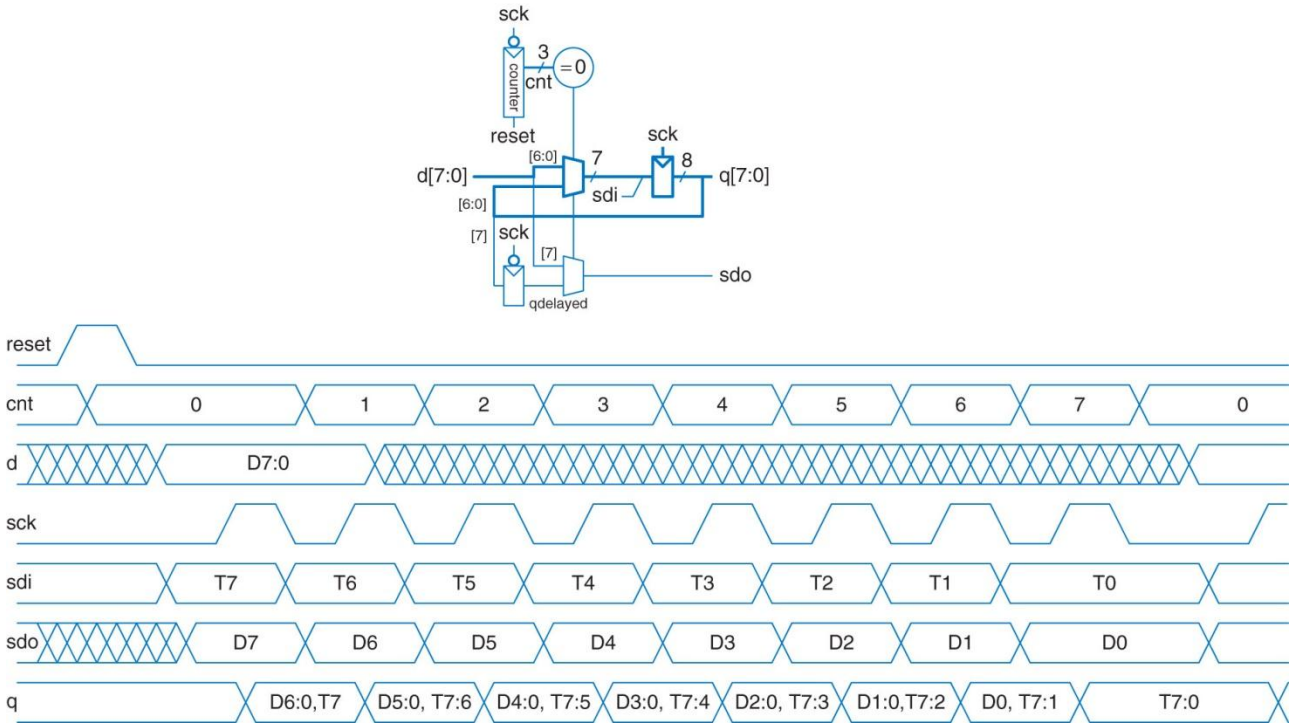

Figure 8.38 SPI slave circuitry and timing

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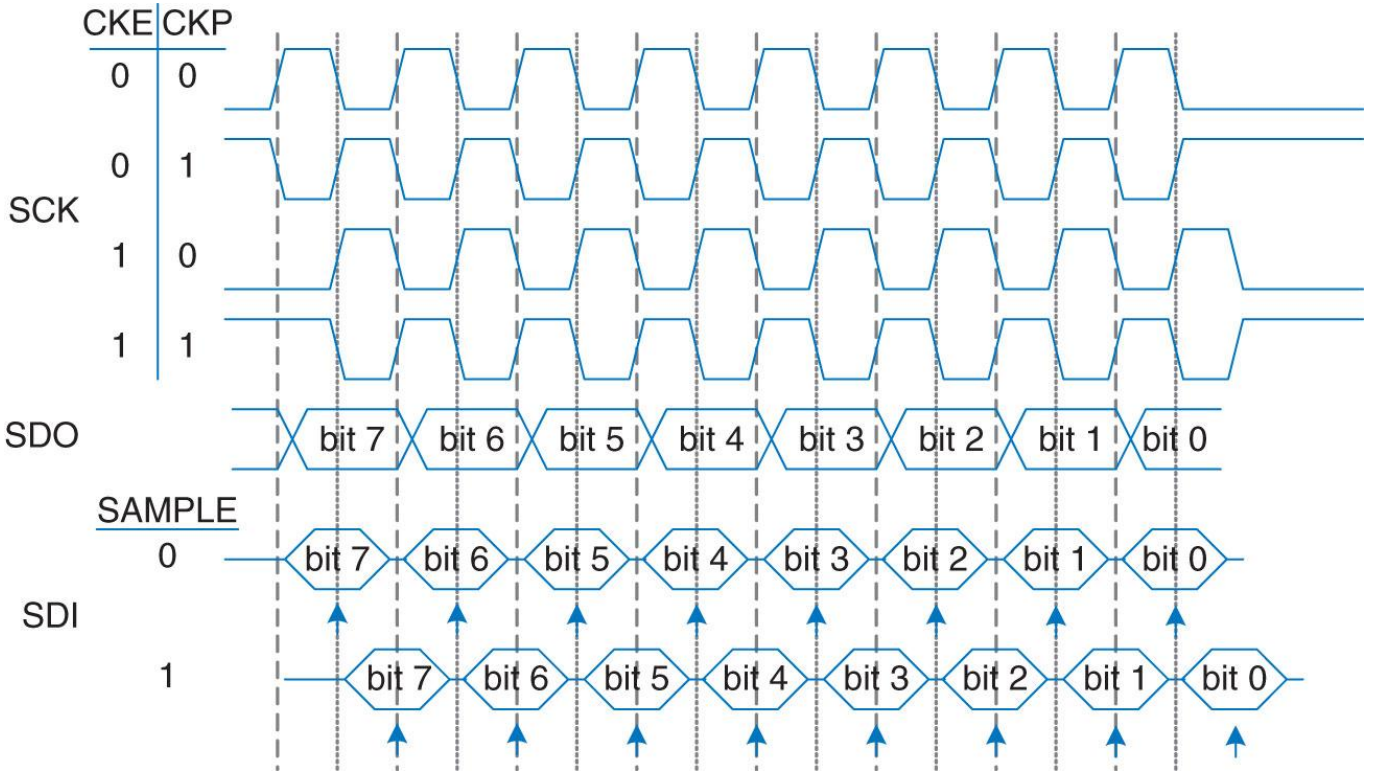

Figure 8.39 Clock and data timing controlled by CKE, CKP, and SAMPLE

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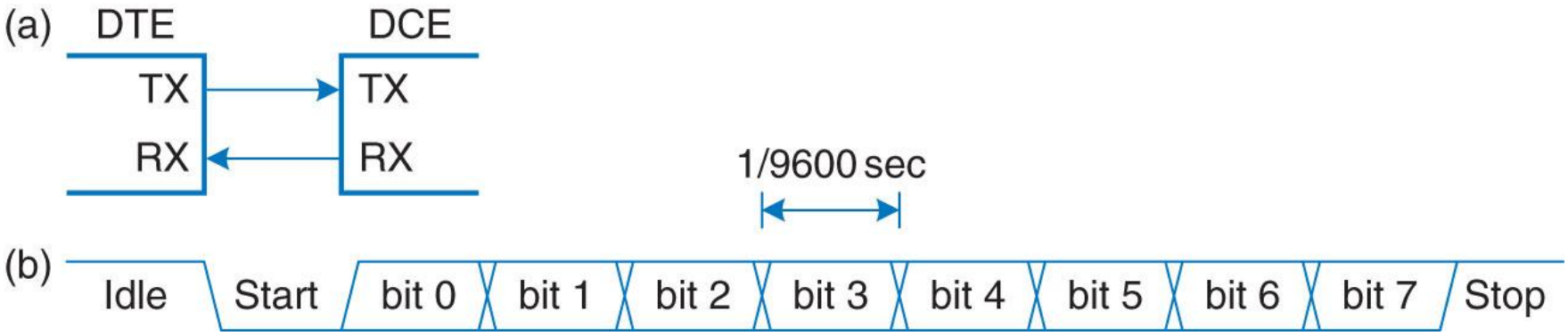

Figure 8.40 Asynchronous serial link

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Figure 8.41 Cap'n Crunch Bosun Whistle.
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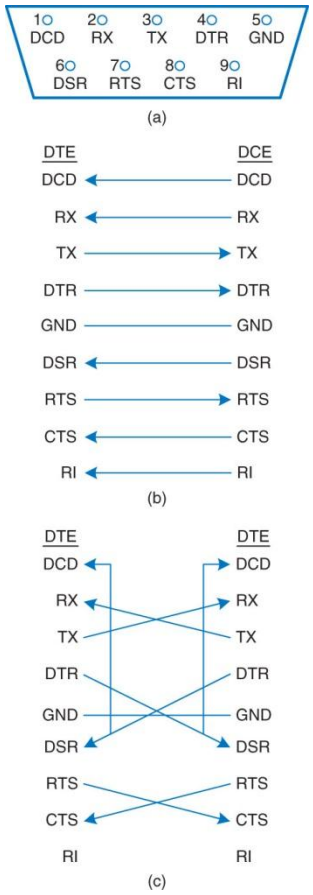

Figure 8.42 DE-9 male cable (a) pinout, (b) standard wiring, and (c) null modem wiring

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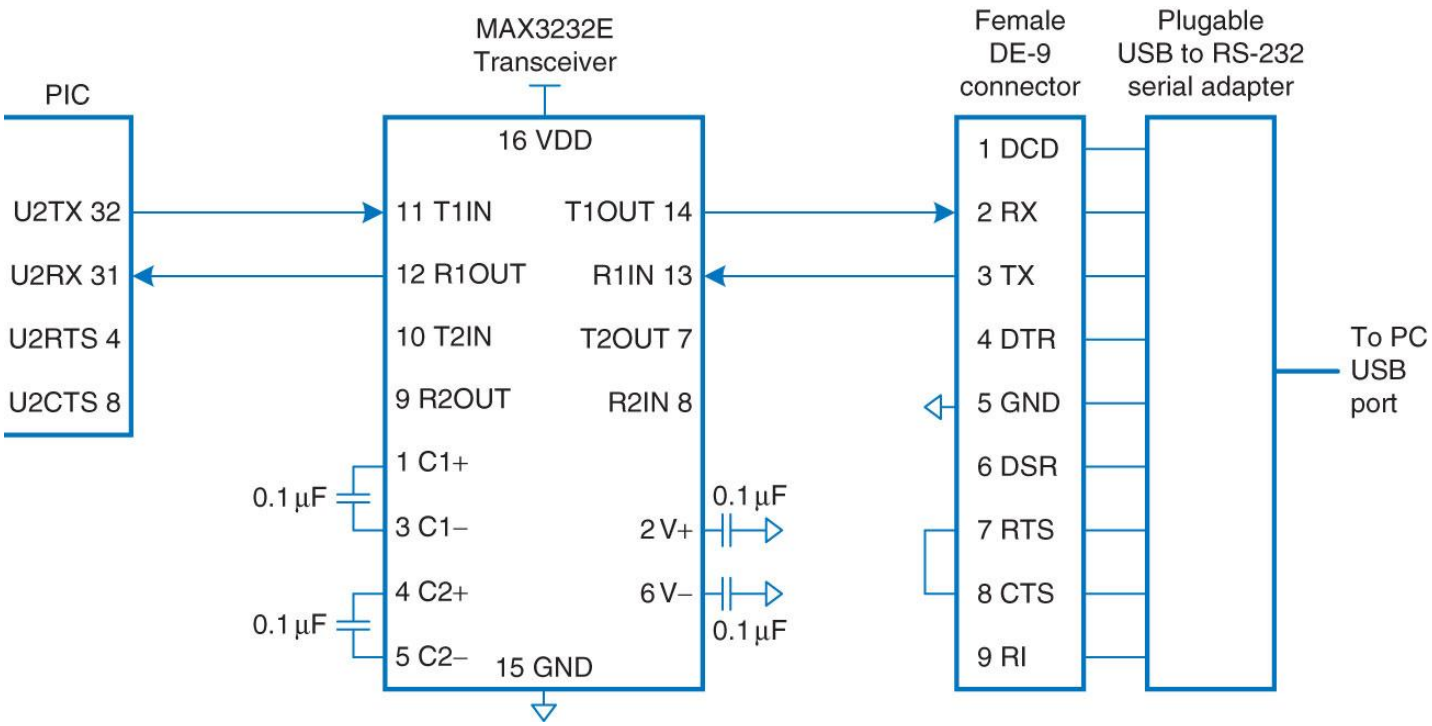

Figure 8.43 PIC32 to PC serial link

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Figure 8.44 Plugable USB to RS-232 DB9 Serial Adapter
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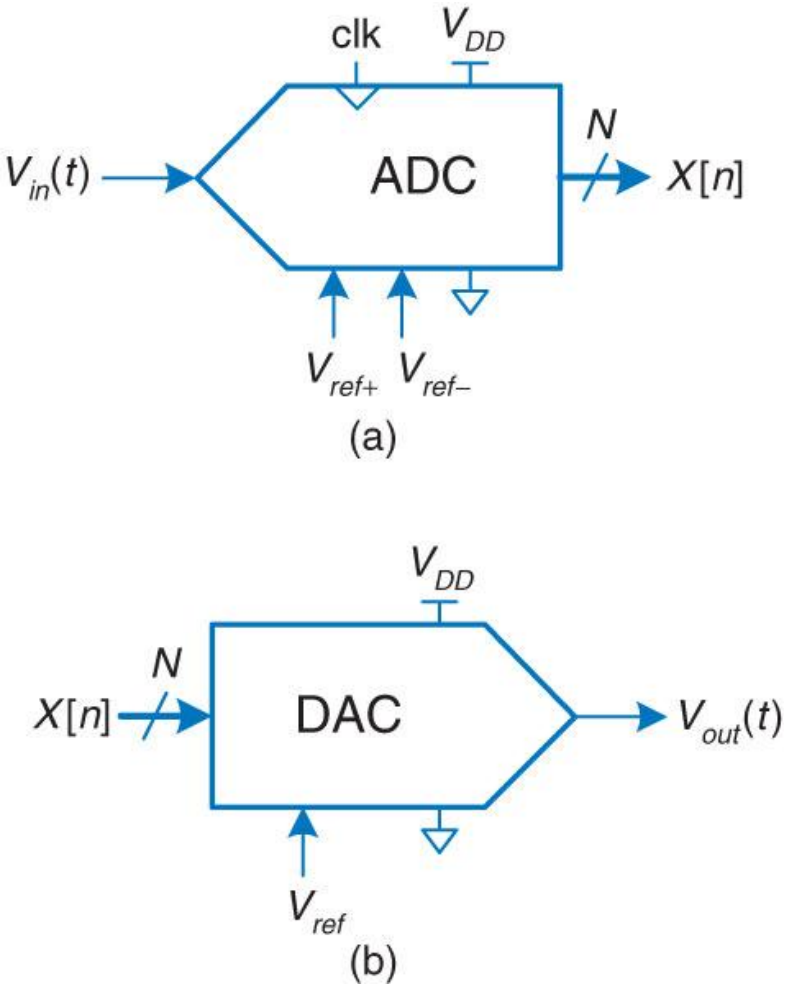

Figure 8.45 ADC and DAC symbols

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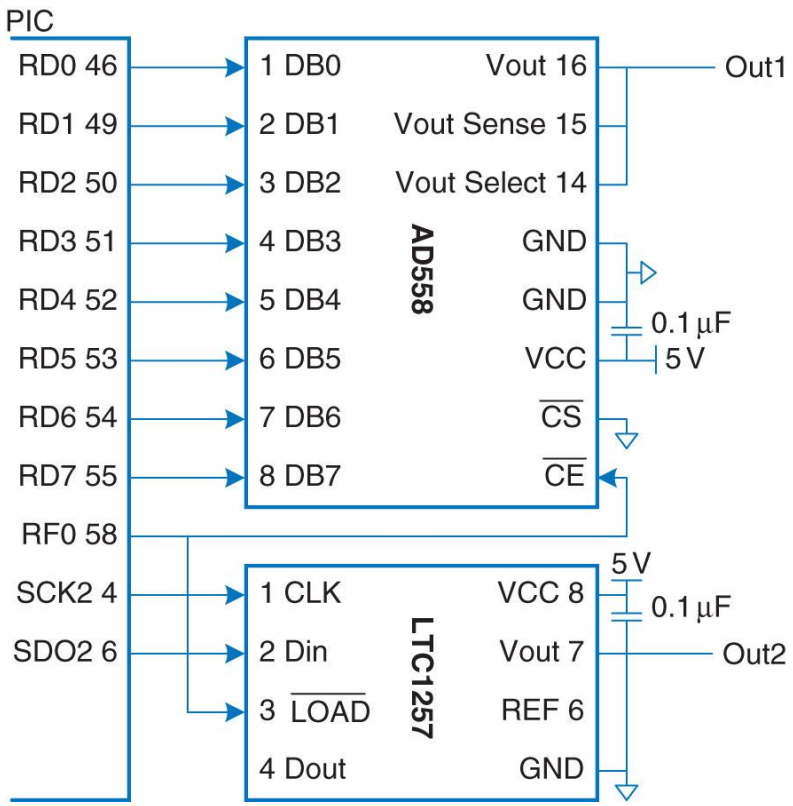

Figure 8.46 DAC parallel and serial interfaces to a PIC32

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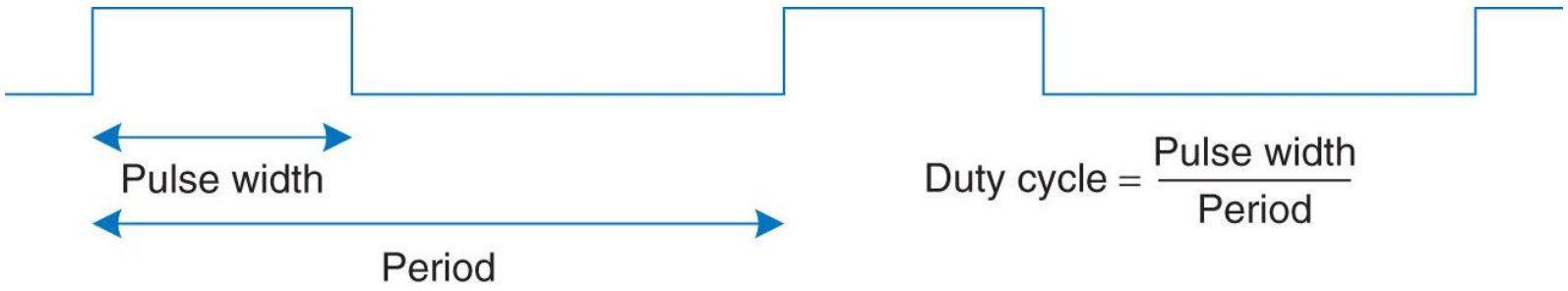

Figure 8.47 Pulse-width modulated (PWM) signal

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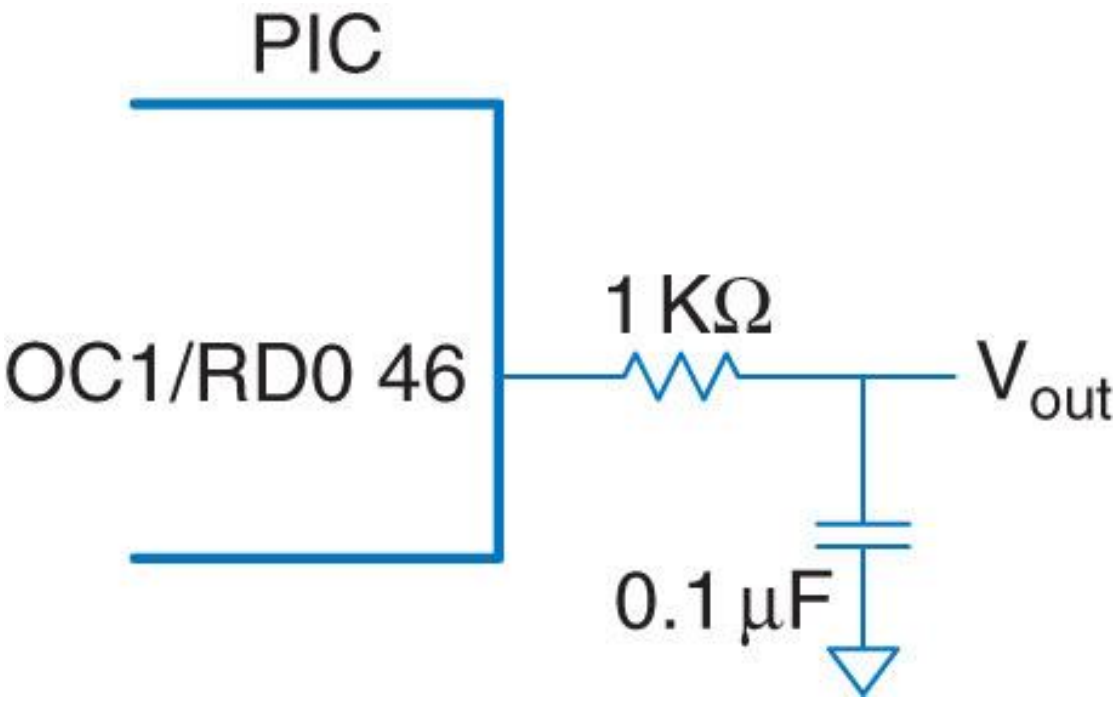

Figure 8.48 Analog output using PWM and low-pass filter

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Figure 8.49 Crystalfontz CFAH2002A-TMI 20 · 2 character LCD
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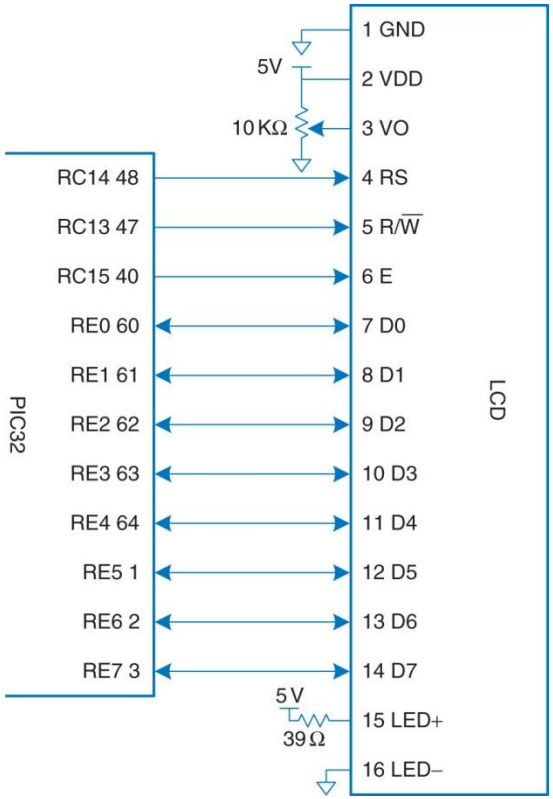

Figure 8.50 Parallel LCD interface

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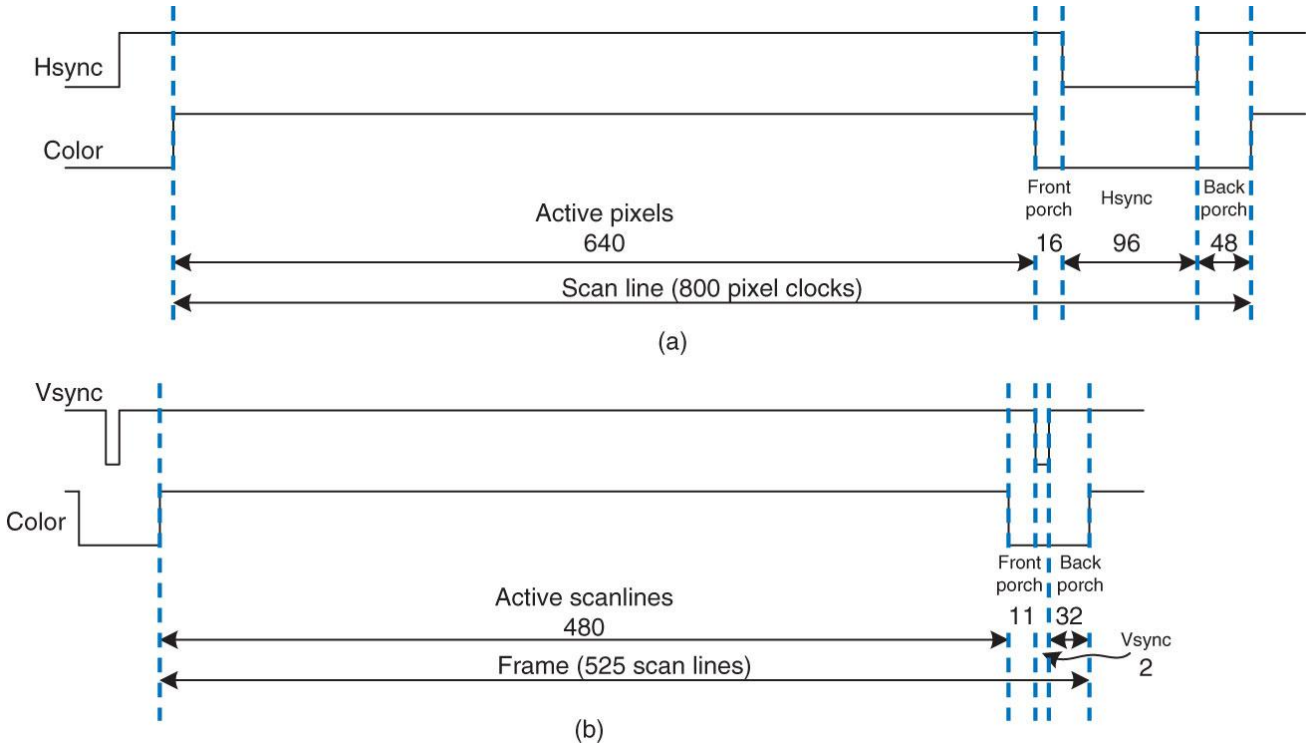

Figure 8.51 VGA timing: (a) horizontal, (b) vertical

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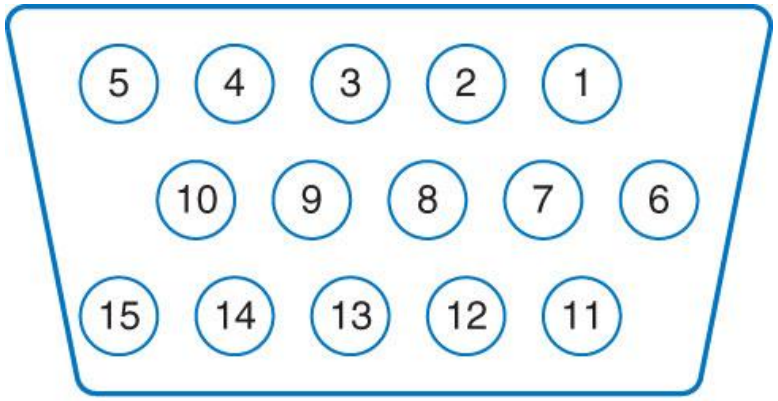

1: Red
2: Green
3: Blue
4: Reserved
5: GND
6: GND
7: GND
8: GND
9: 5 V (optional)
10: GND
11: Reserved
12: I^2C data
13: HSync
14: Vsync
15: I^2C clock

Figure 8.52 VGA connector pinout

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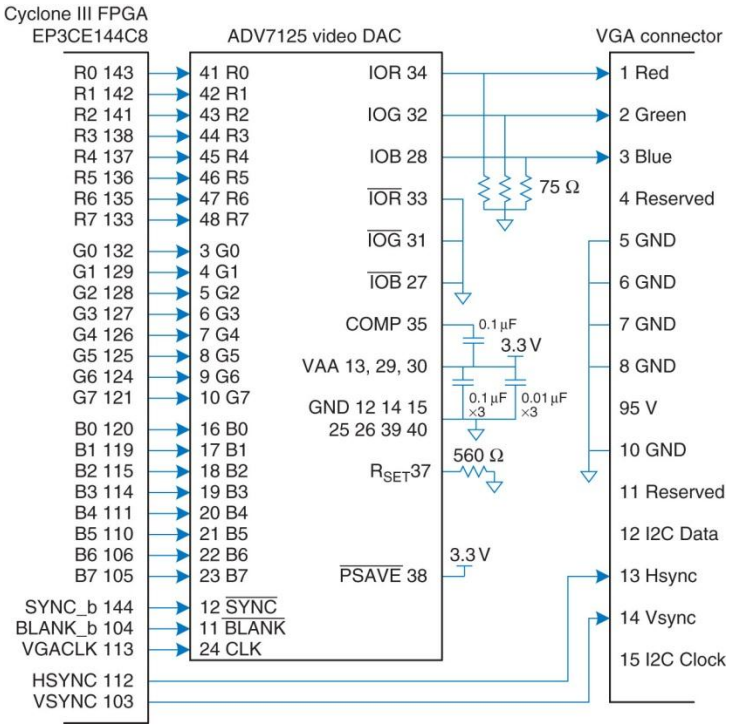

Figure 8.53 FPGA driving VGA cable through video DAC

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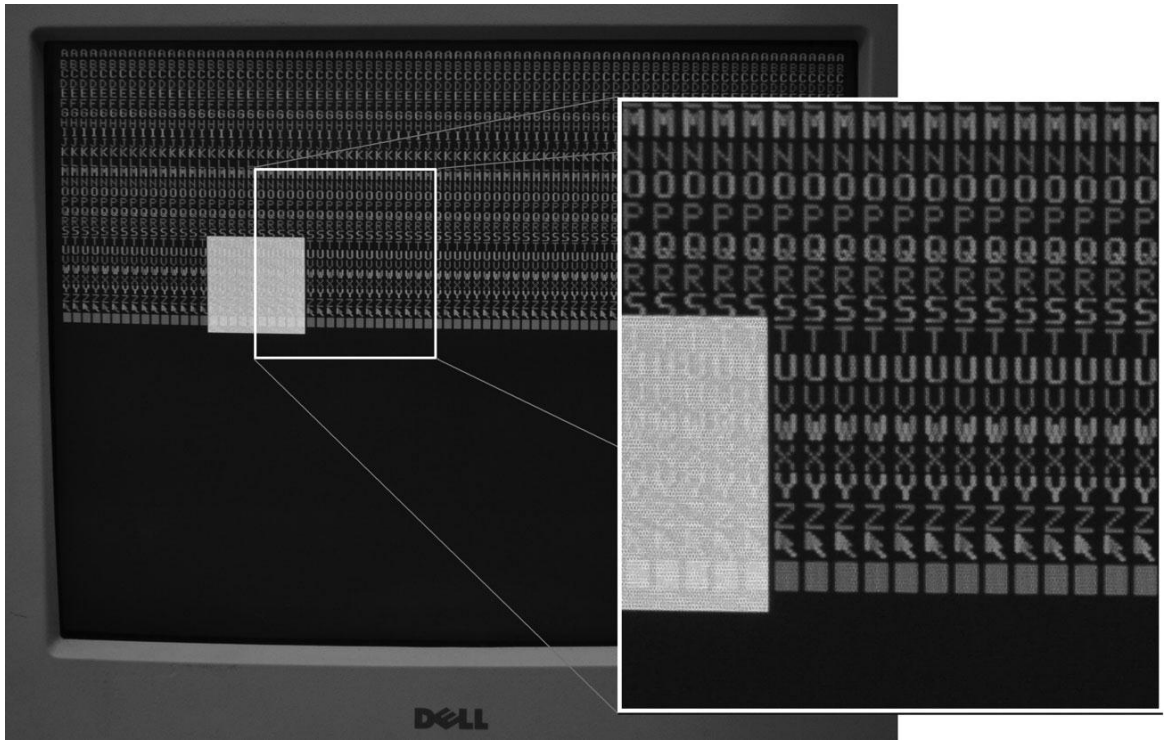

Figure 8.54 VGA output

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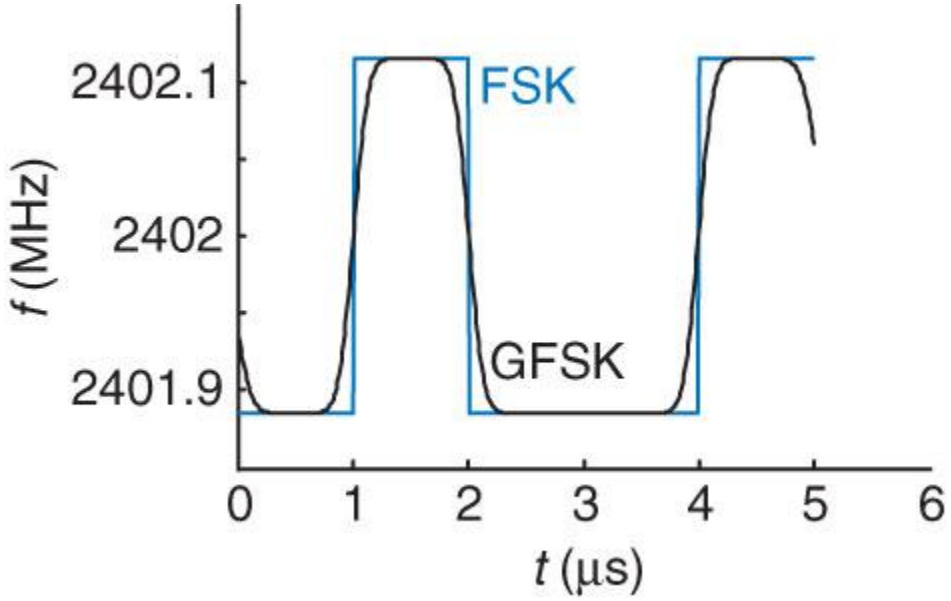

Figure 8.55 FSK and GFSK waveforms

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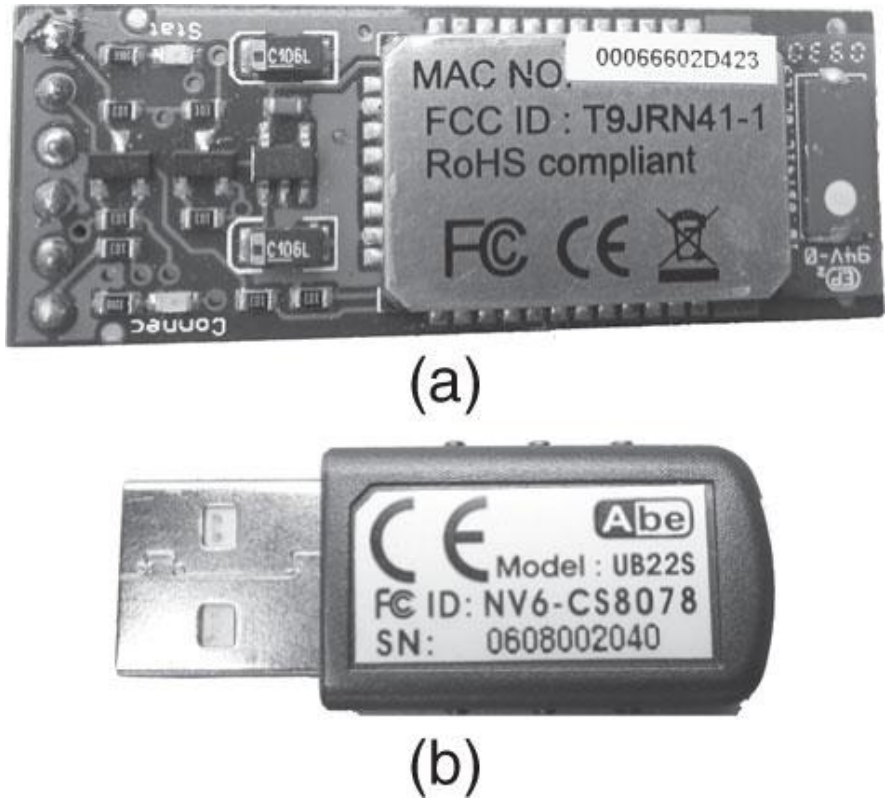

Figure 8.56 BlueSMiRF module and USB dongle

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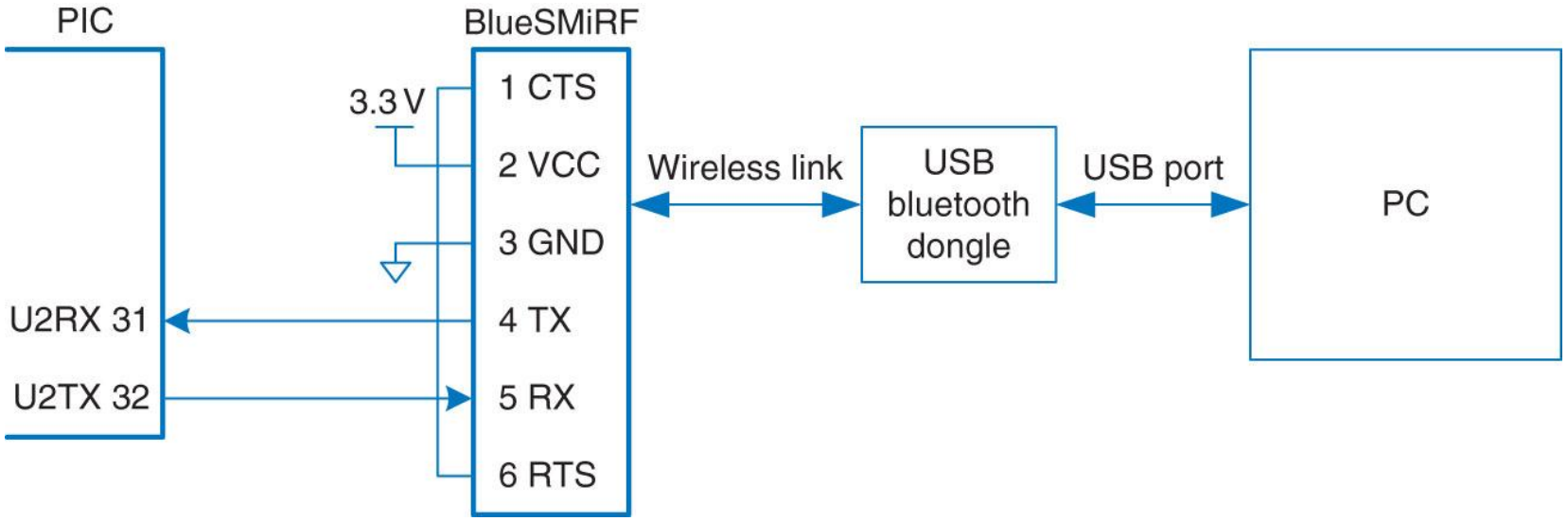

Figure 8.57 Bluetooth PIC32 to PC link

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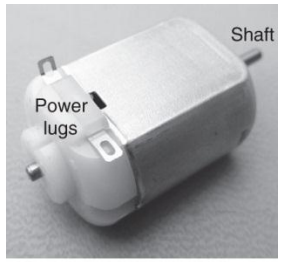
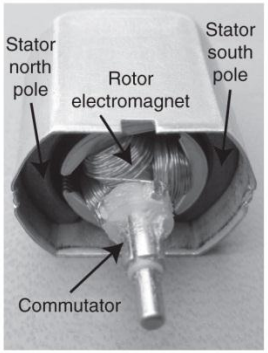
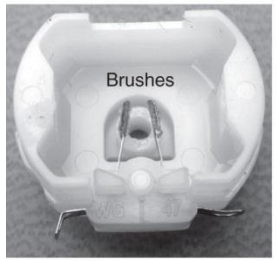


(a)



(b)



(c)

Figure 8.58 DC motor

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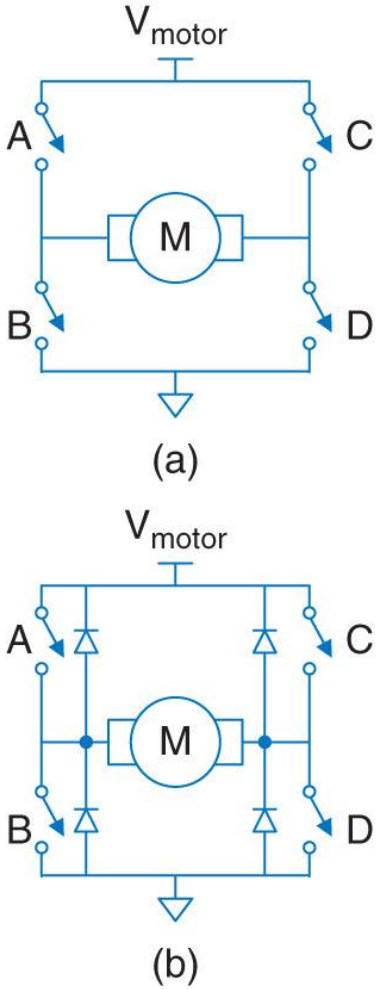

Figure 8.59 H-bridge

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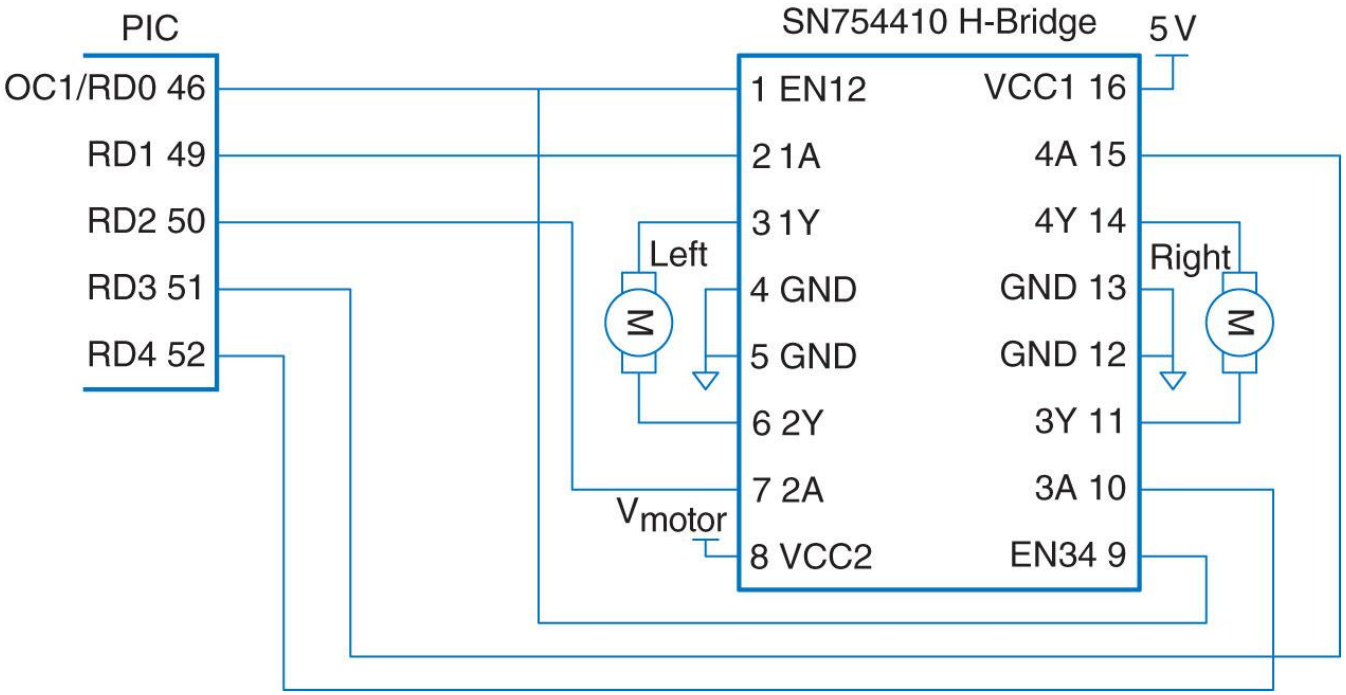

Figure 8.60 Motor control with dual H-bridge

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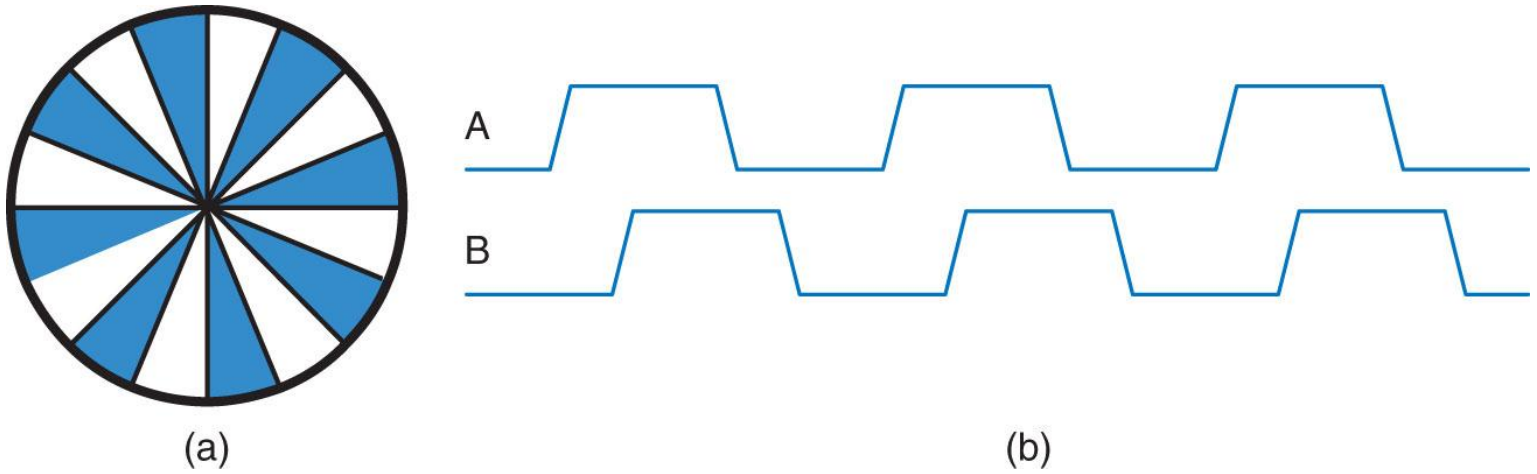

Figure 8.61 Shaft encoder (a) disk, (b) quadrature outputs

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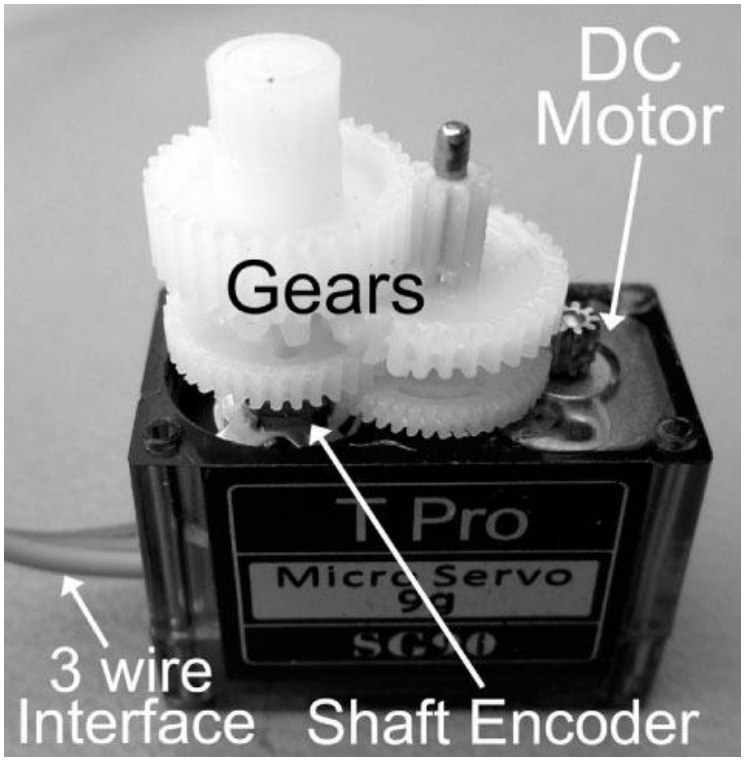

Figure 8.62 SG90 servo motor

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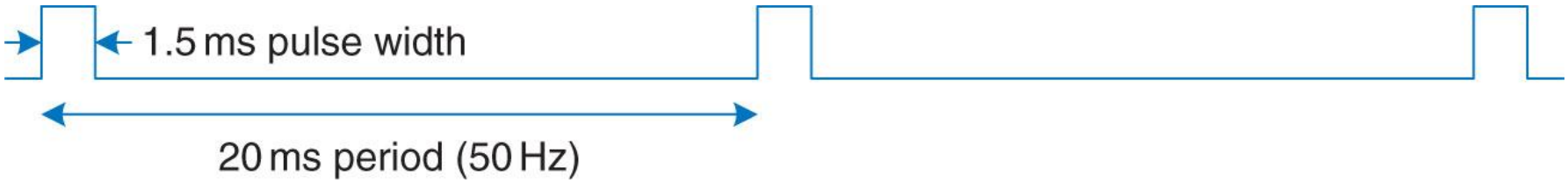

Figure 8.63 Servo control waveform

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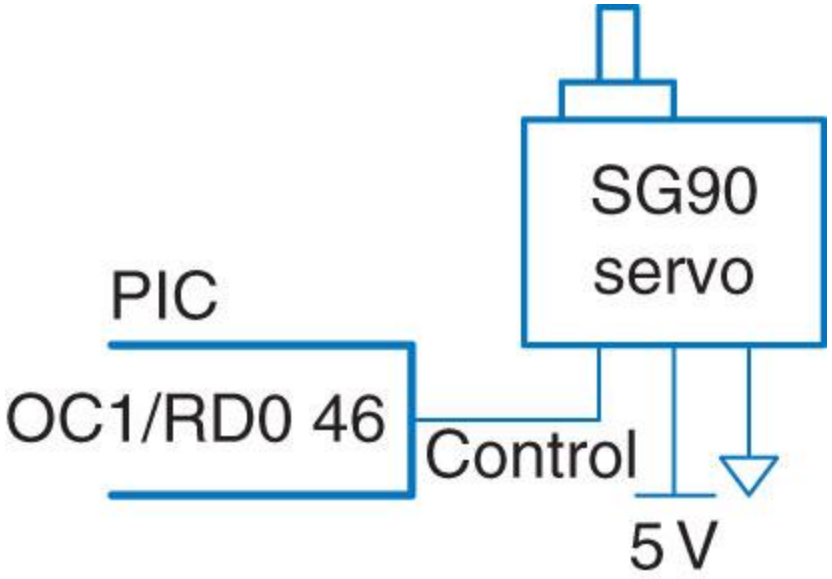

Figure 8.64 Servo motor control

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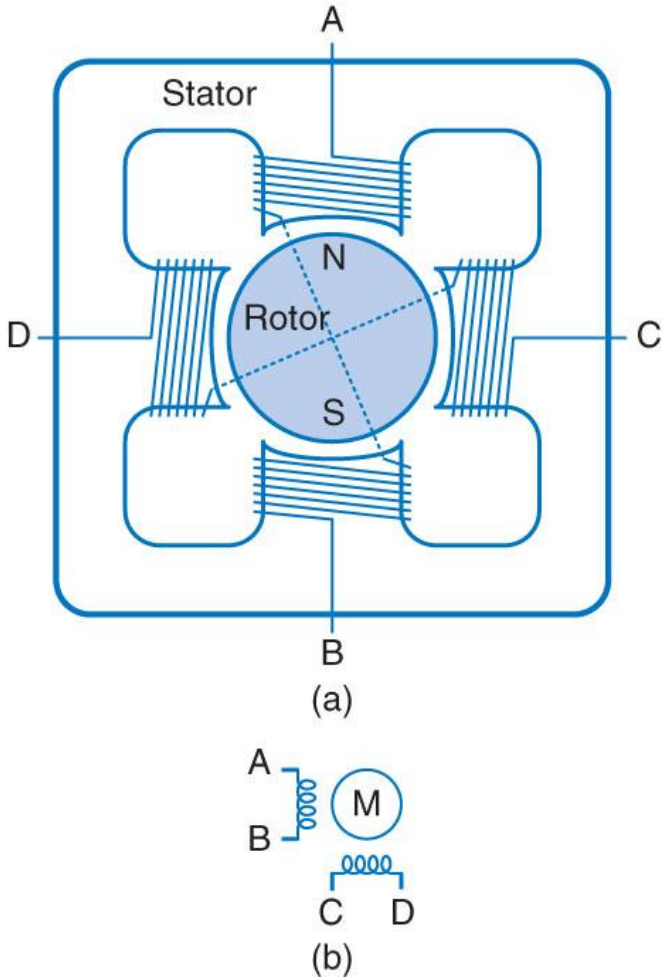

Figure 8.65 (a) Simplified bipolar stepper motor; (b) stepper motor symbol

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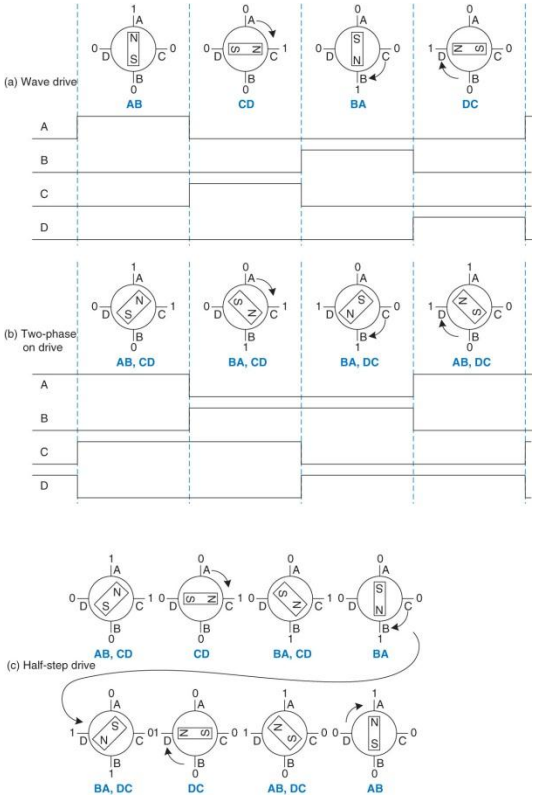

Figure 8.66 Bipolar motor drive

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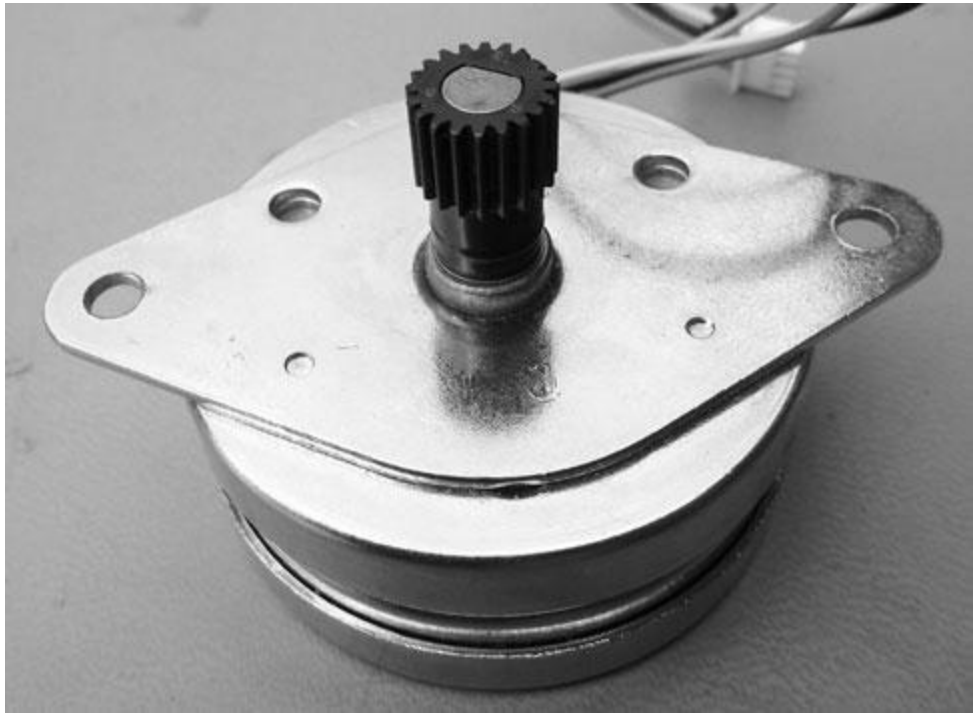

Figure 8.67 AIRPAX LB82773-M1 bipolar stepper motor

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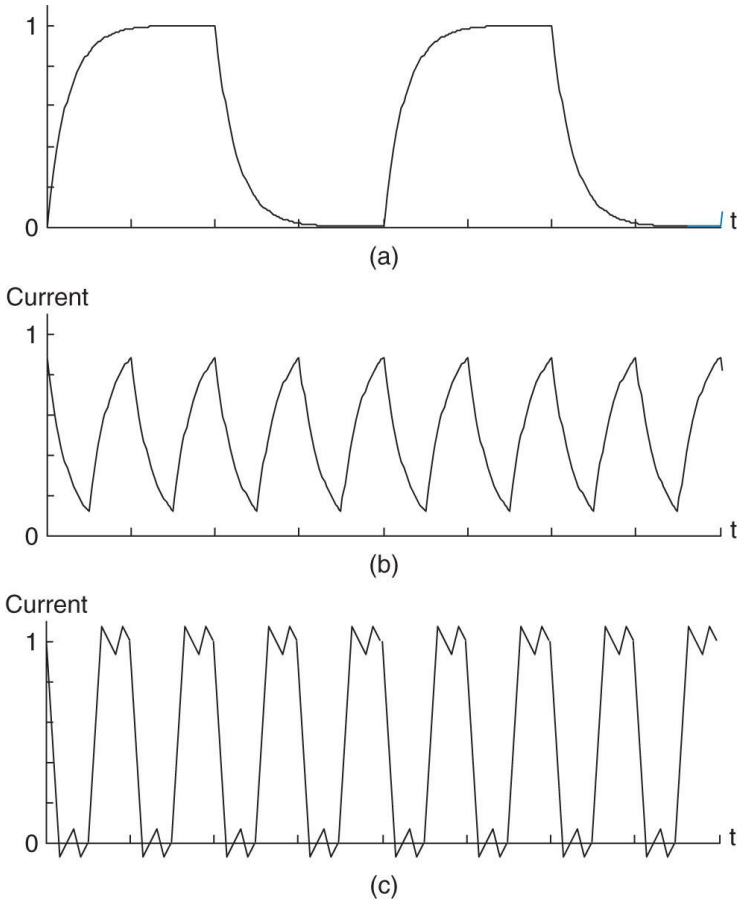

Figure 8.68 Bipolar stepper motor direct drive current: (a) slow rotation, (b) fast rotation, (c) fast rotation with chopper drive

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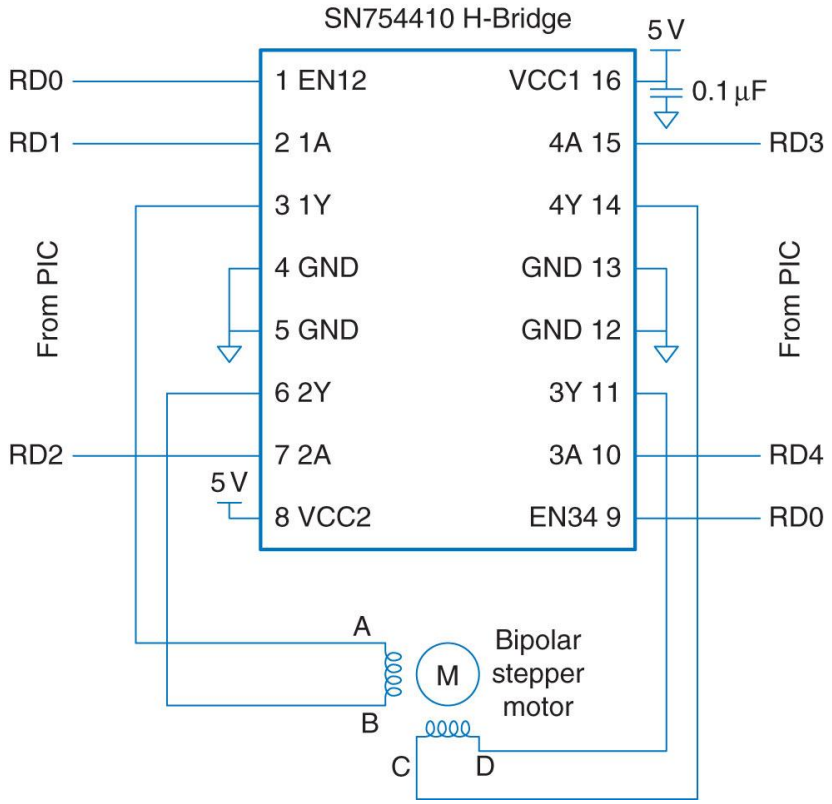

Figure 8.69 Bipolar stepper motor direct drive with H-bridge

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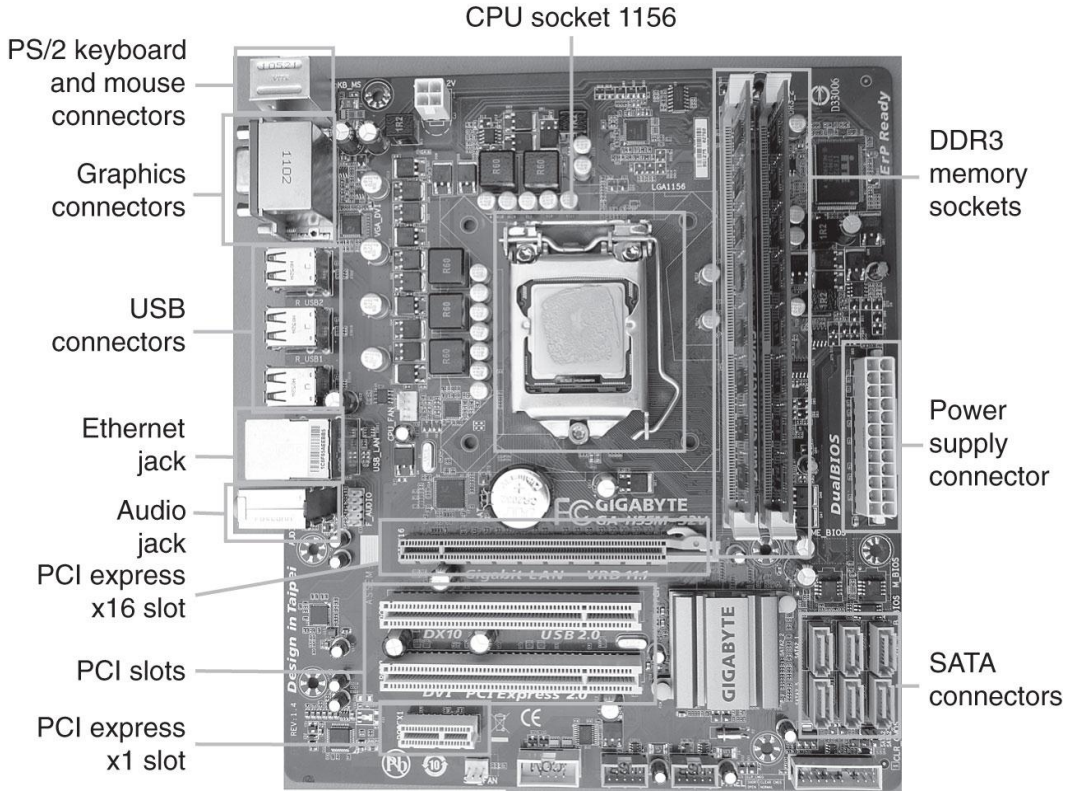

Figure 8.70 Gigabyte GA-H55M-S2V Motherboard

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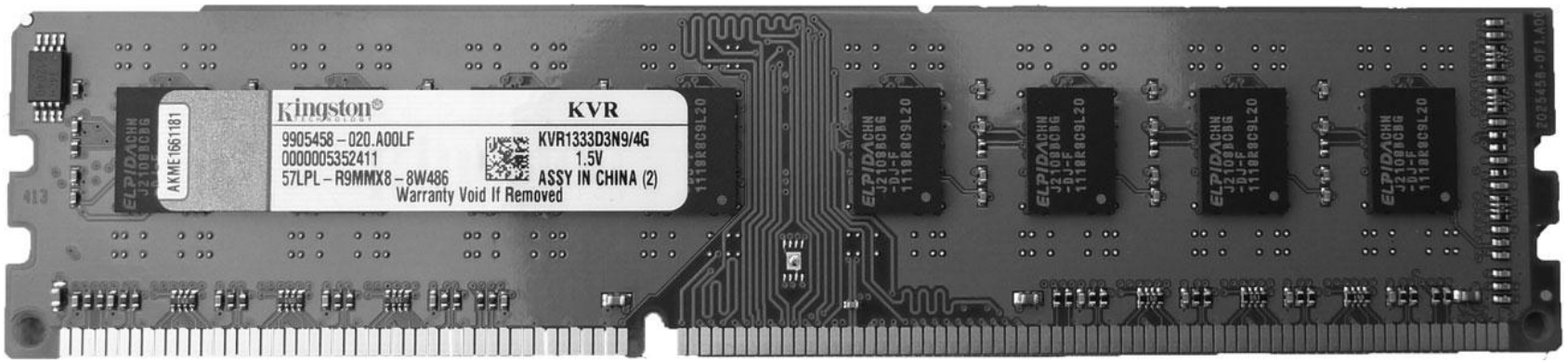

Figure 8.71 DDR3 memory module

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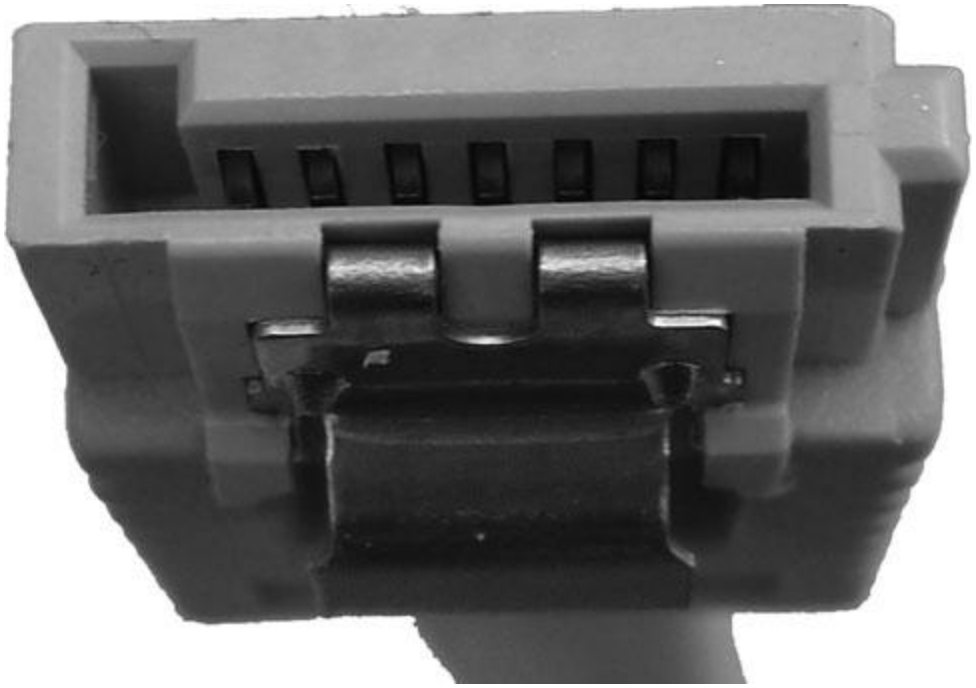

Figure 8.72 SATA cable

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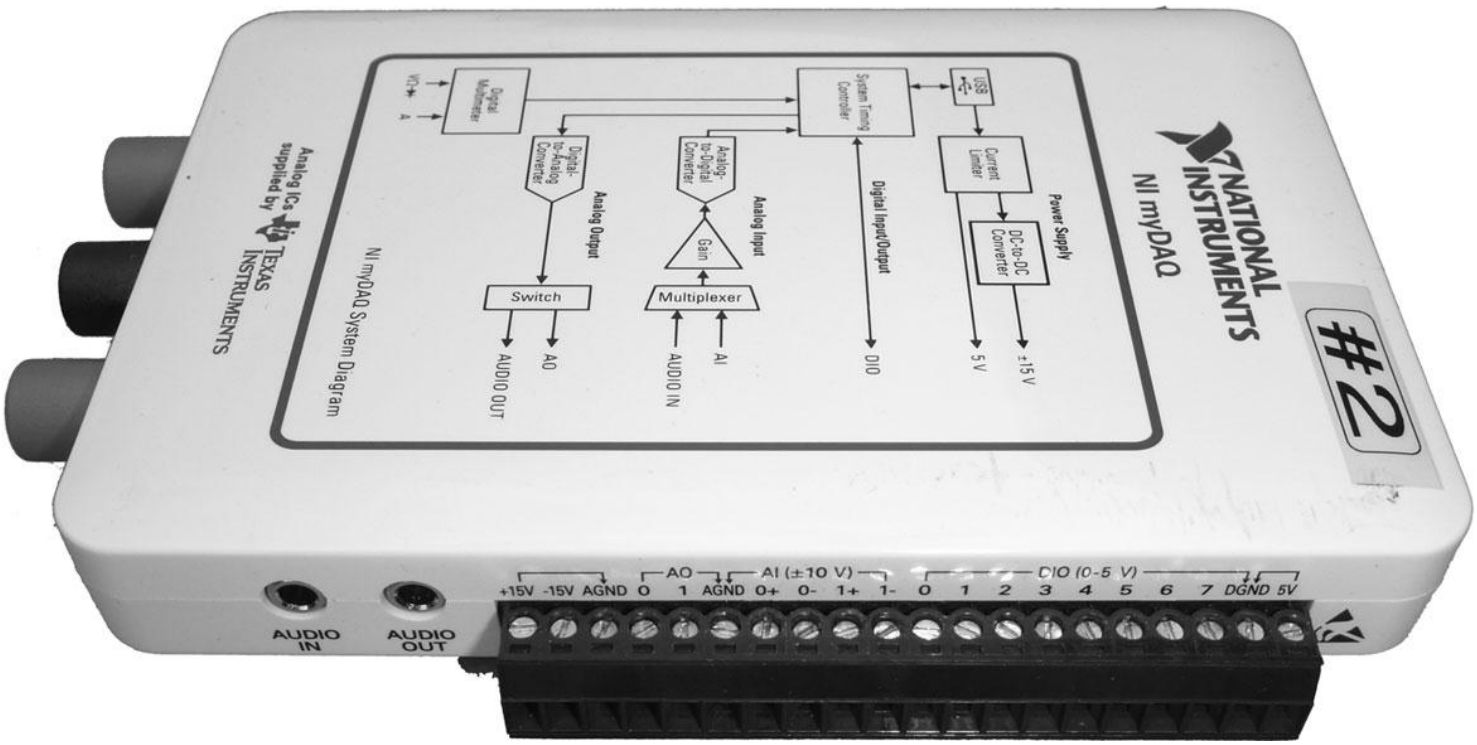

Figure 8.73 NI myDAQ

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Figure 8.74 FTDI USB to MPSSE cable
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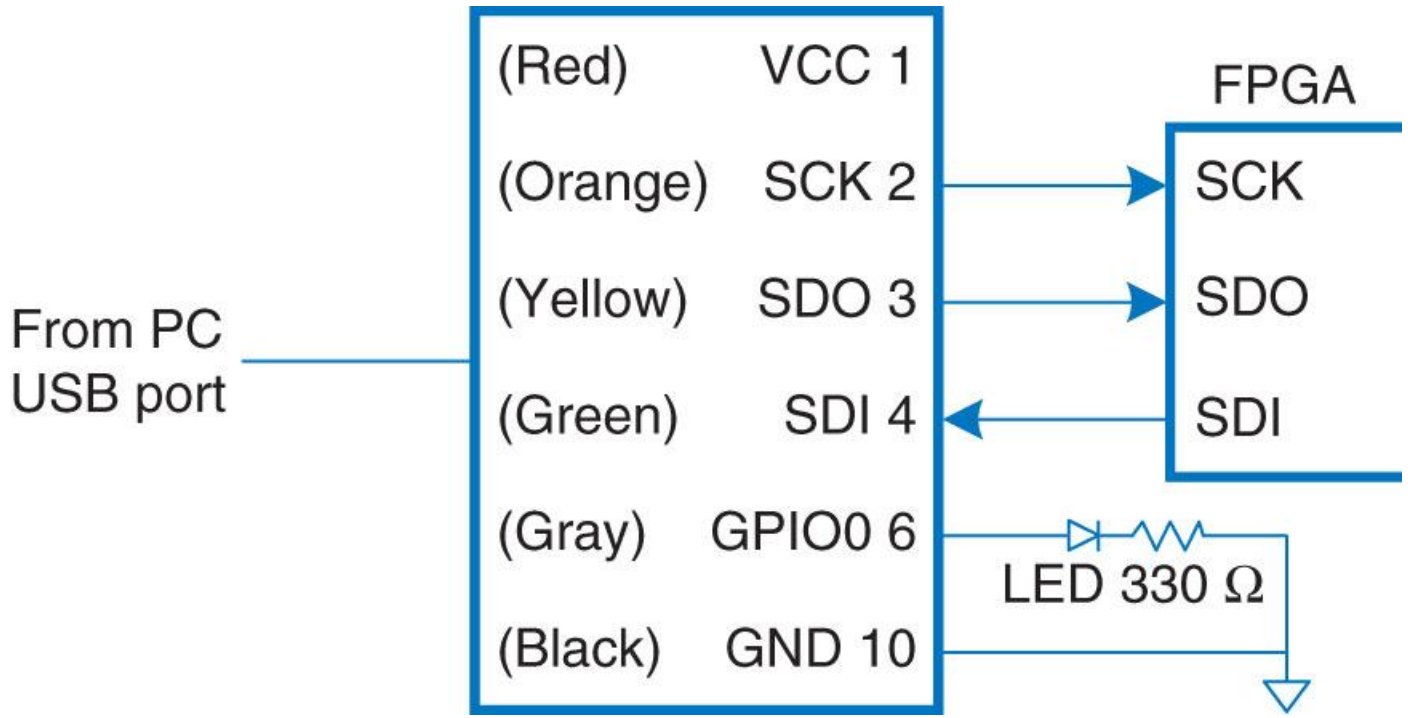

Figure 8.75 C232HM-DDHSL USB to MPSESE interface from PC to FPGA

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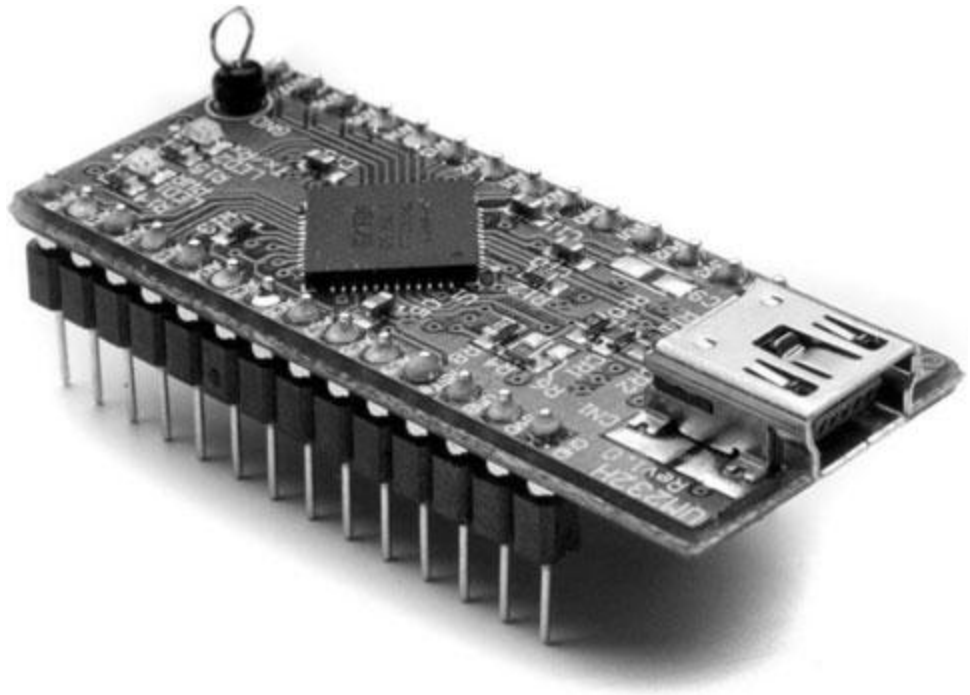

Figure 8.76 FTDI UM232H module
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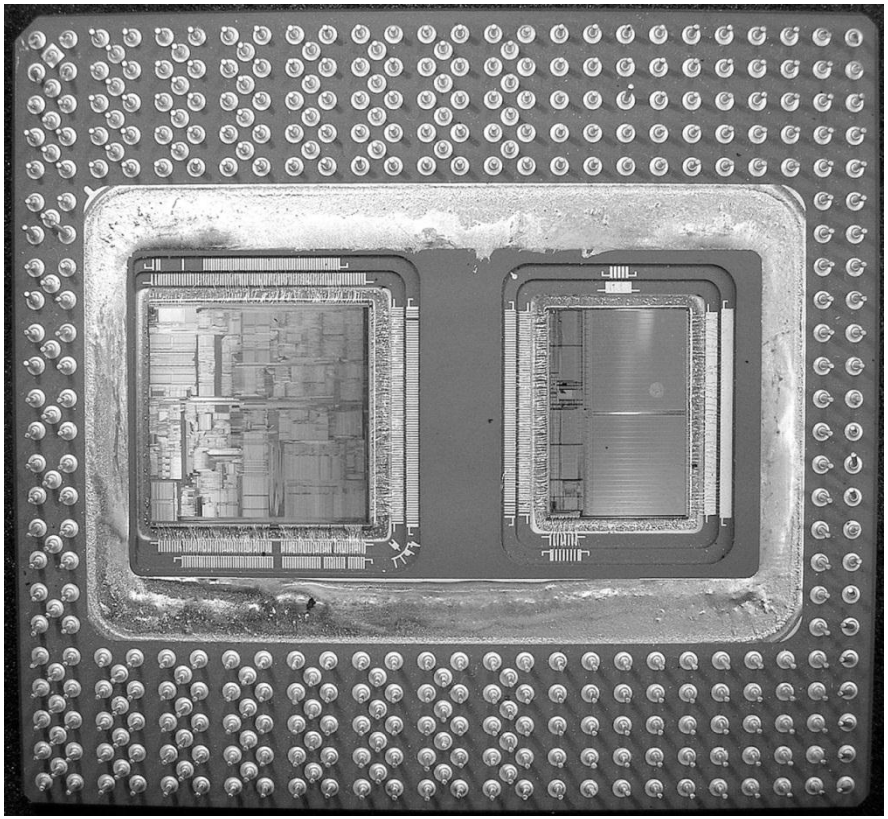

Figure 8.77 Pentium Pro multichip module with processor (left) and 256-KB cache (right) in a pin grid array (PGA) package
(Courtesy Intel.)

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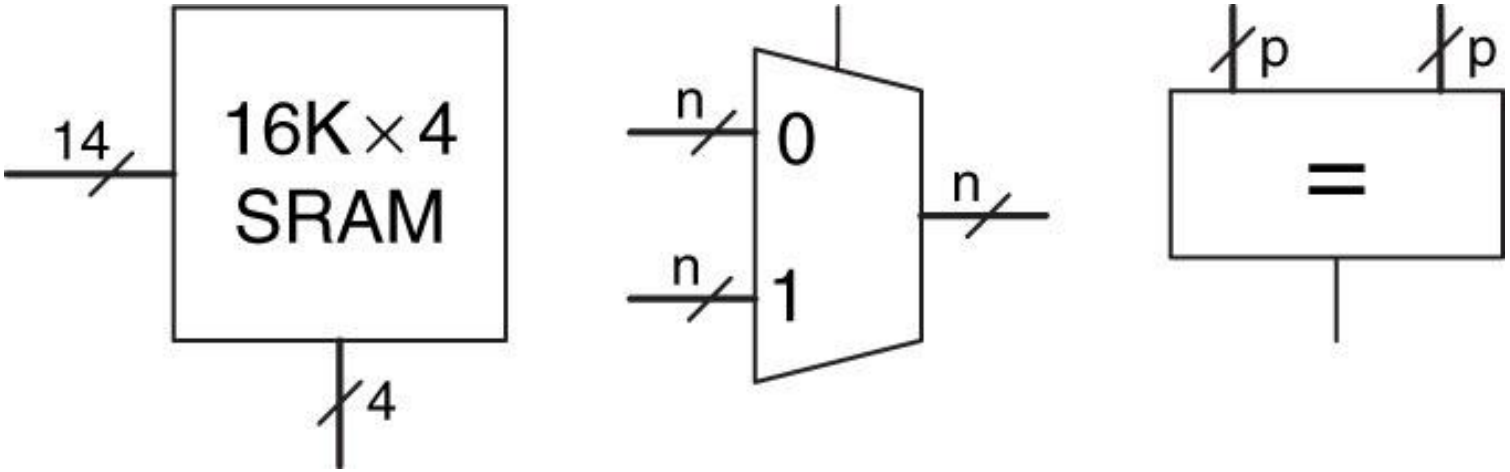

Figure 8.78 Building blocks

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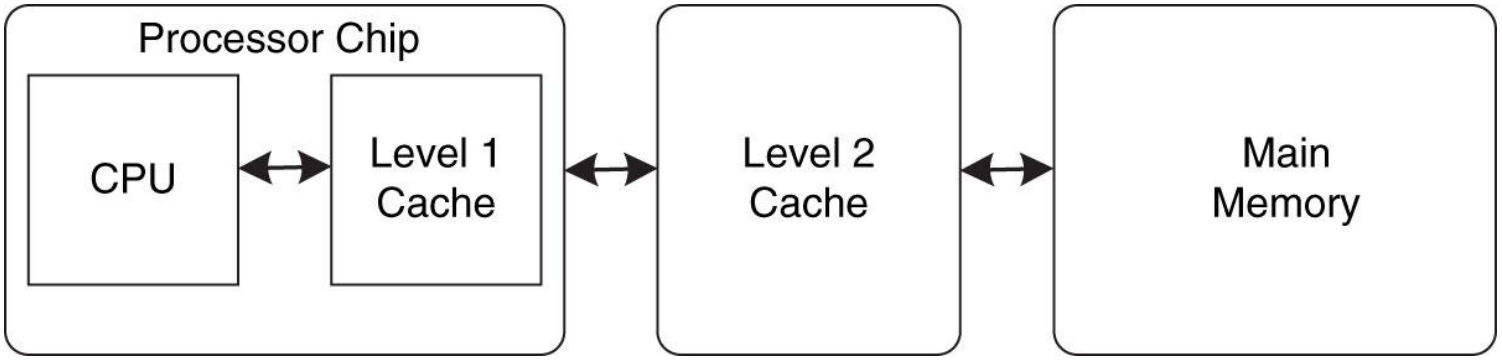

Figure 8.79 Computer system

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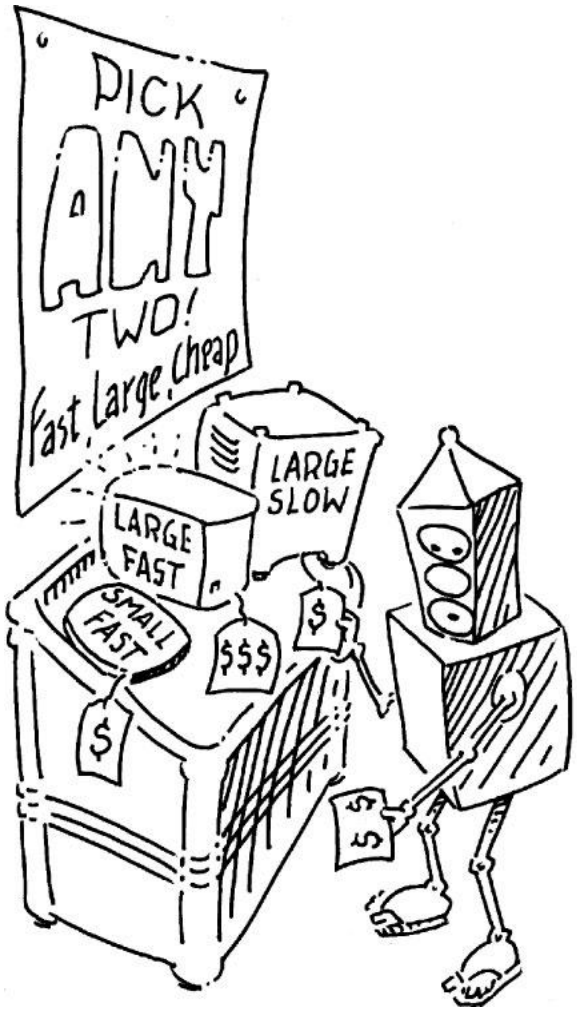

Figure M 01

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Figure M 02

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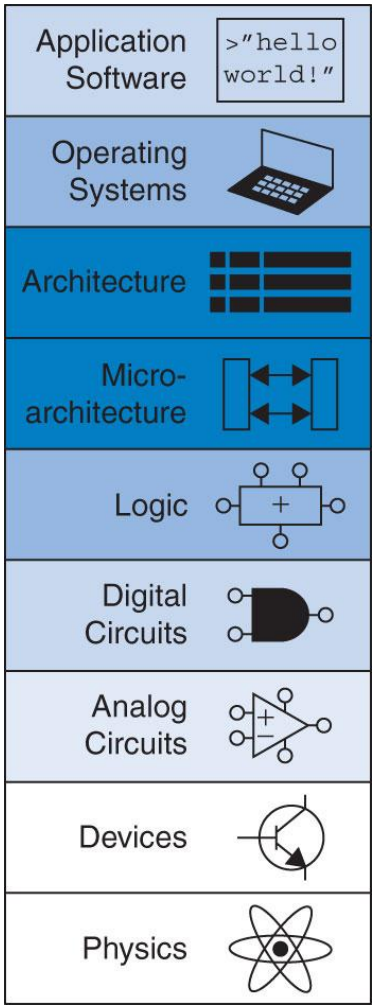

UNN Figure 1

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