Chapter 08

Synchronization

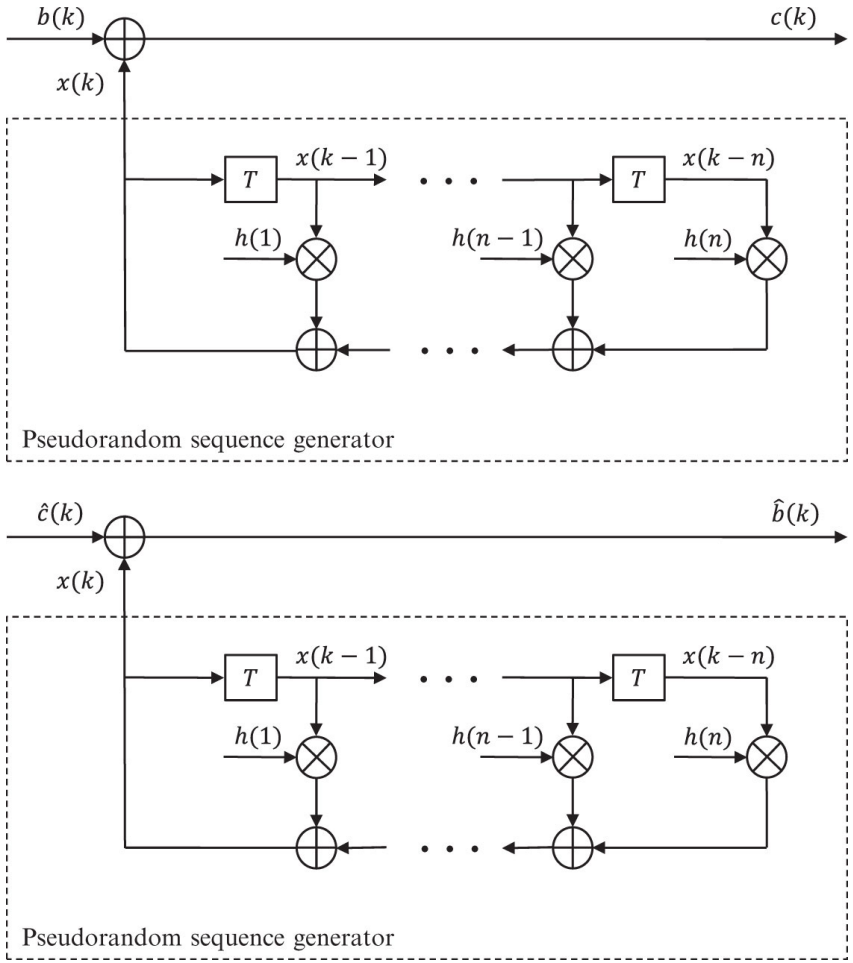

Figure 8.1 (a) A pseudorandom scrambler and (b) a pseudorandom descrambler.

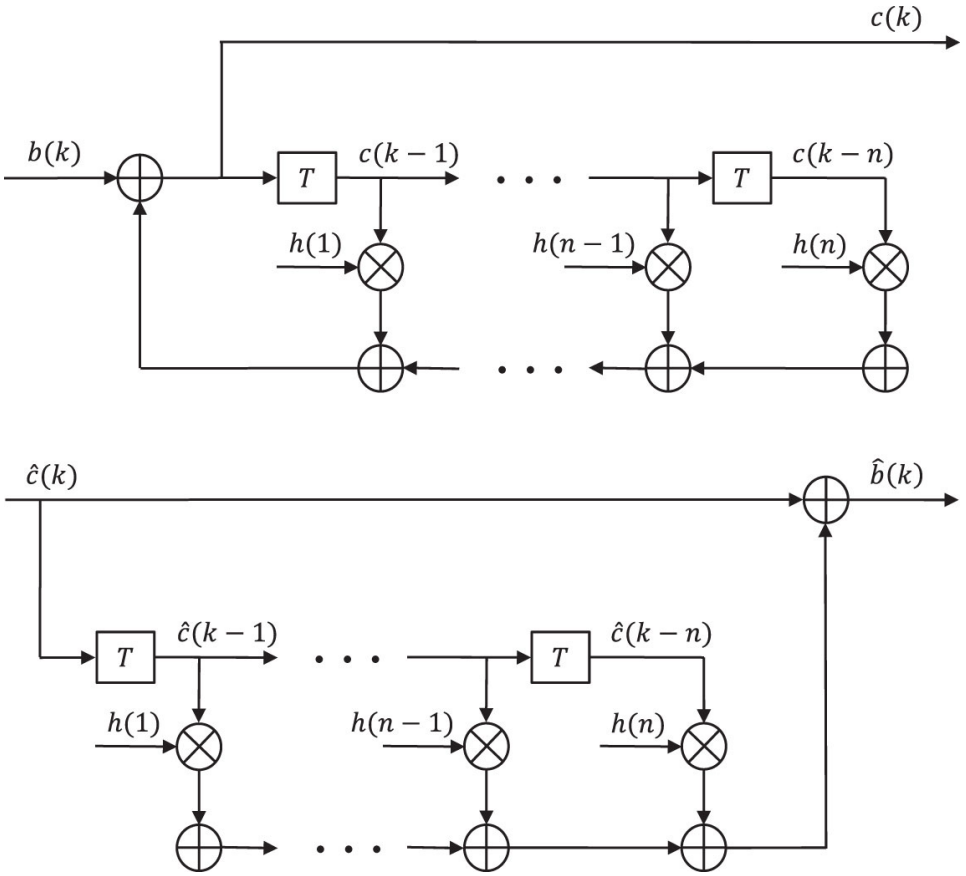

Figure 8.2 (a) A self-synchronizing scrambler and (b) a self-synchronizing descrambler.

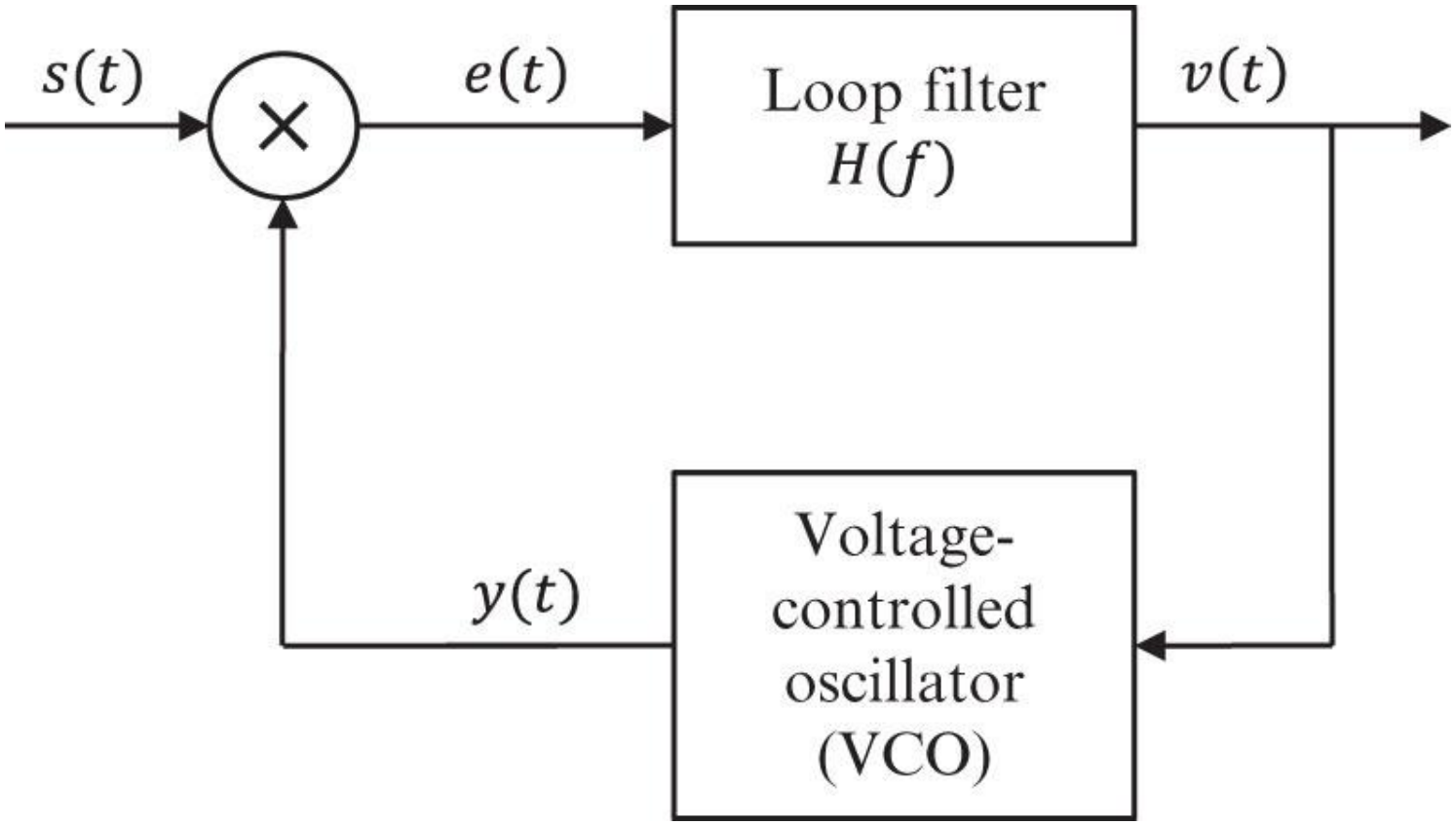

Figure 8.3 Basic components of a phase-locked loop.

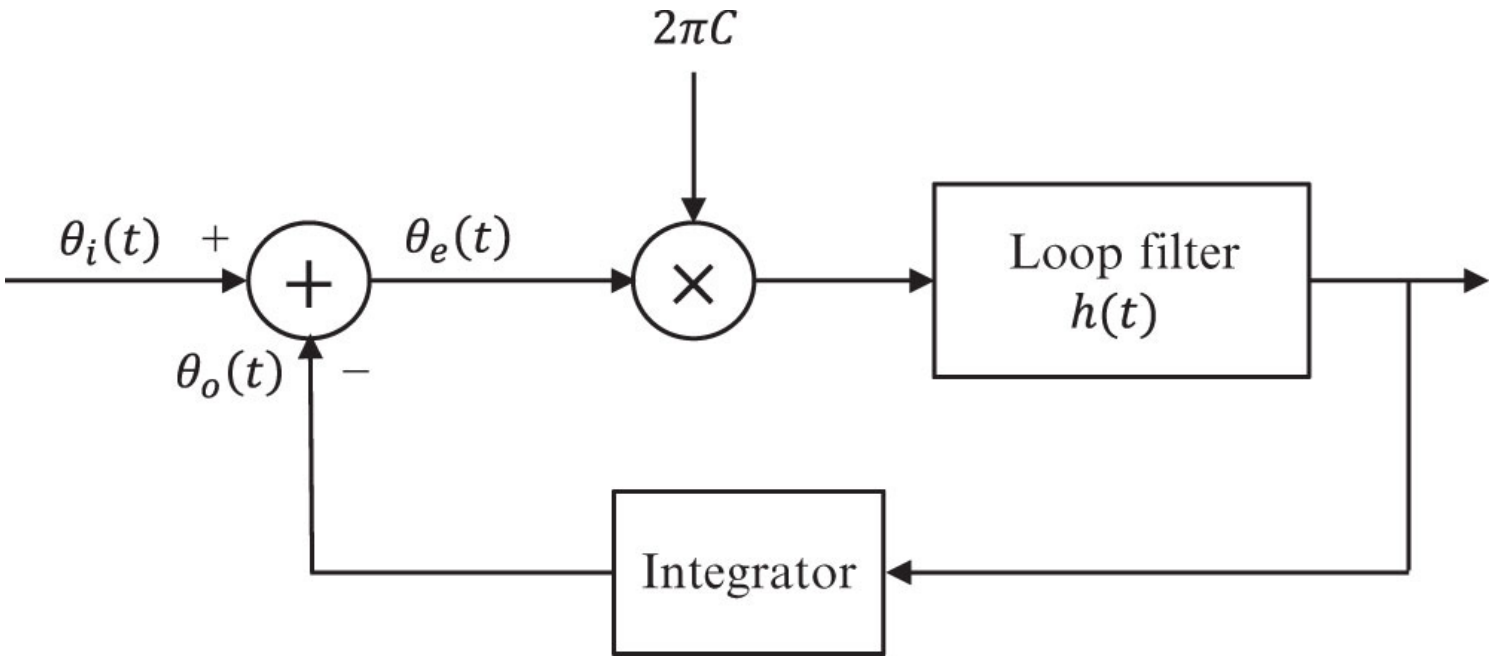

Figure 8.4 Linearized model of a phased-locked loop.

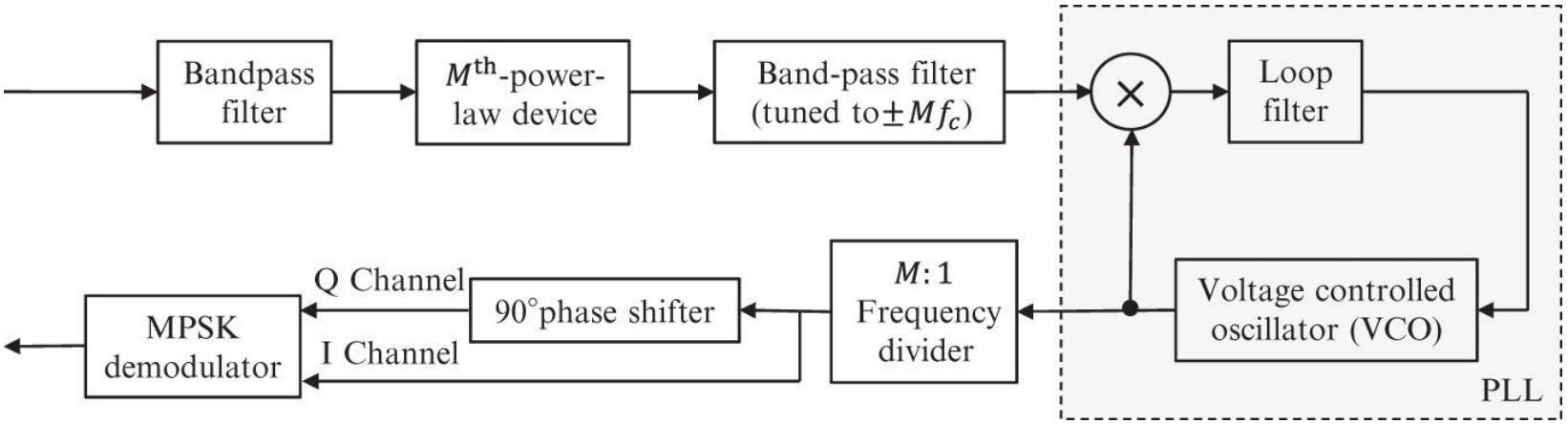

Figure 8.5 M^{th} power loop for carrier recovery for MPSK.

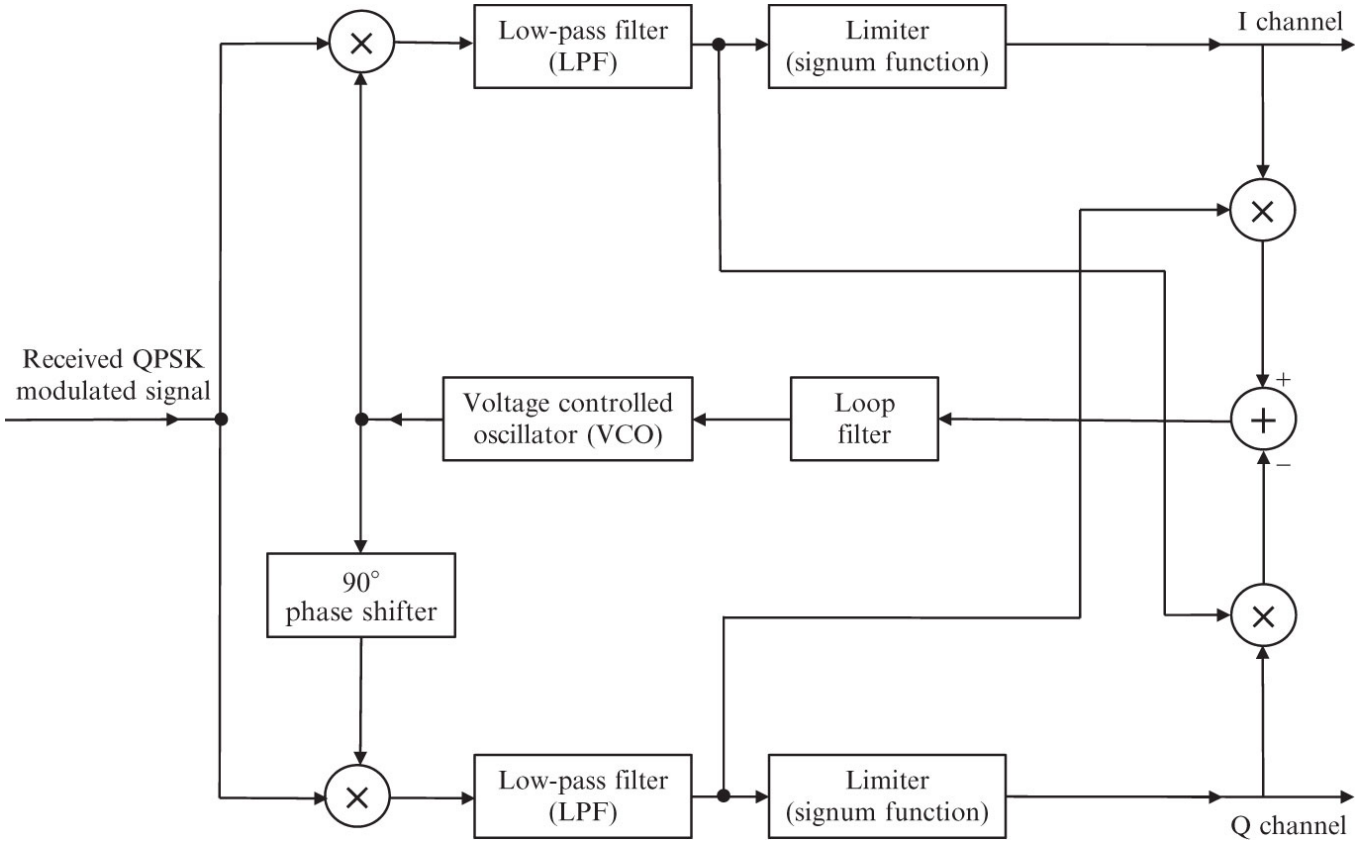

Figure 8.6 Costas loop for carrier recovery for QPSK.

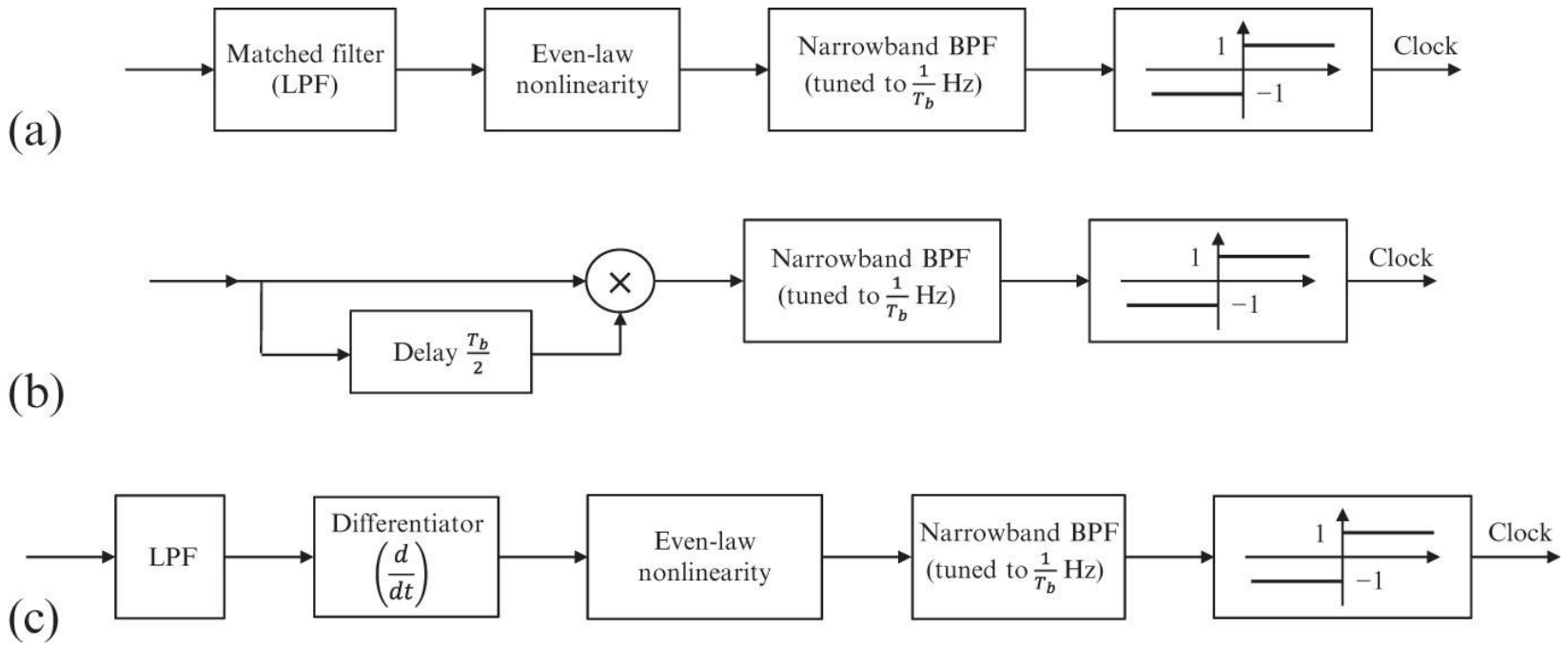

Figure 8.7 Nonlinear filter symbol synchronizer: (a) even-law-based, (b) correlation-based, and (c) differentiation-based.

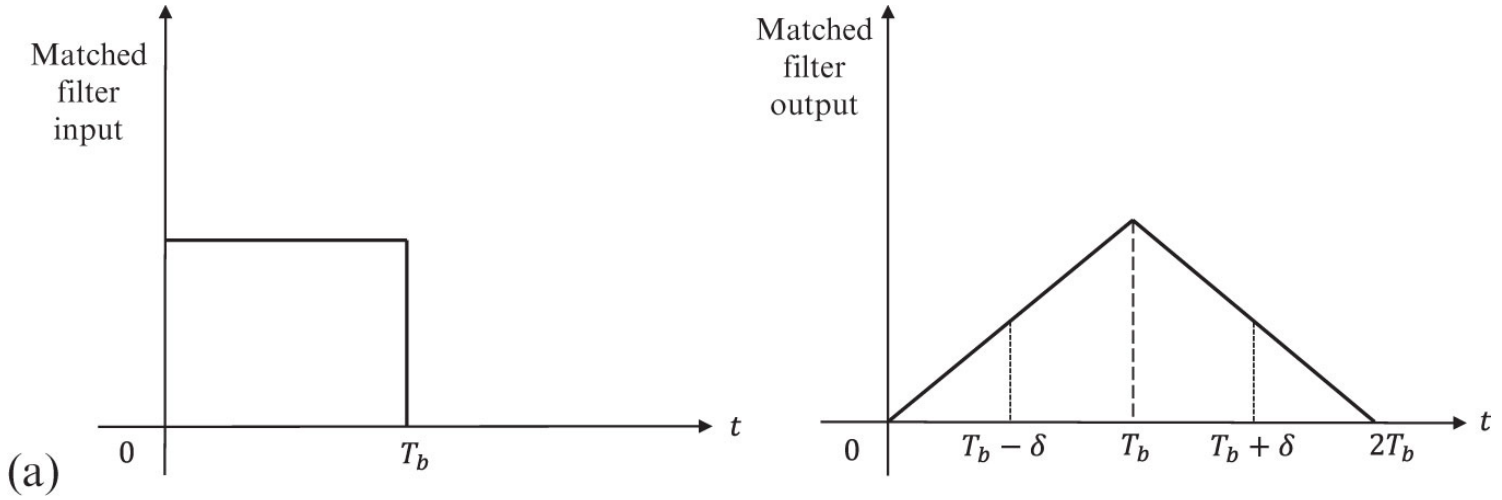

Figure 8.8a Early-late gate symbol synchronizer: (a) matched-filter input and output and (b) block diagram.

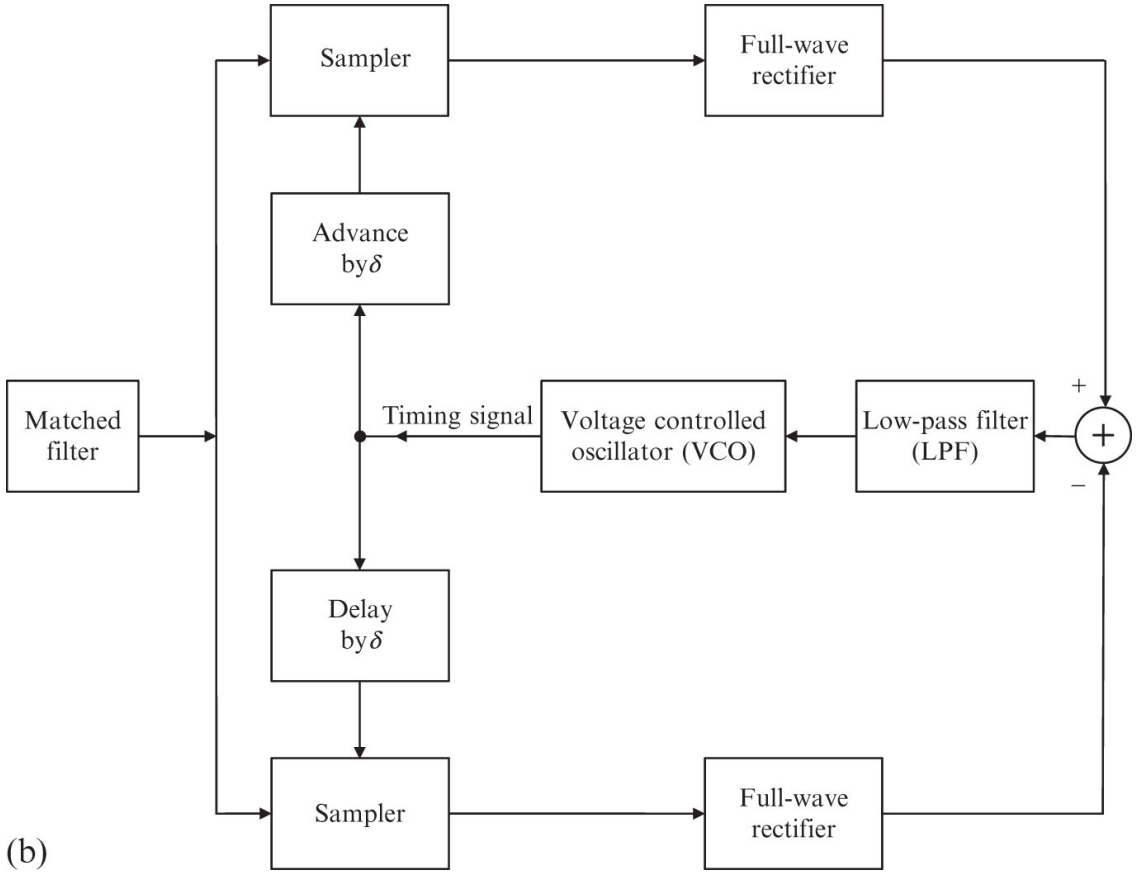

Figure 8.8b Early-late gate symbol synchronizer: (a) matched-filter input and output and (b) block diagram.