Graphical Representations of DSP Instructions

This appendix contains graphical representations of the Enhanced DSP instructions in ARM Cortex®-M4 Processor. See section 5.7 for details, and appendix section A.2 for summaries.

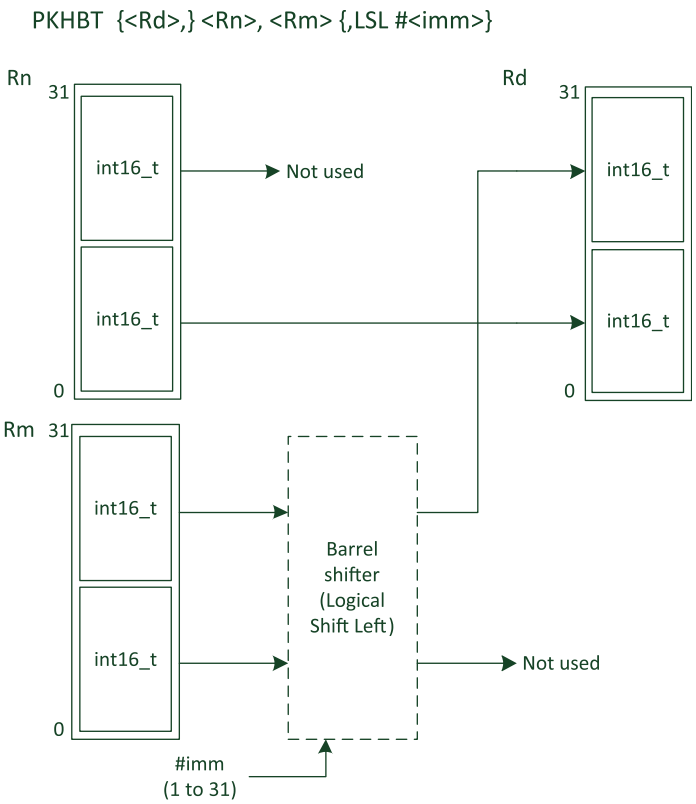

FIGURE B.1

PKHBT

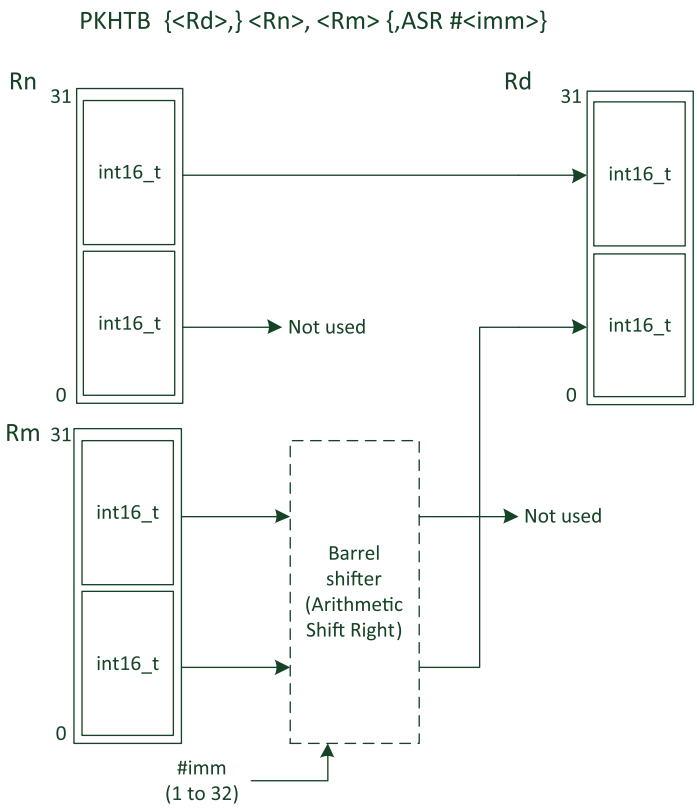

FIGURE B.2

PKHTB

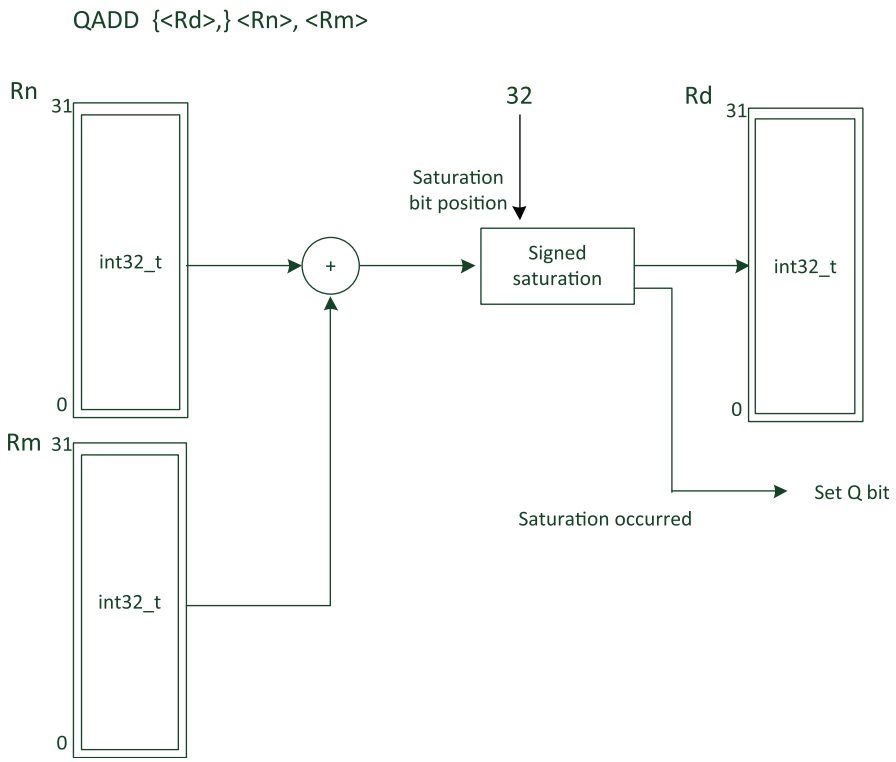

FIGURE B.3

QADD

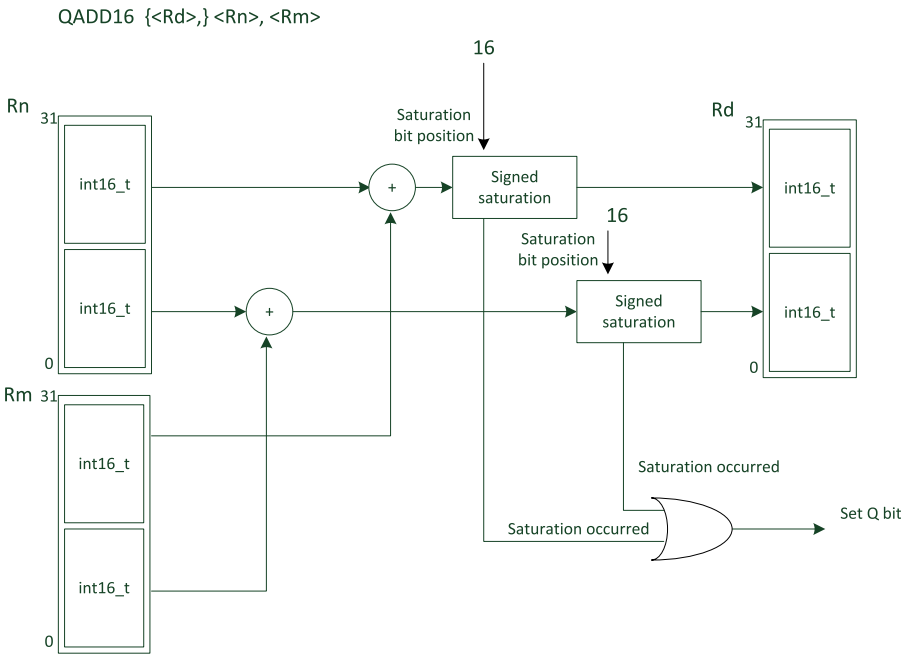

FIGURE B.4

QADD16

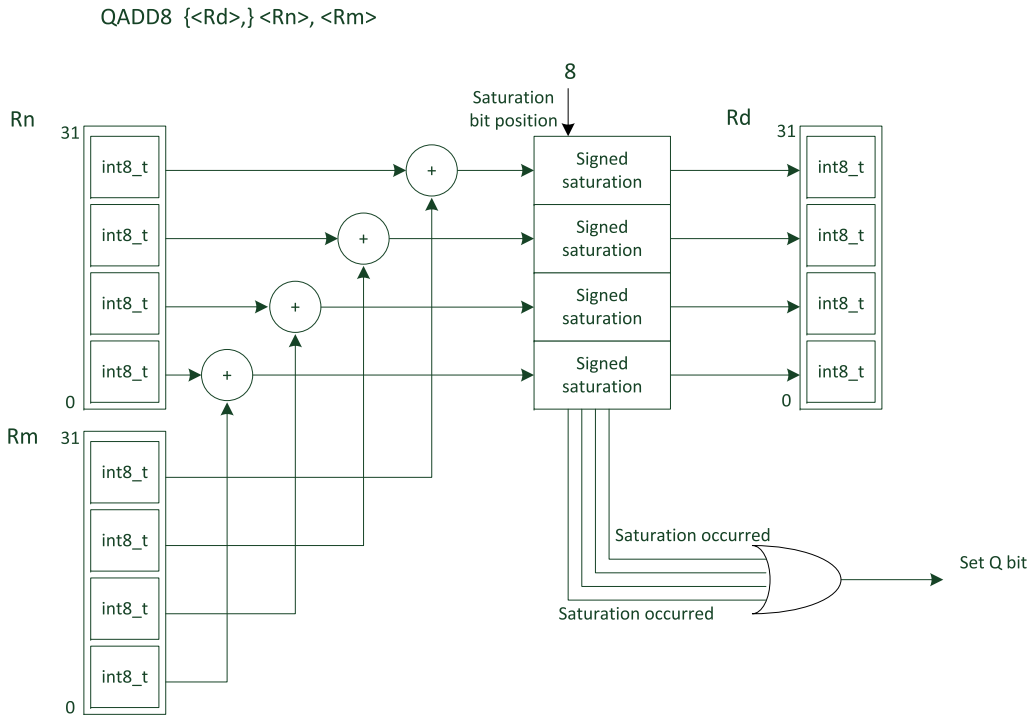

FIGURE B.5

QADD8

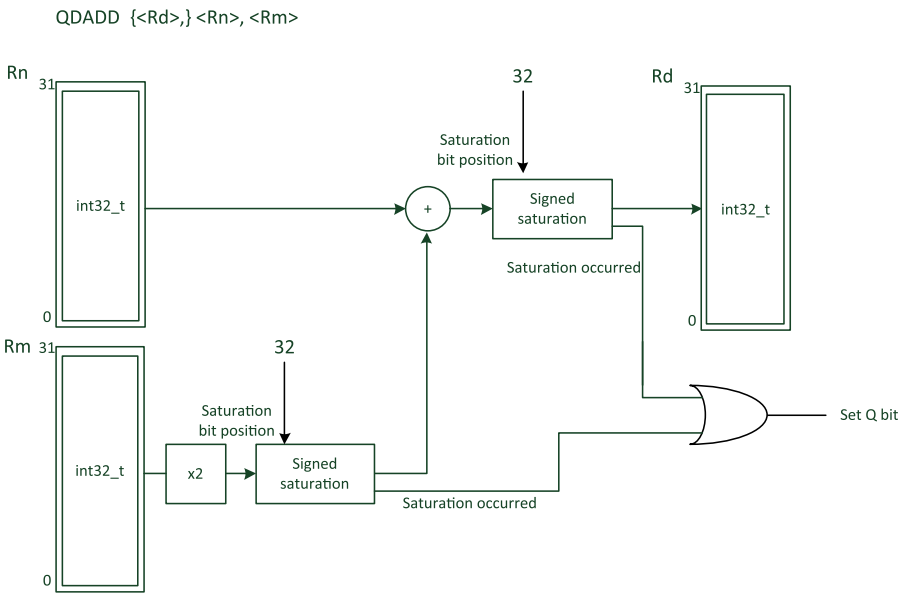

FIGURE B.6

QDADD

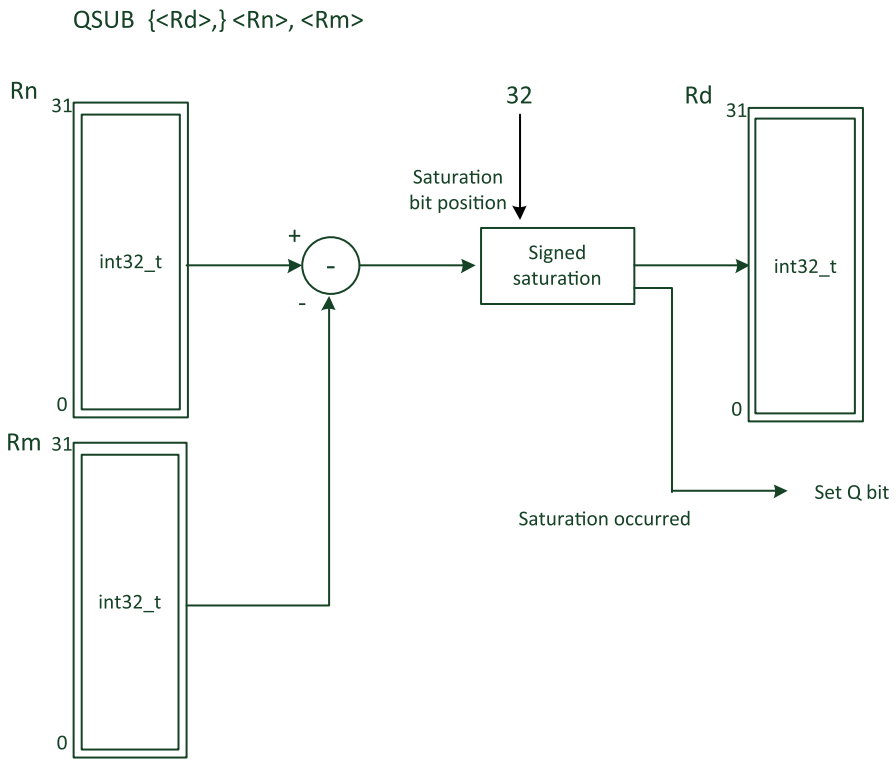

FIGURE B.7

QSUB

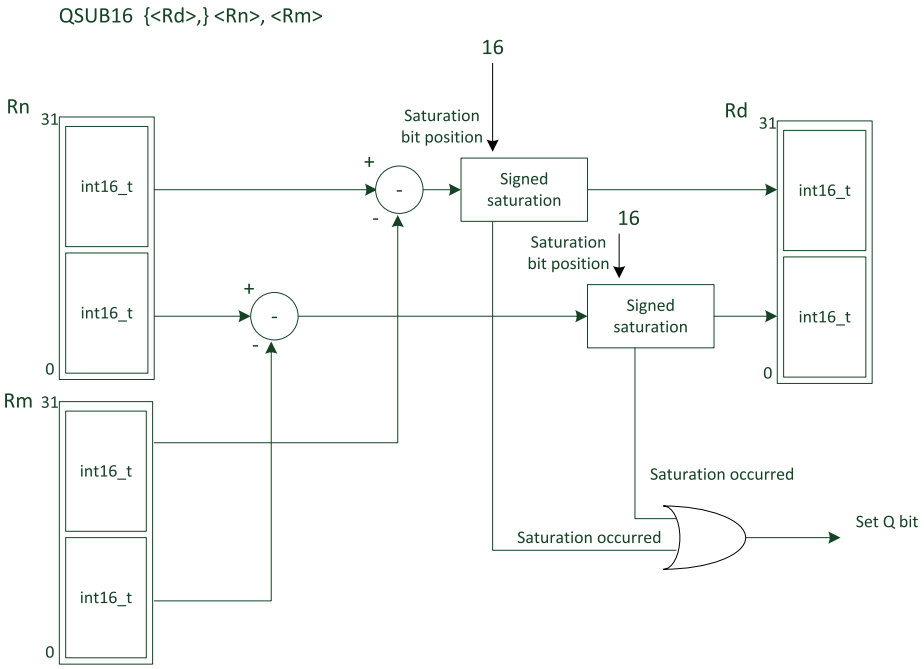

FIGURE B.8

QSUB16

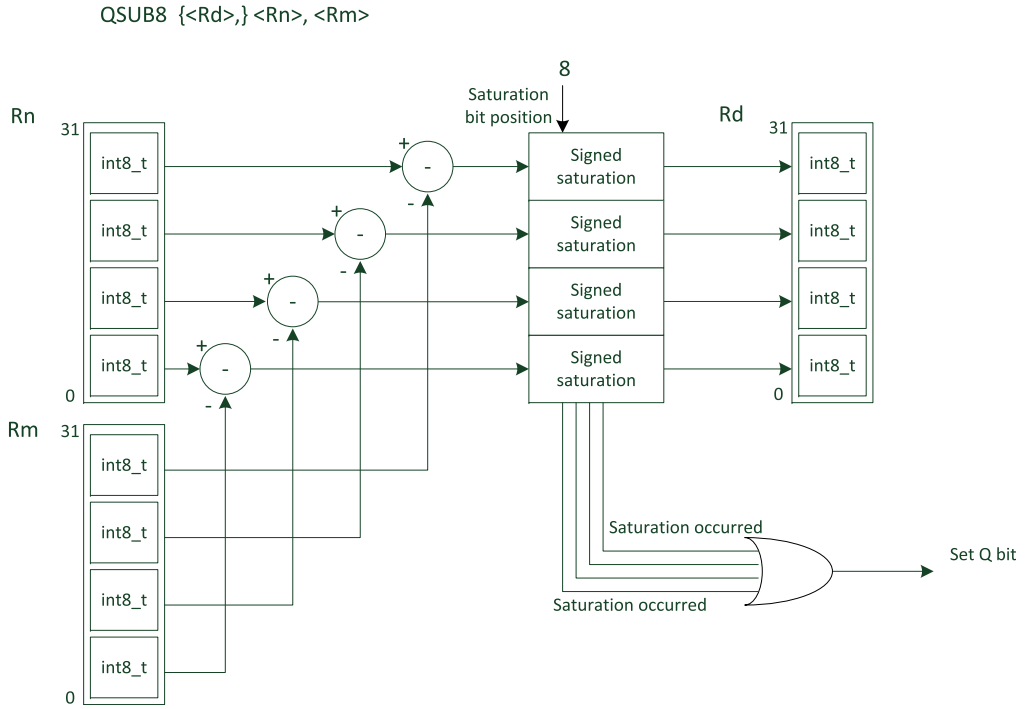

FIGURE B.9

QSUB8

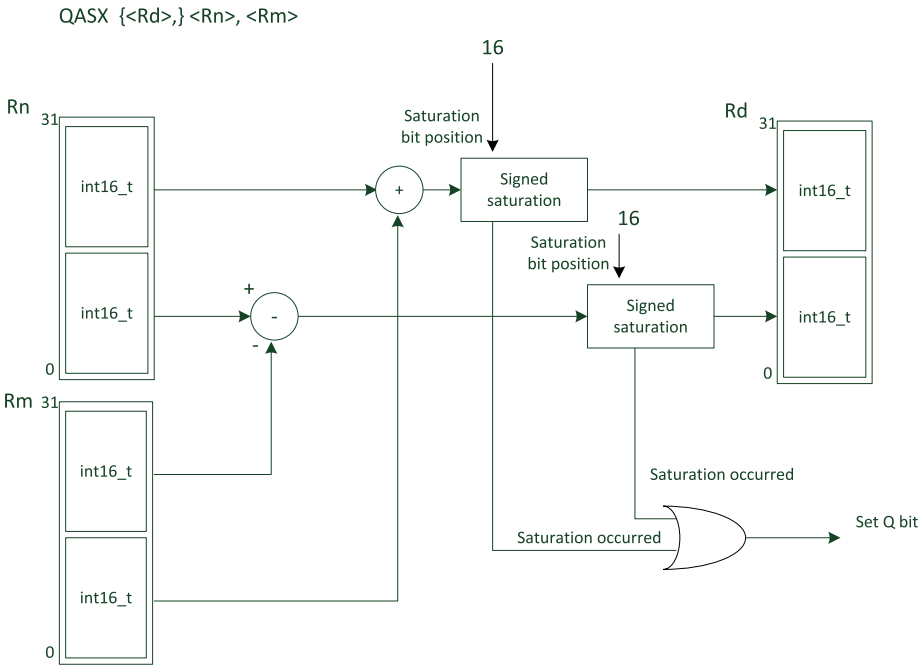

FIGURE B.10

QASX

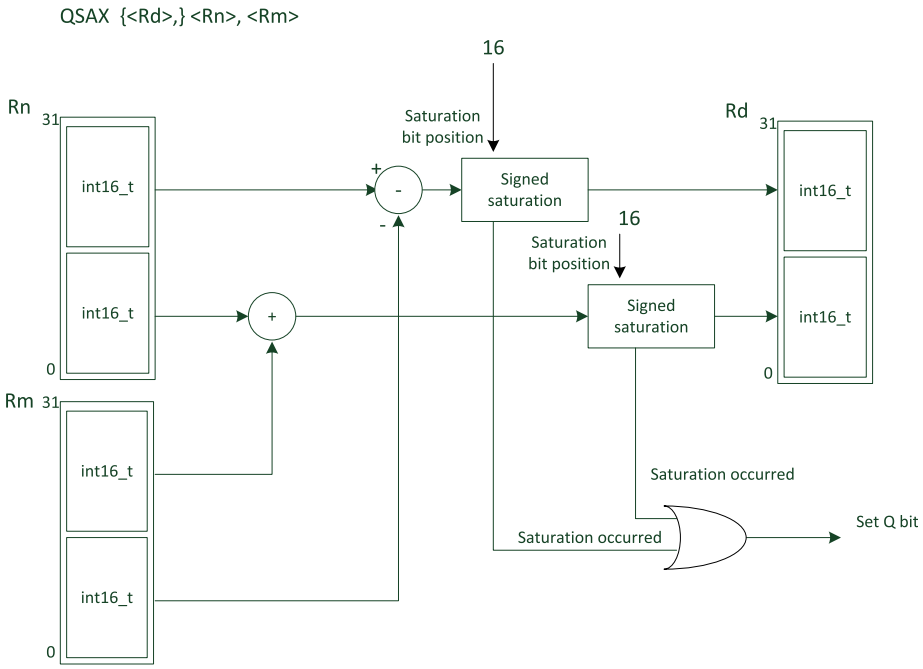

FIGURE B.11

QSAX

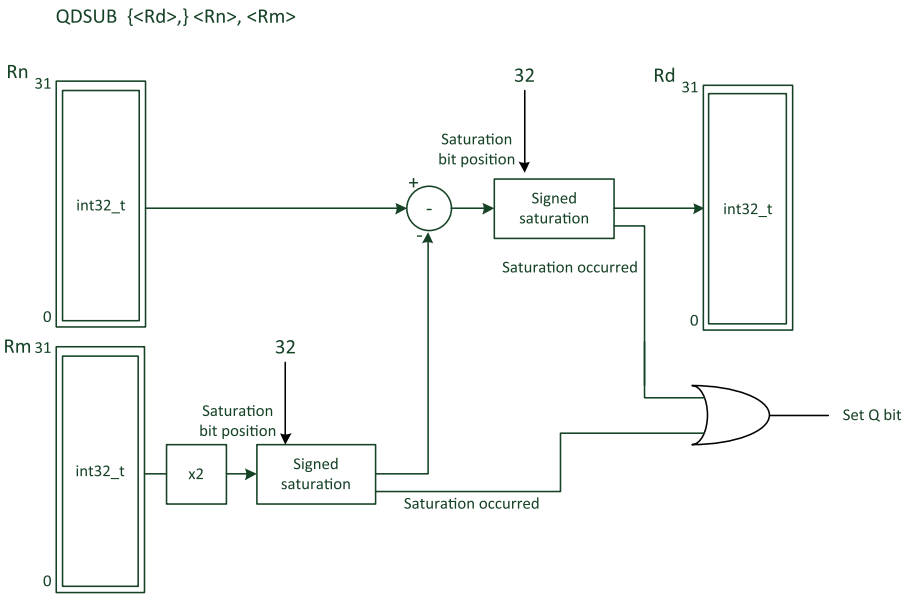

FIGURE B.12

QDSUB

SADD8 {<Rd>,} <Rn>, <Rm>

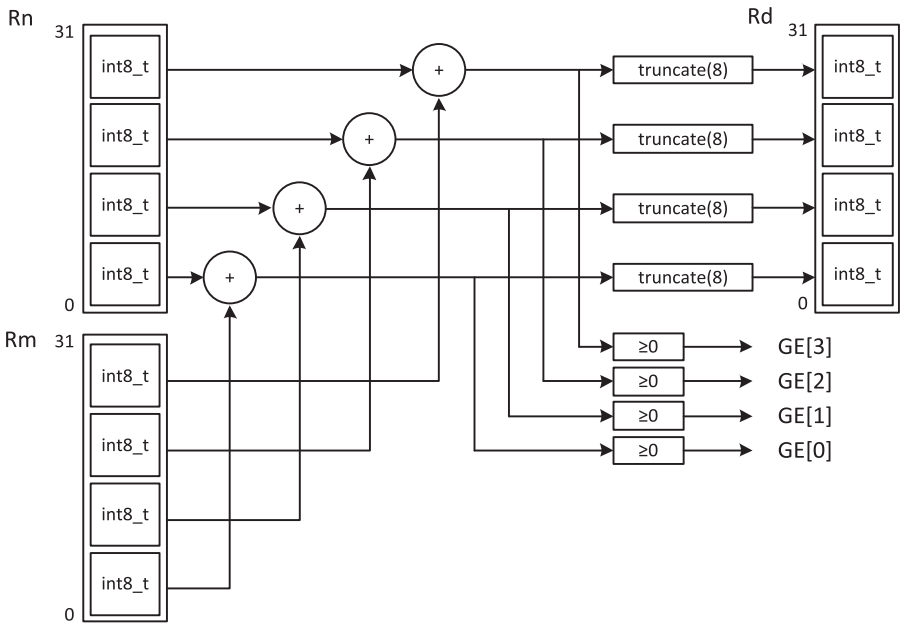

FIGURE B.13

SADD8

SADD16 {<Rd>,} <Rn>, <Rm>

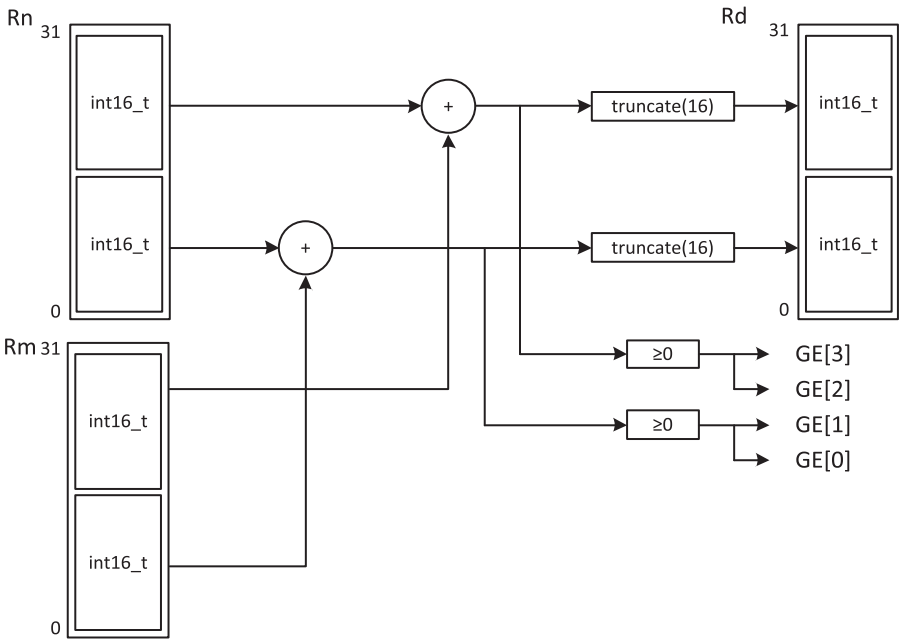

FIGURE B.14

SADD16

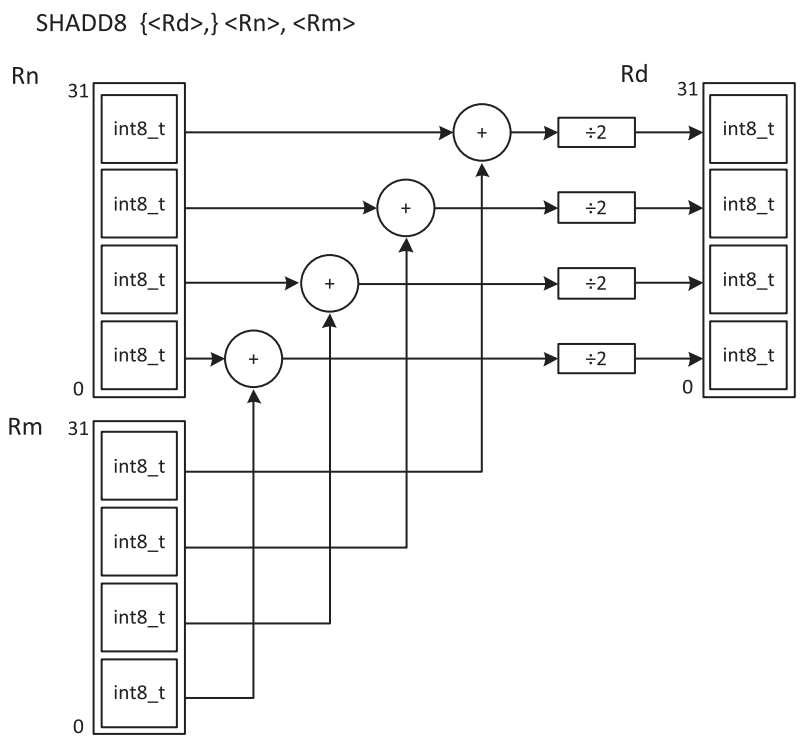

FIGURE B.15

SHADD8

SHADD16 {<Rd>,} <Rn>, <Rm>

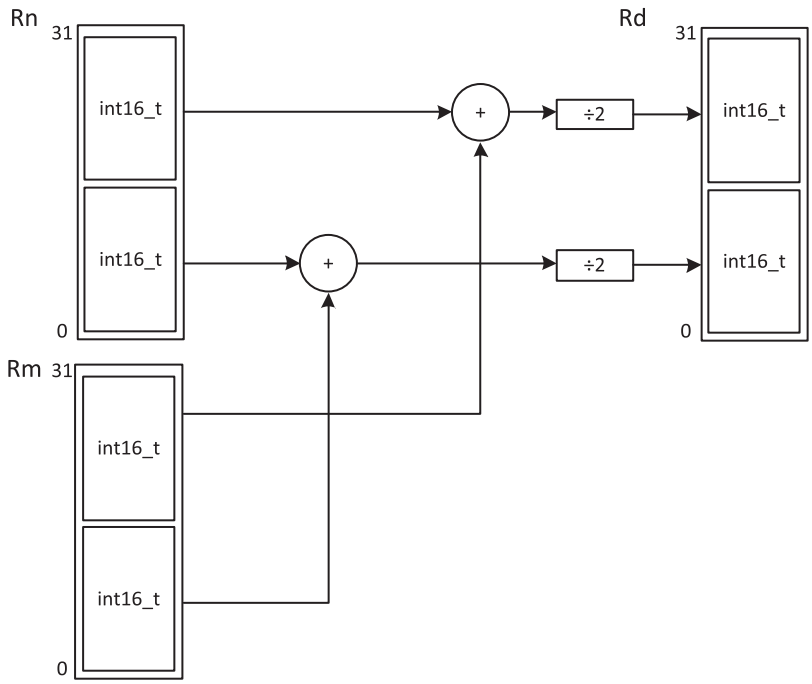

FIGURE B.16

SHADD16

SSUB8 {<Rd>,} <Rn>, <Rm>

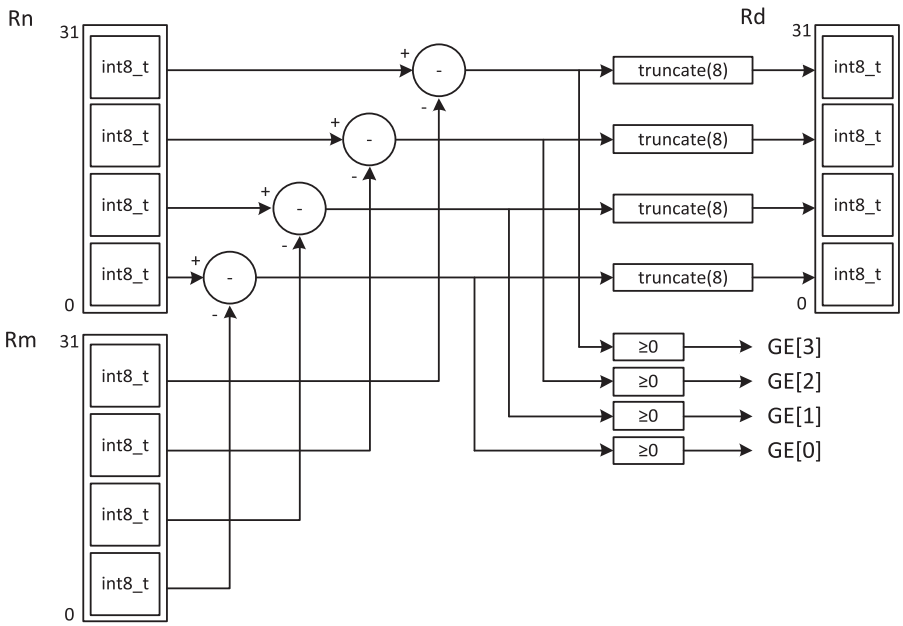

FIGURE B.17

SSUB8

SSUB16 {<Rd>,} <Rn>, <Rm>

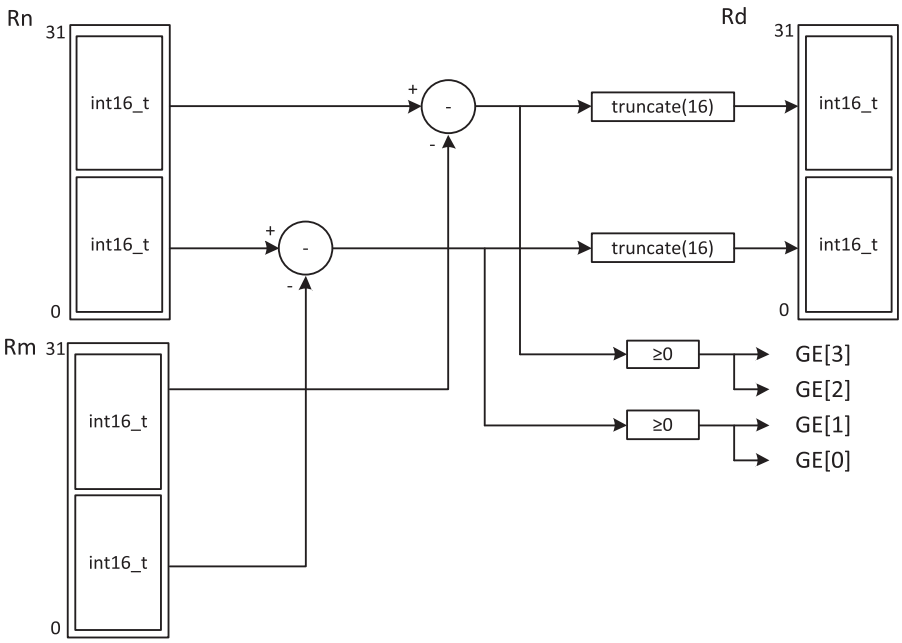

FIGURE B.18

SSUB16

SHSUB8 {<Rd>,} <Rn>, <Rm>

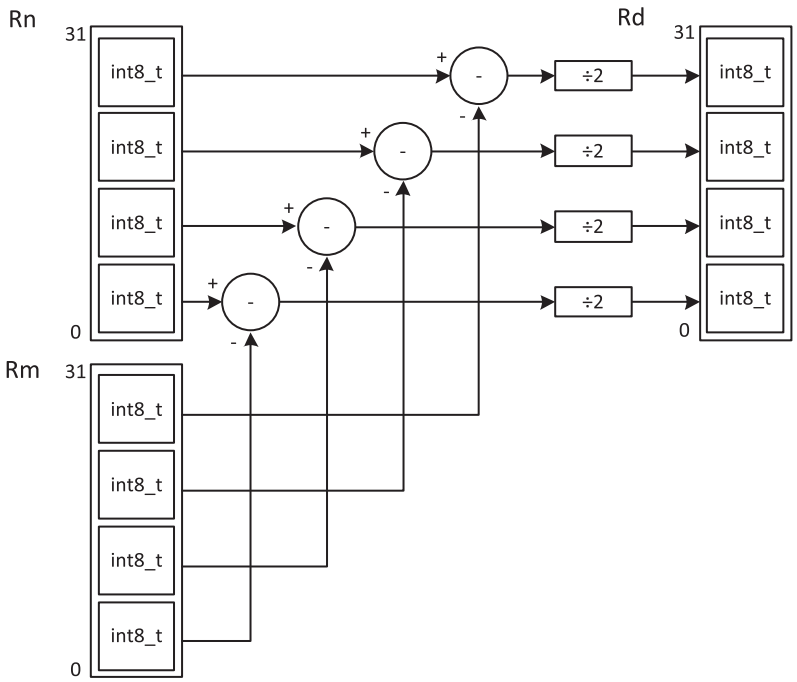

FIGURE B.19

SHSUB8

SHSUB16 {<Rd>,} <Rn>, <Rm>

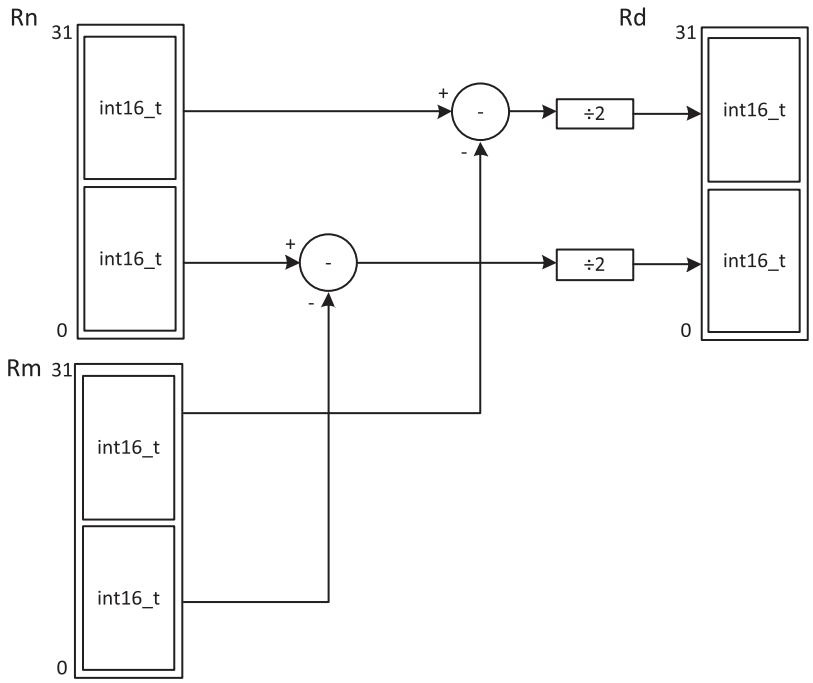

FIGURE B.20

SHSUB16

SASX {<Rd>,} <Rn>, <Rm>

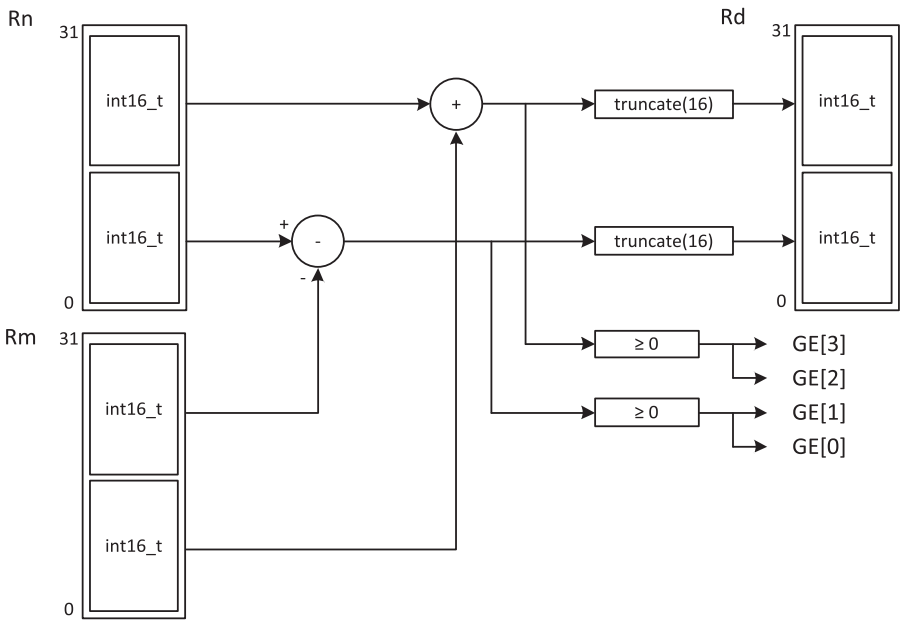

FIGURE B.21

SASX

SSAX {<Rd>,} <Rn>, <Rm>

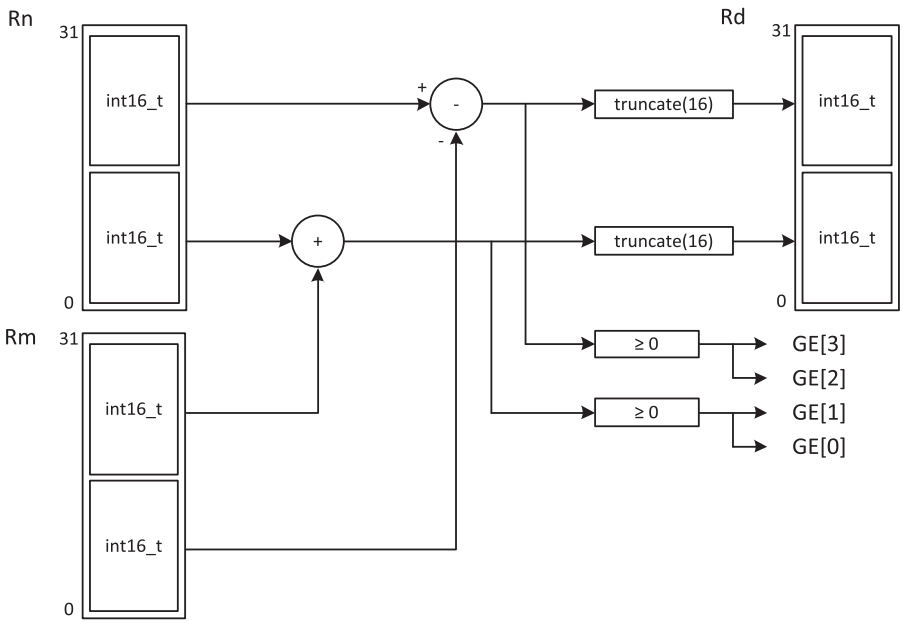

FIGURE B.22

SSAX

SHASX {<Rd>,} <Rn>, <Rm>

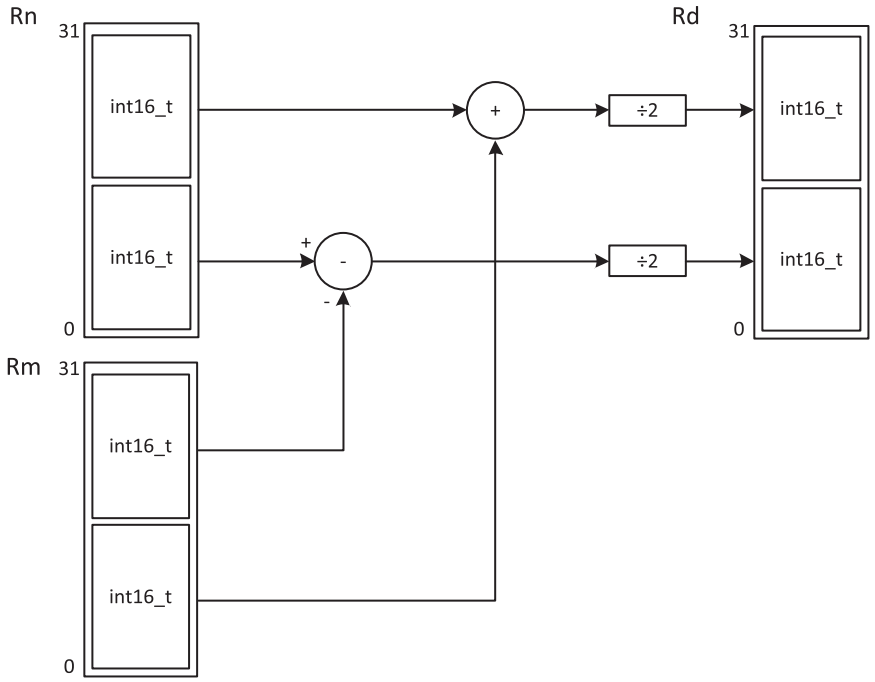

FIGURE B.23

SHASX

SHSAX {<Rd>,} <Rn>, <Rm>

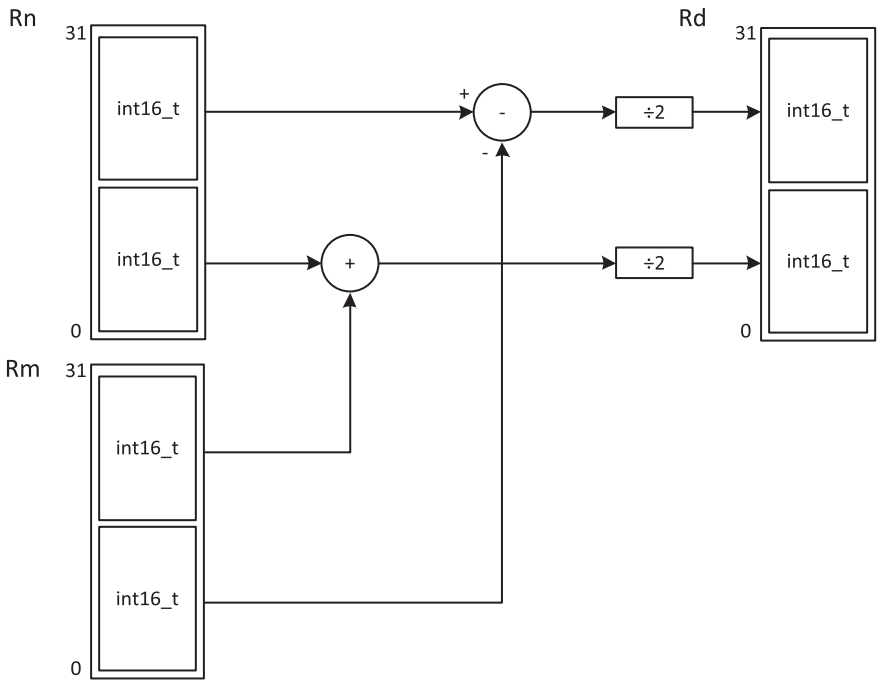

FIGURE B.24

SHSAX

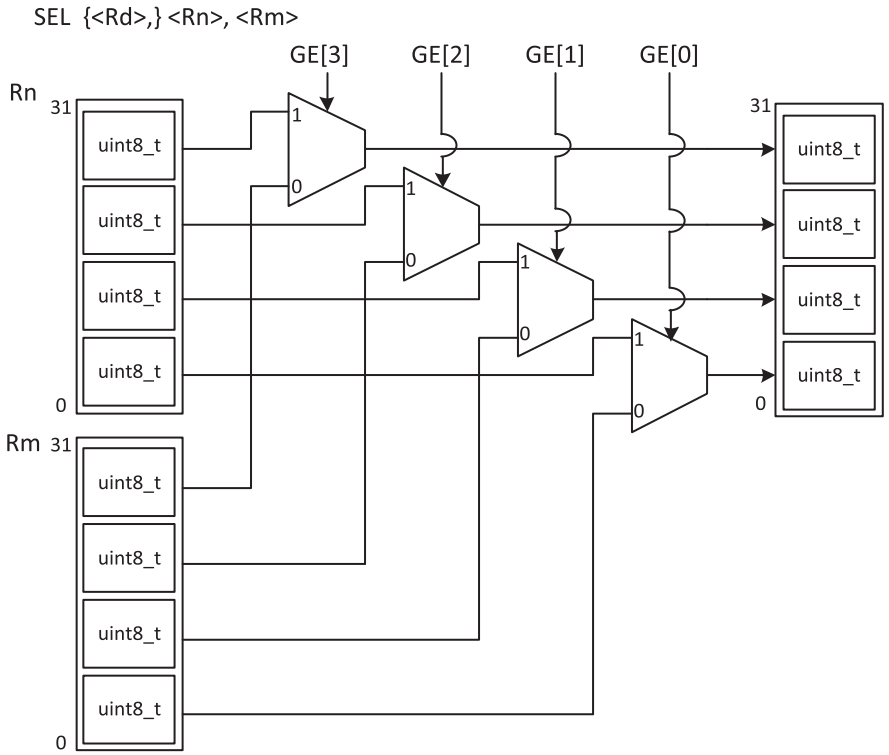

FIGURE B.25

SEL

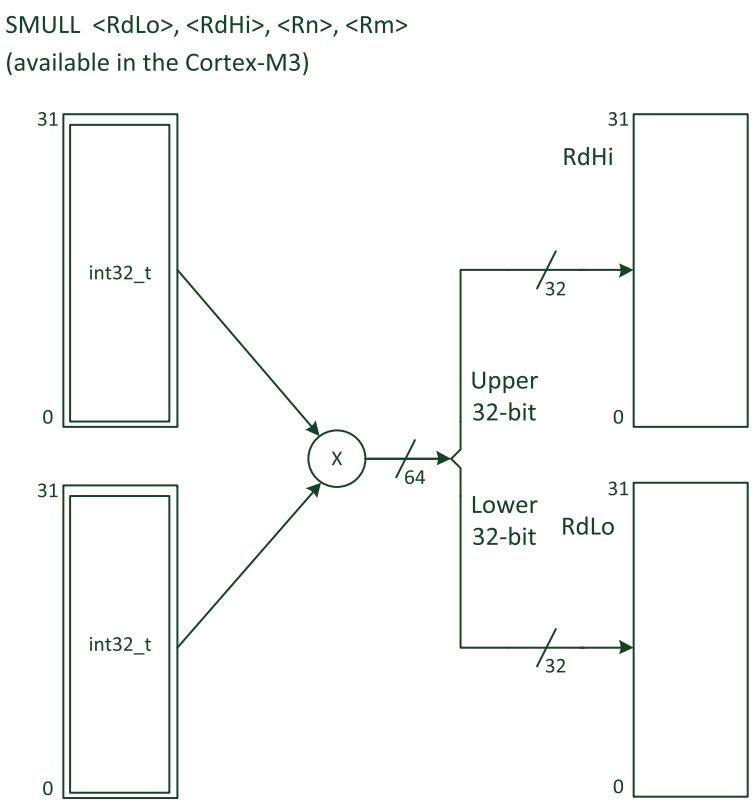

FIGURE B.26

SMULL

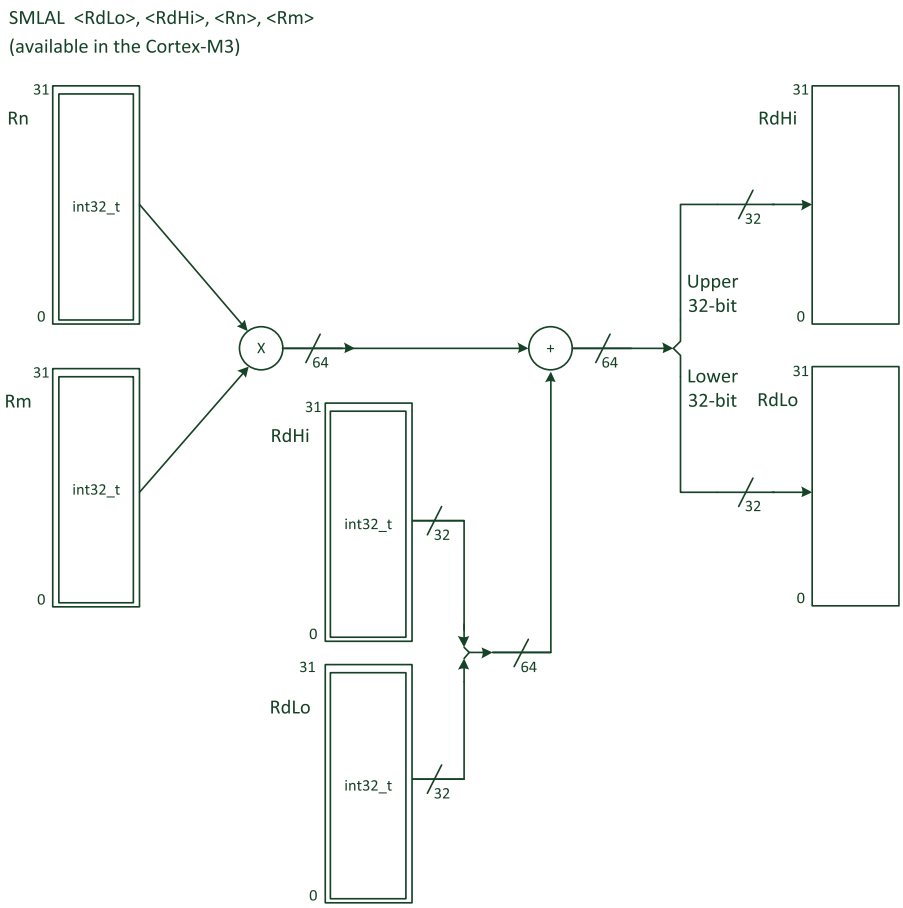

FIGURE B.27

SMLAL

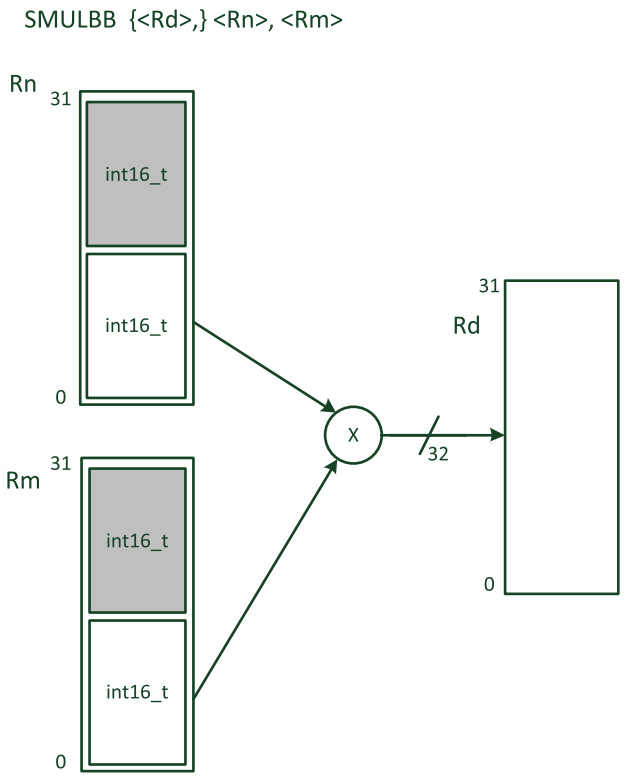

FIGURE B.28

SMULBB

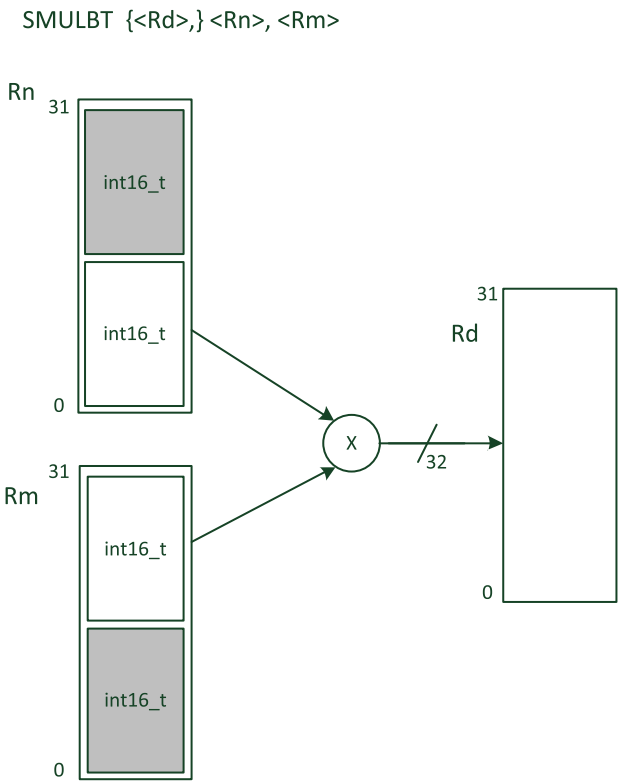

FIGURE B.29

SMULBT

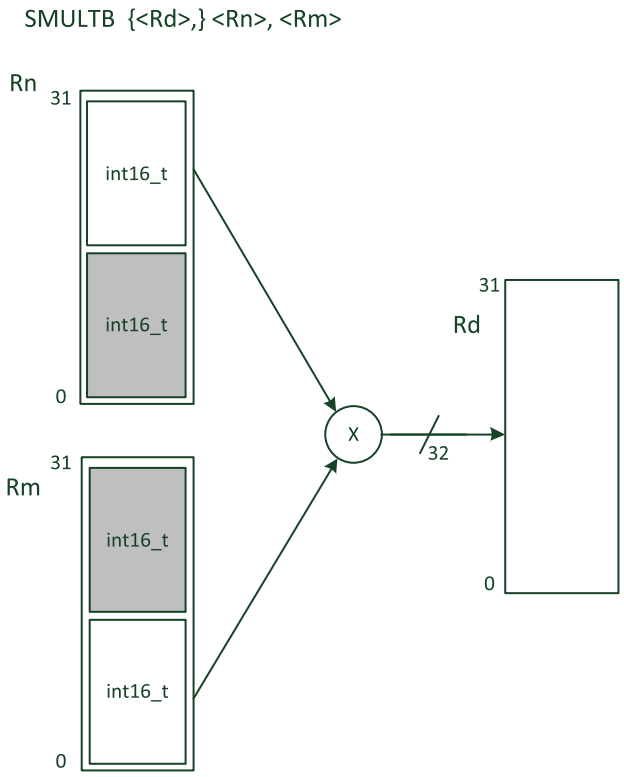

FIGURE B.30

SMULTB

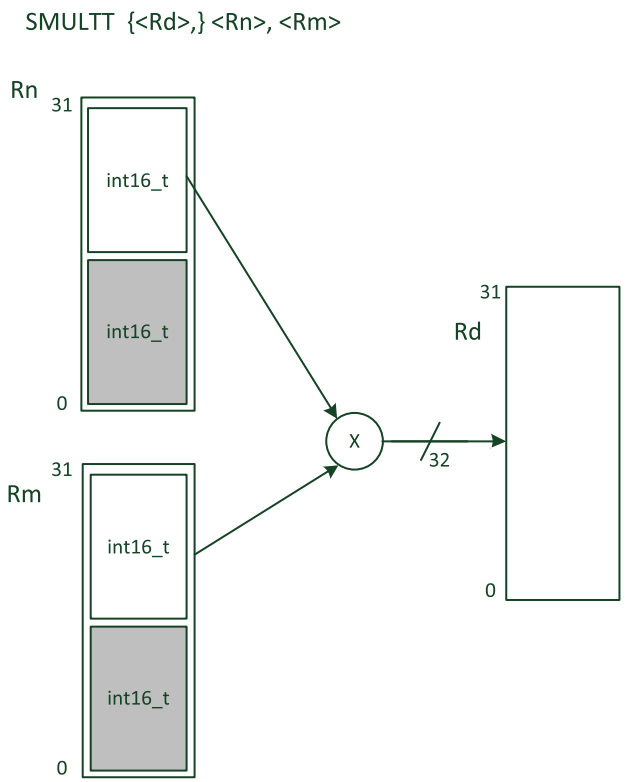

FIGURE B.31

SMULTT

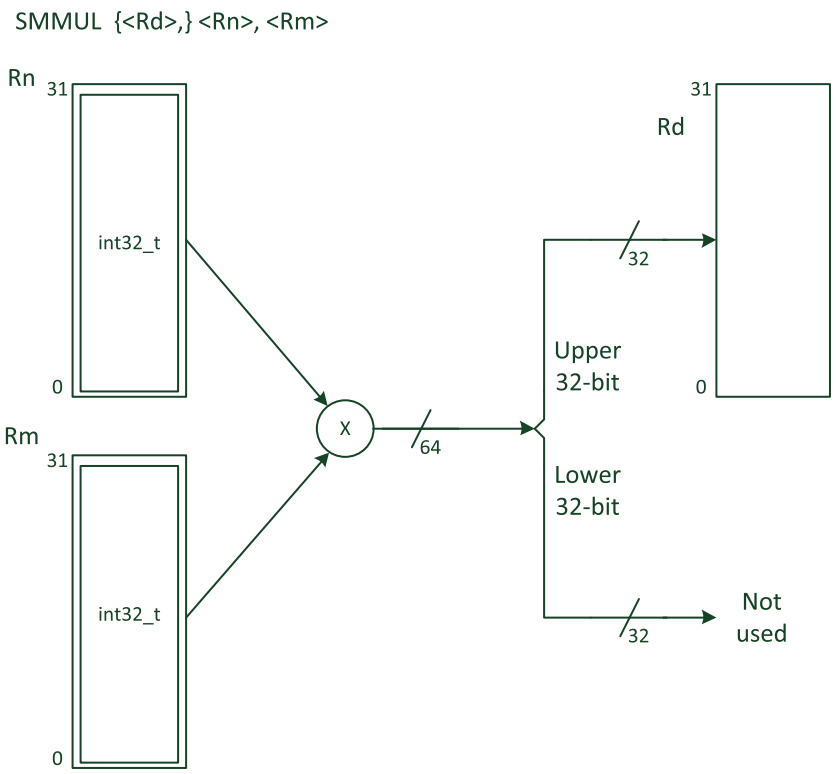

FIGURE B.32

SMMUL

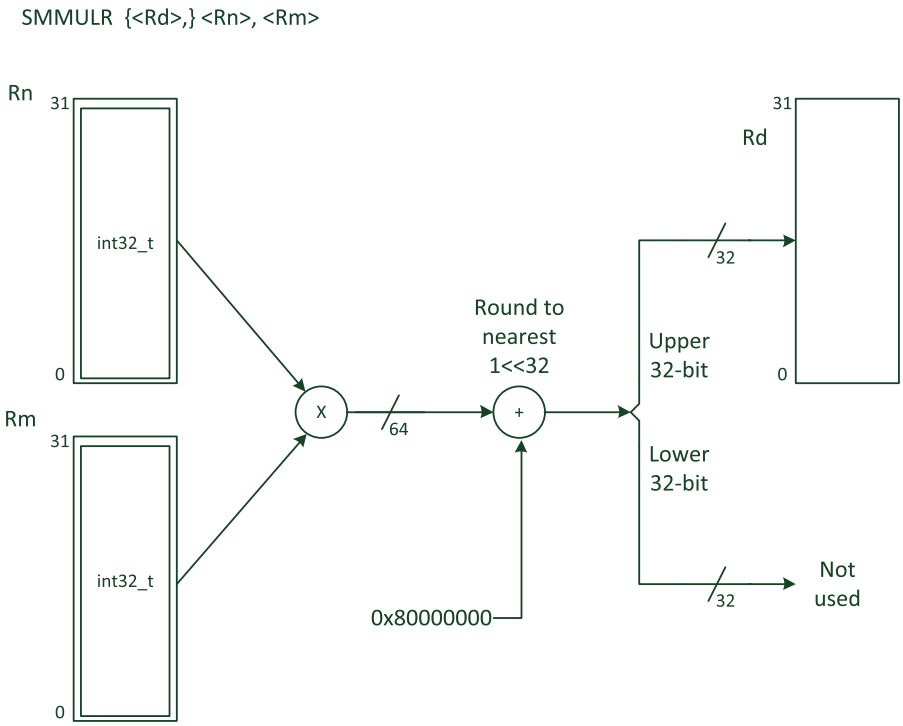

FIGURE B.33

SMMULR

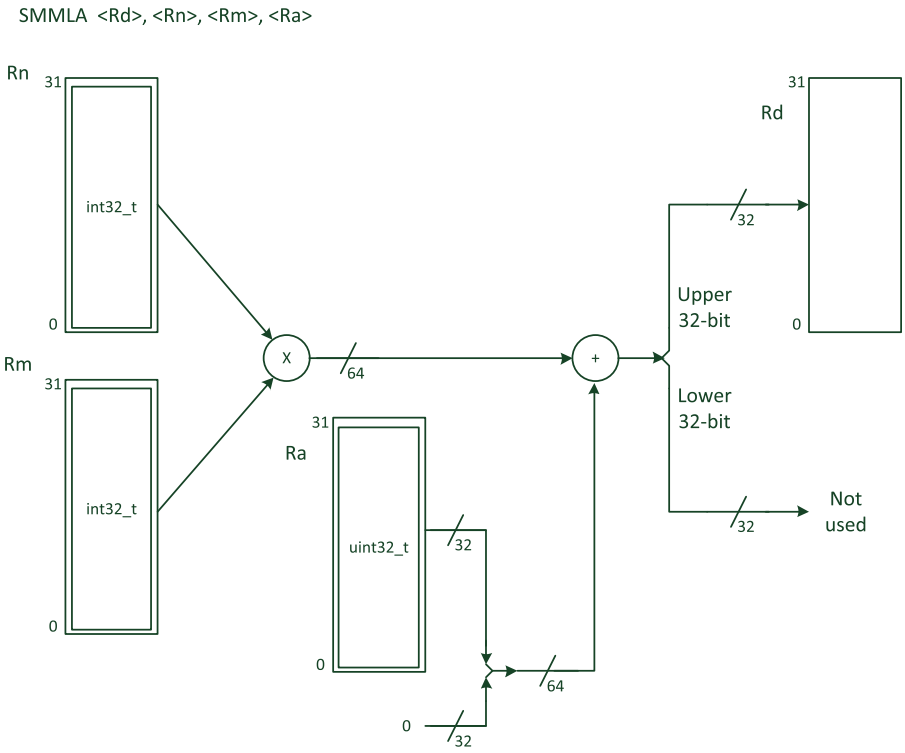

FIGURE B.34

SMMLA

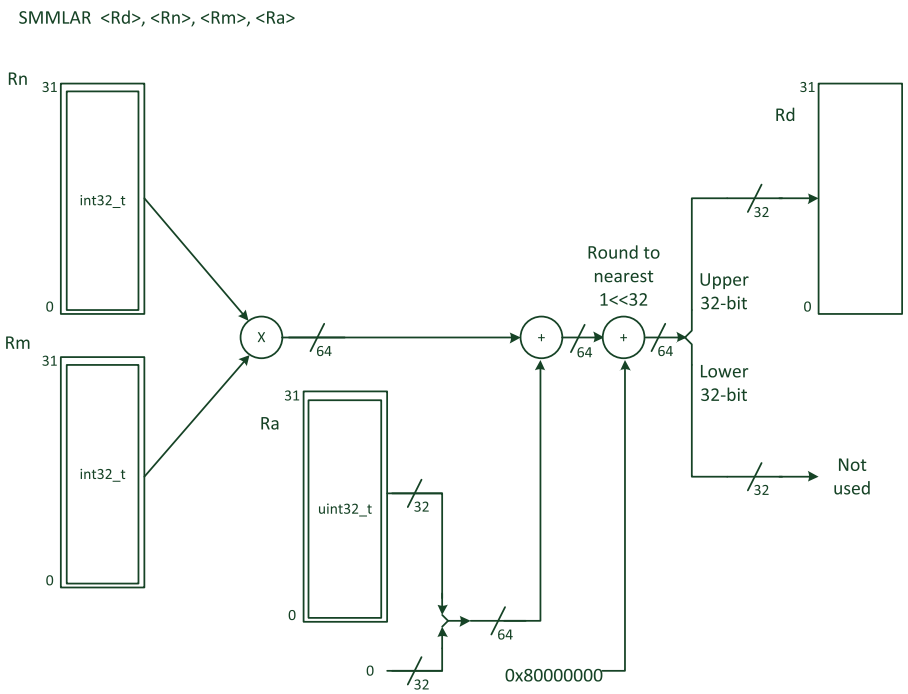

FIGURE B.35

SMMLAR

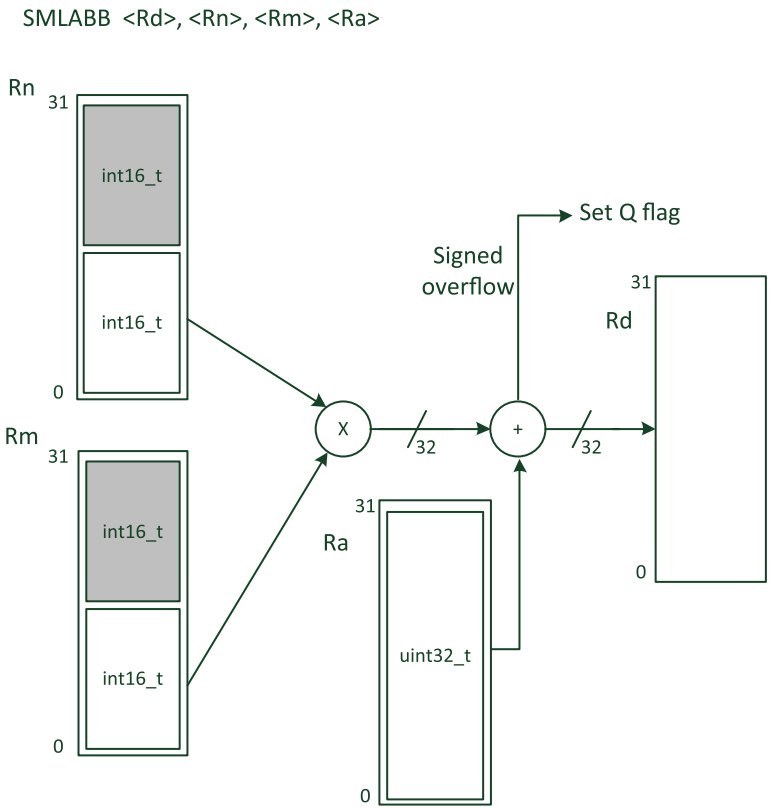

FIGURE B.36

SMLABB

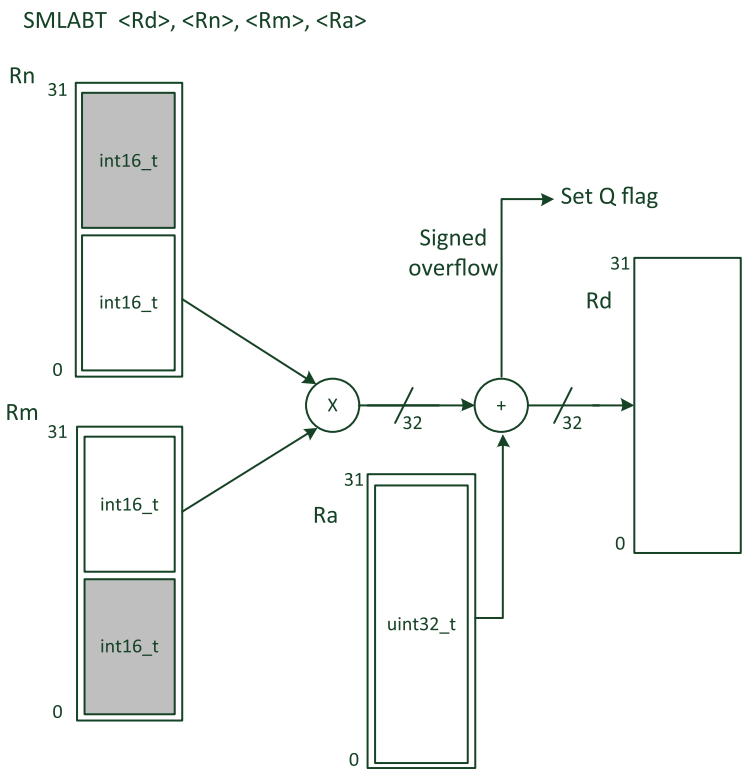

FIGURE B.37

SMLABT

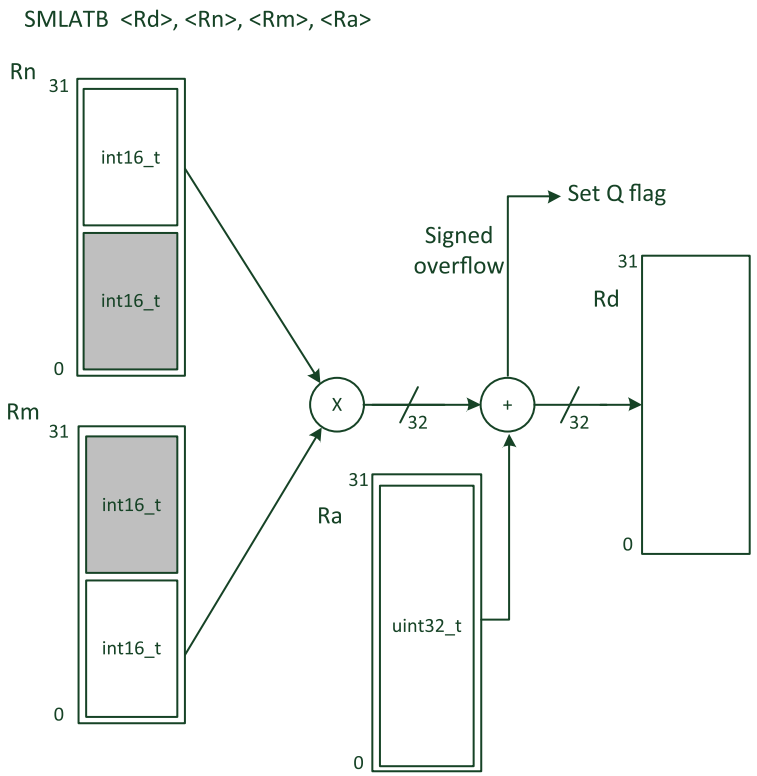

FIGURE B.38

SMLATB

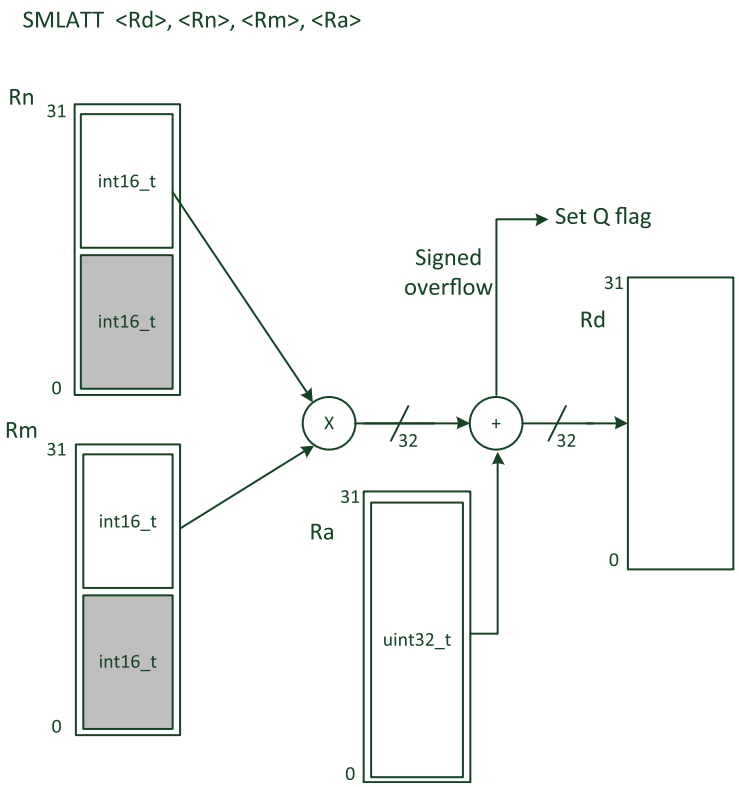

FIGURE B.39

SMLATT

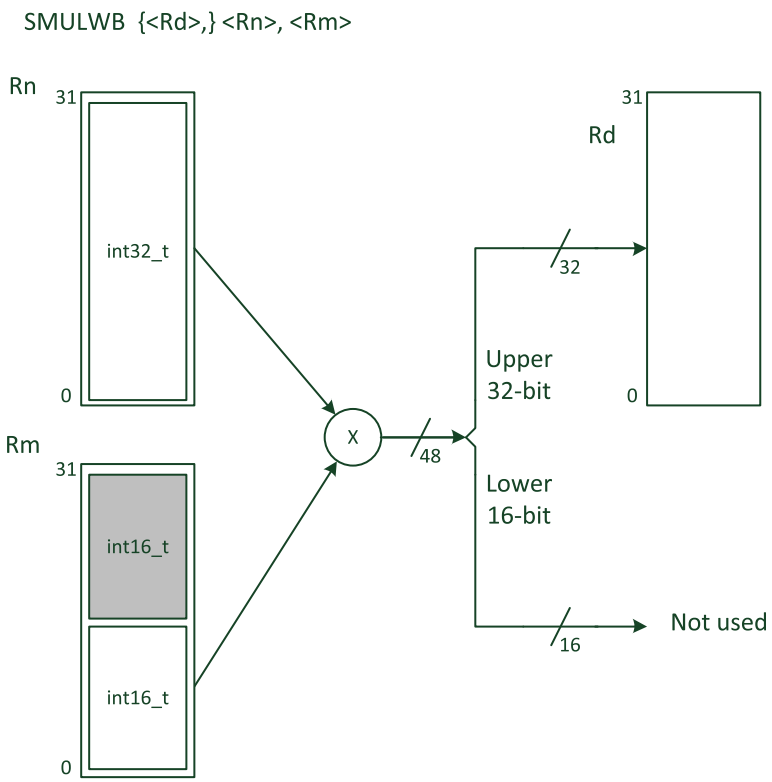

FIGURE B.40

SMULWB

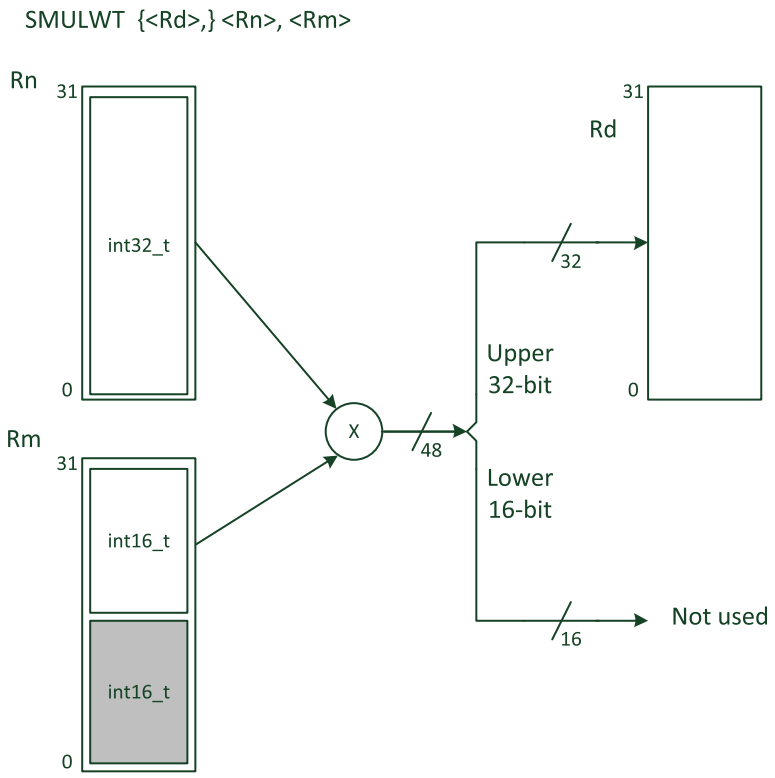

FIGURE B.41

SMULWT

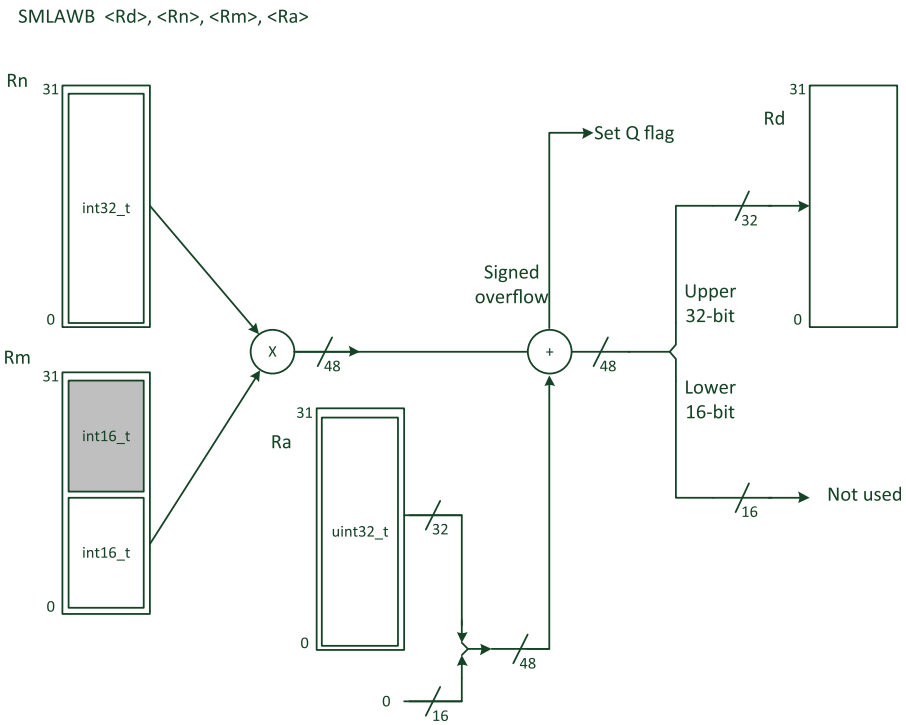

FIGURE B.42

SMLAWB

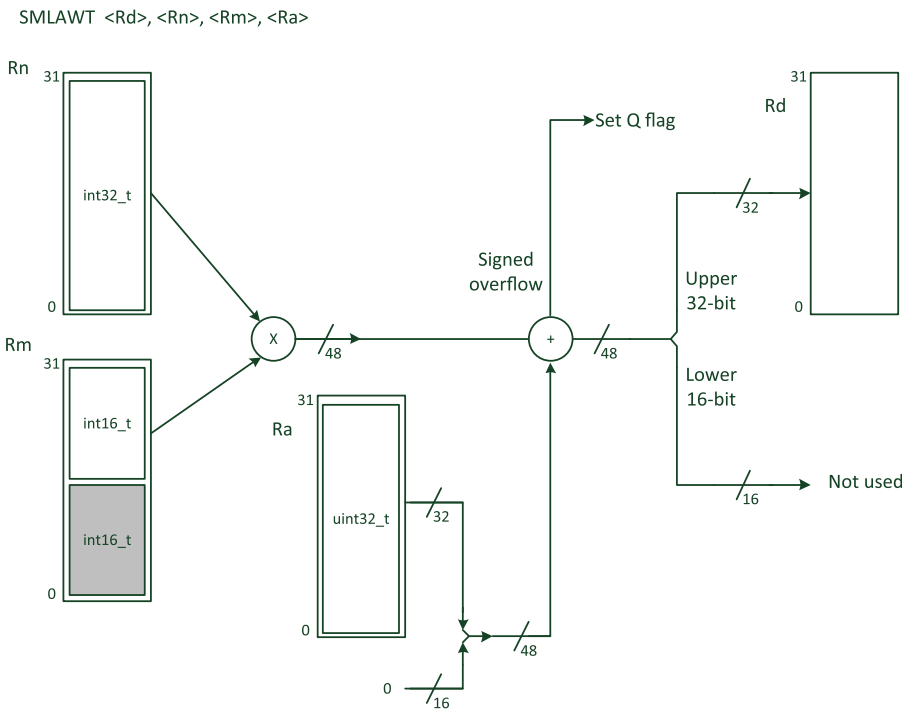

FIGURE B.43

SMLAWT

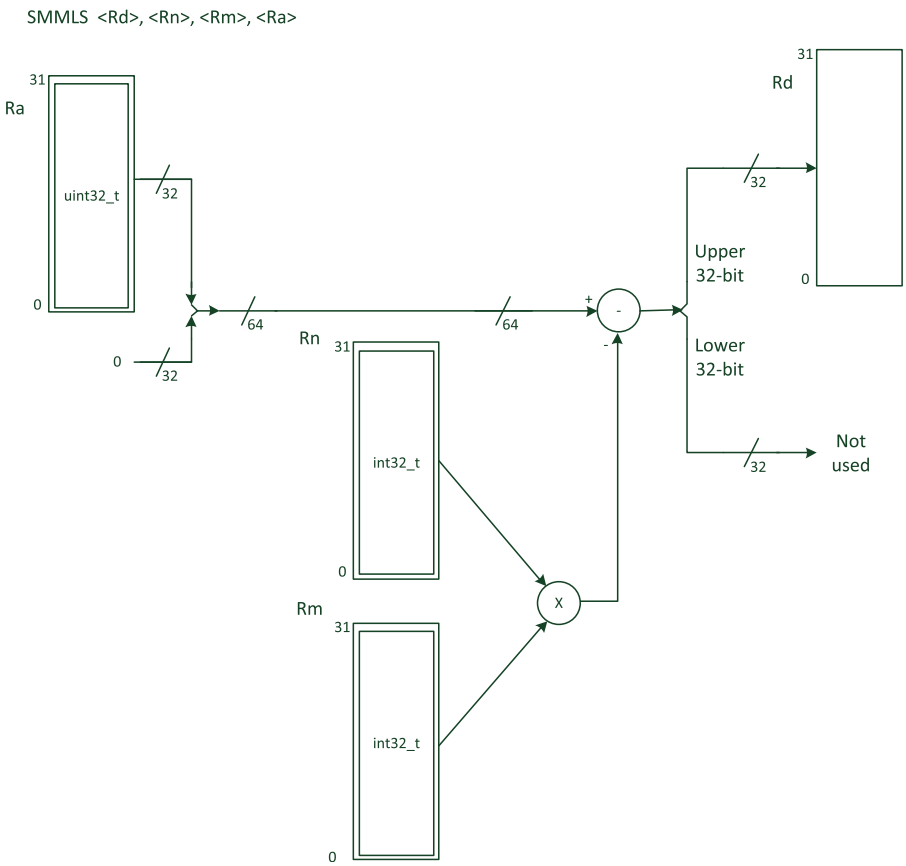

FIGURE B.44

SMMLS

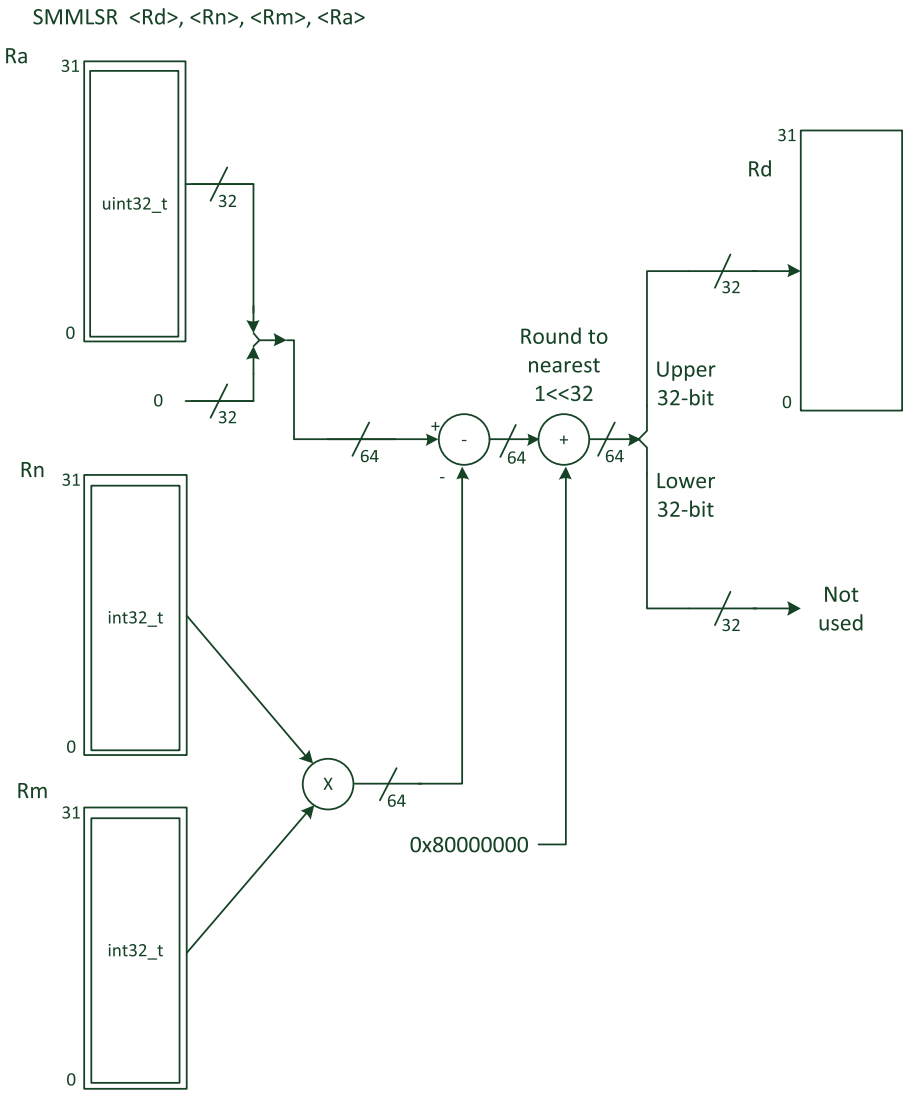

FIGURE B.45

SMMLSR

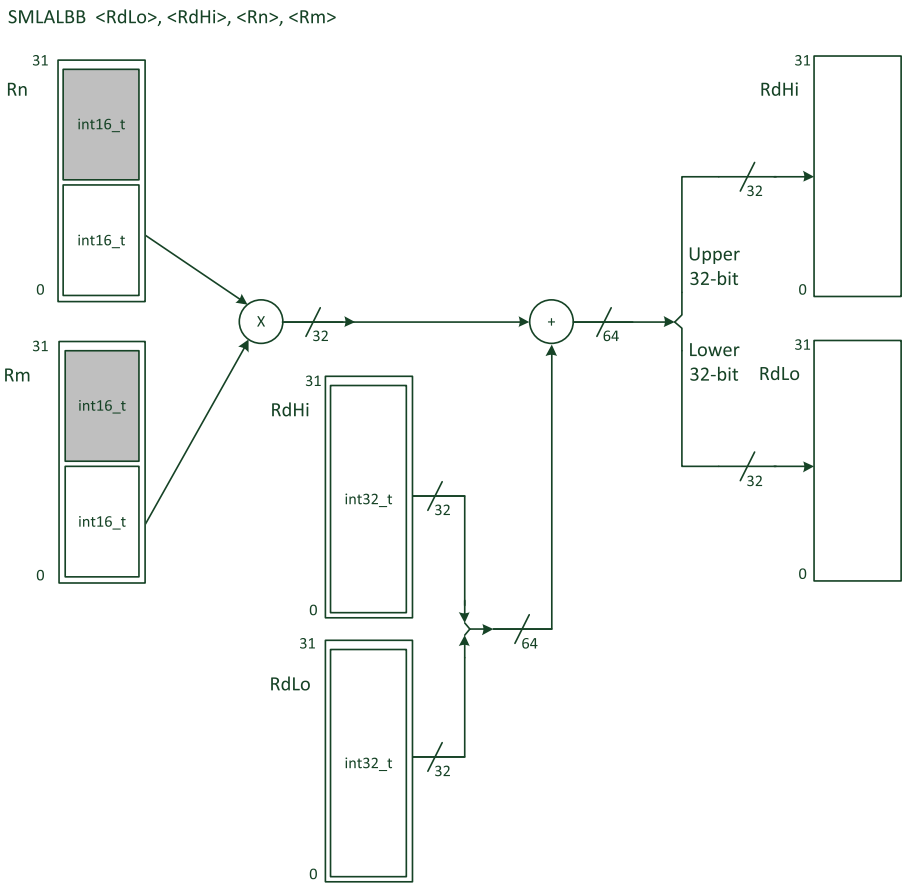

FIGURE B.46

SMLALBB

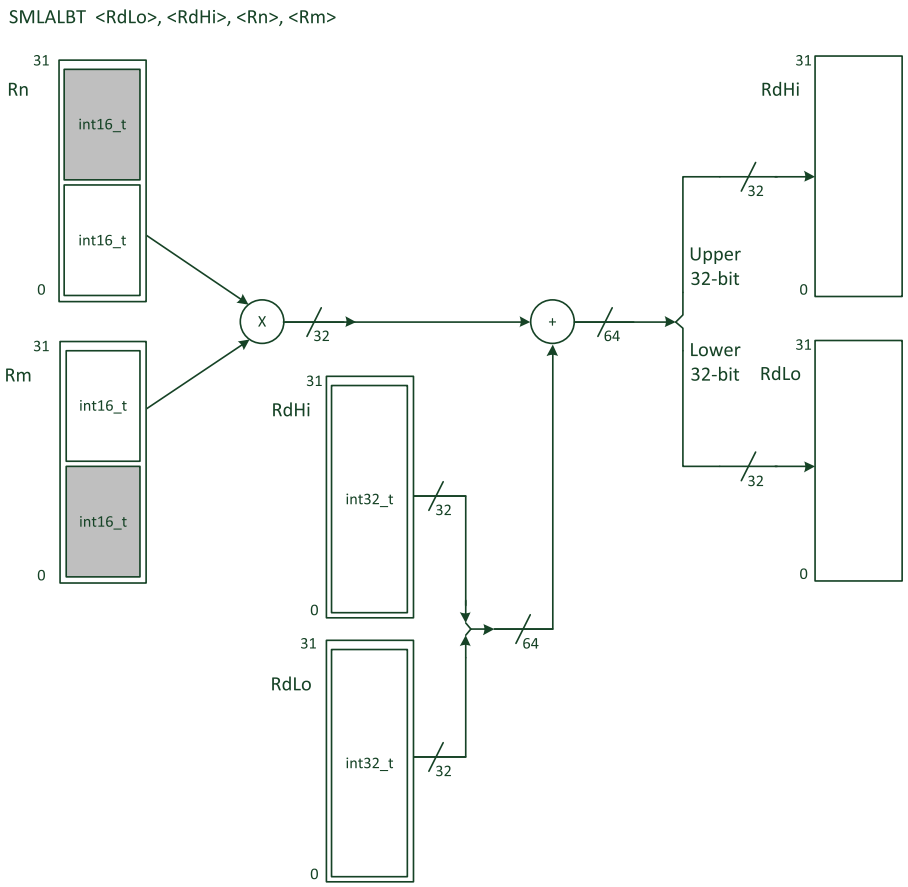

FIGURE B.47

SMLALBT

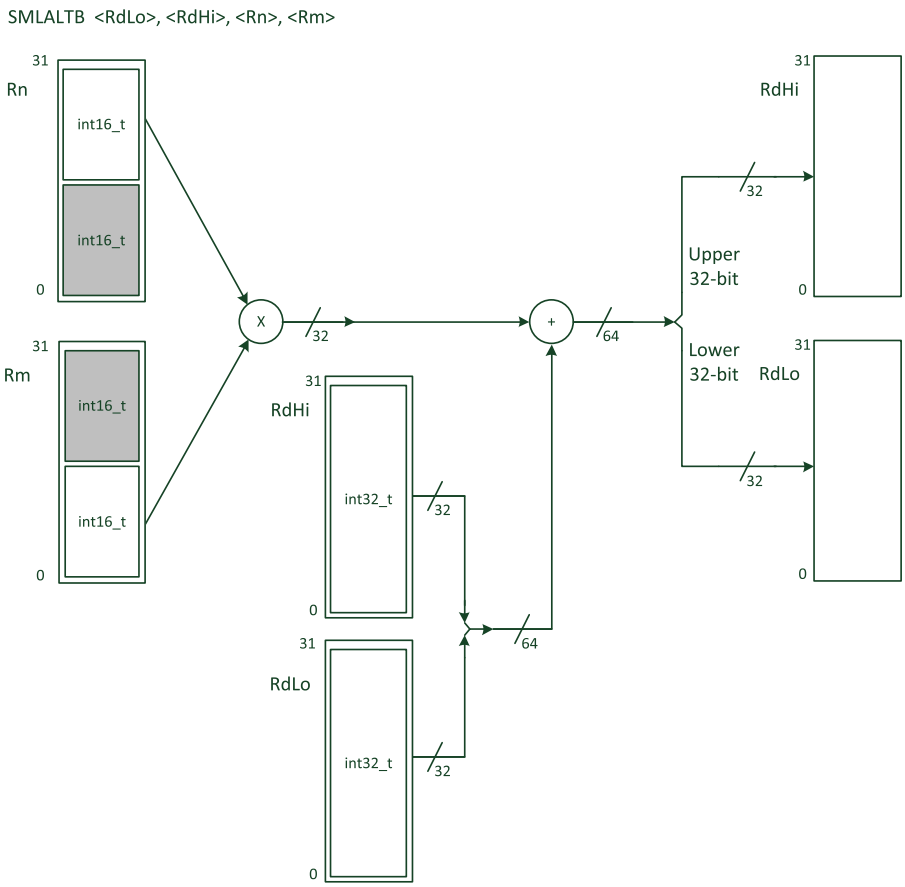

FIGURE B.48

SMLALTB

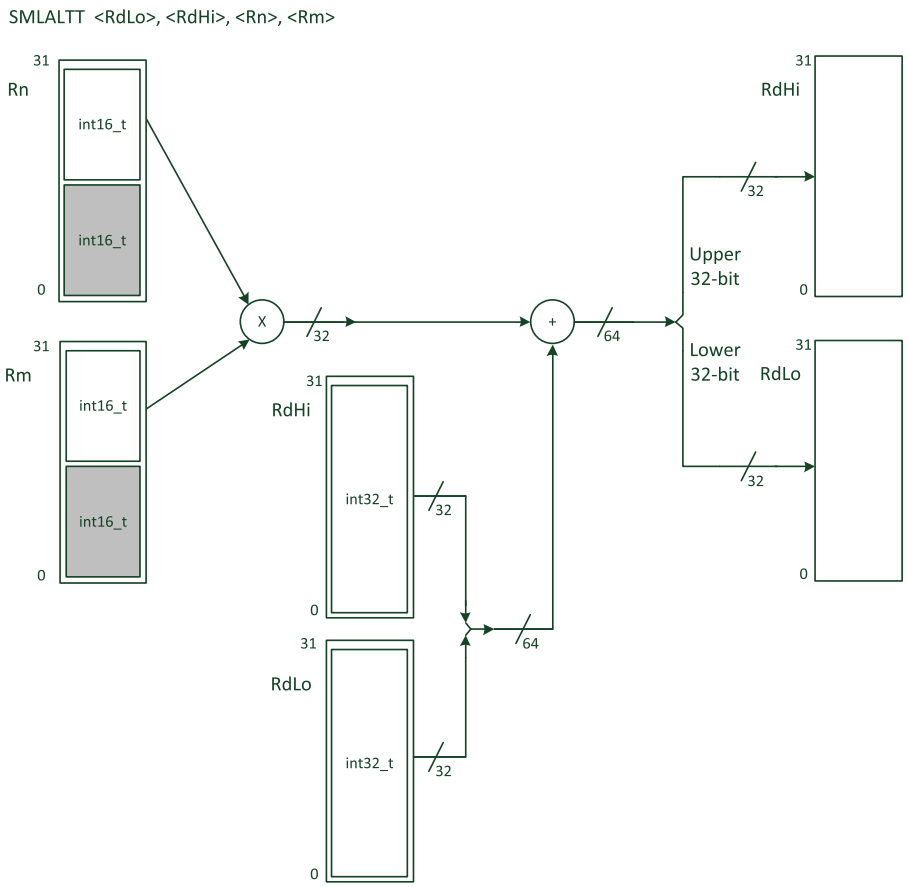

FIGURE B.49

SMLALTT

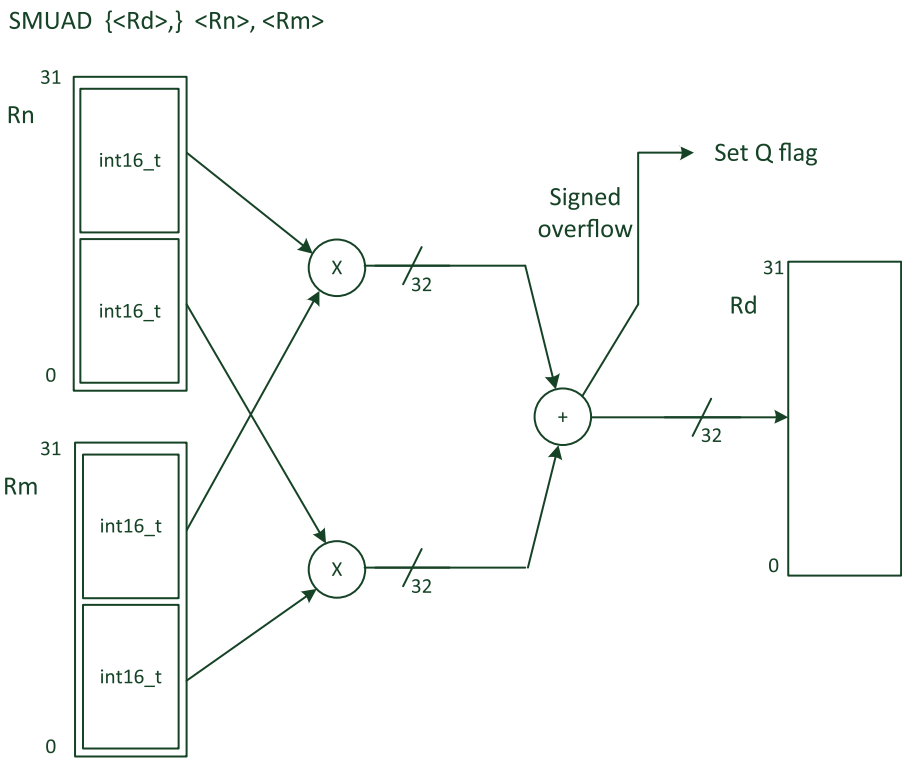

FIGURE B.50

SMUAD

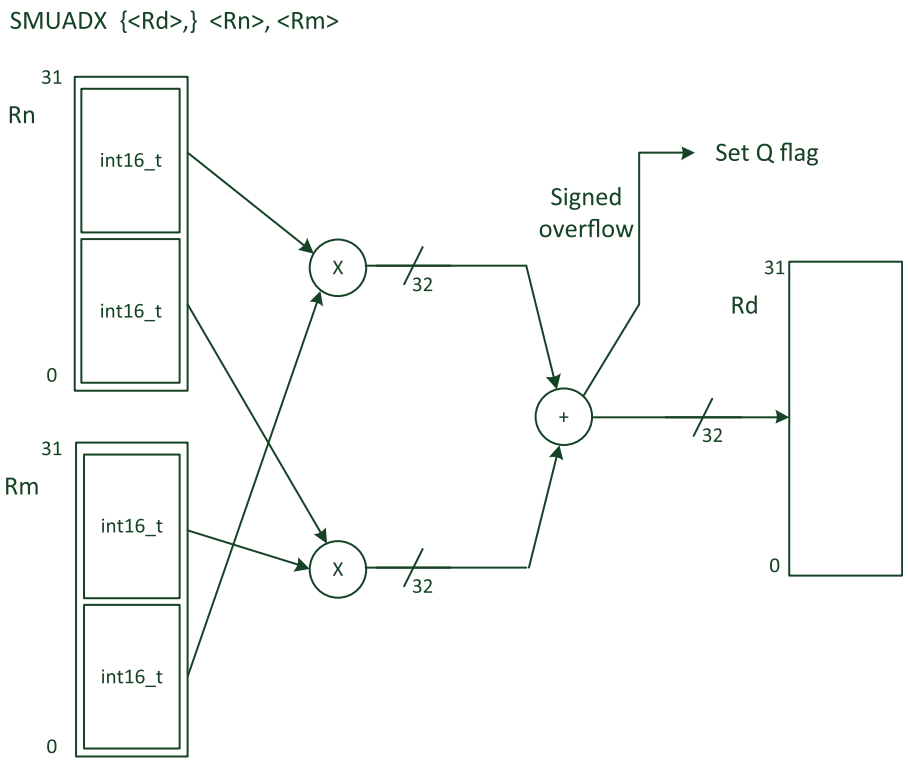

FIGURE B.51

SMUADX

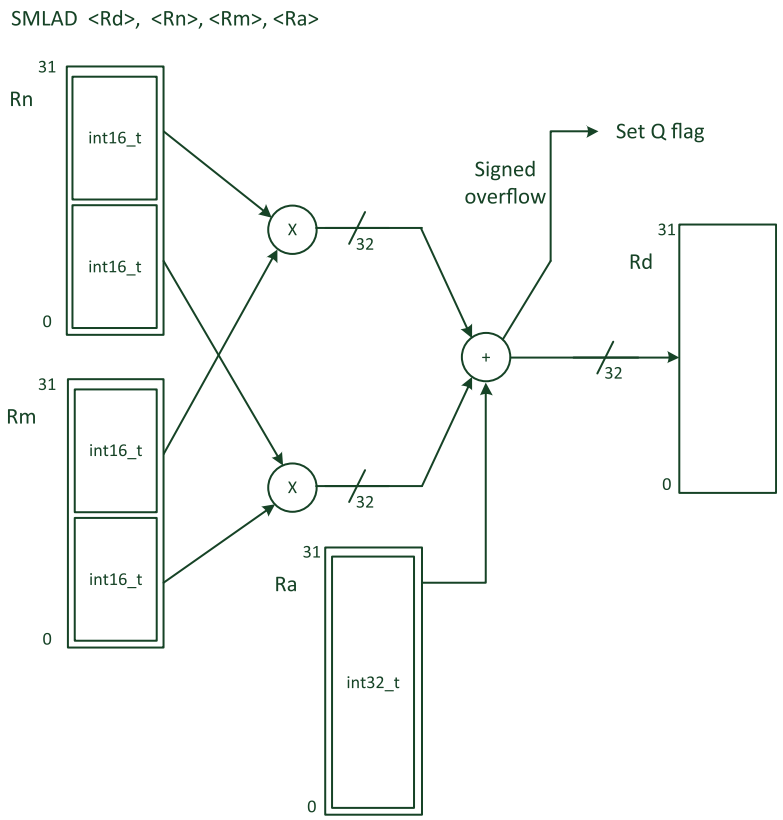

FIGURE B.52

SMLAD

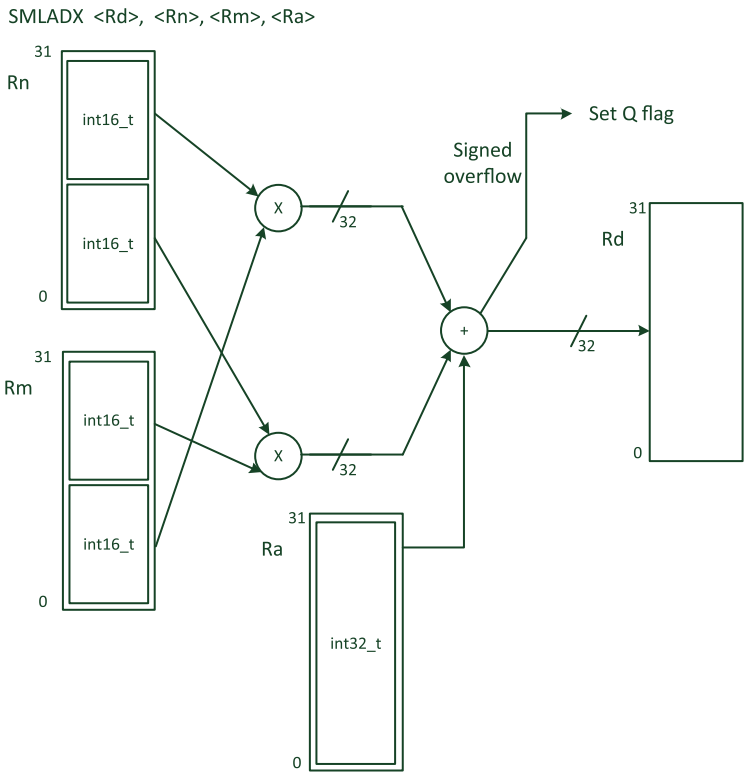

FIGURE B.53

SMLADX

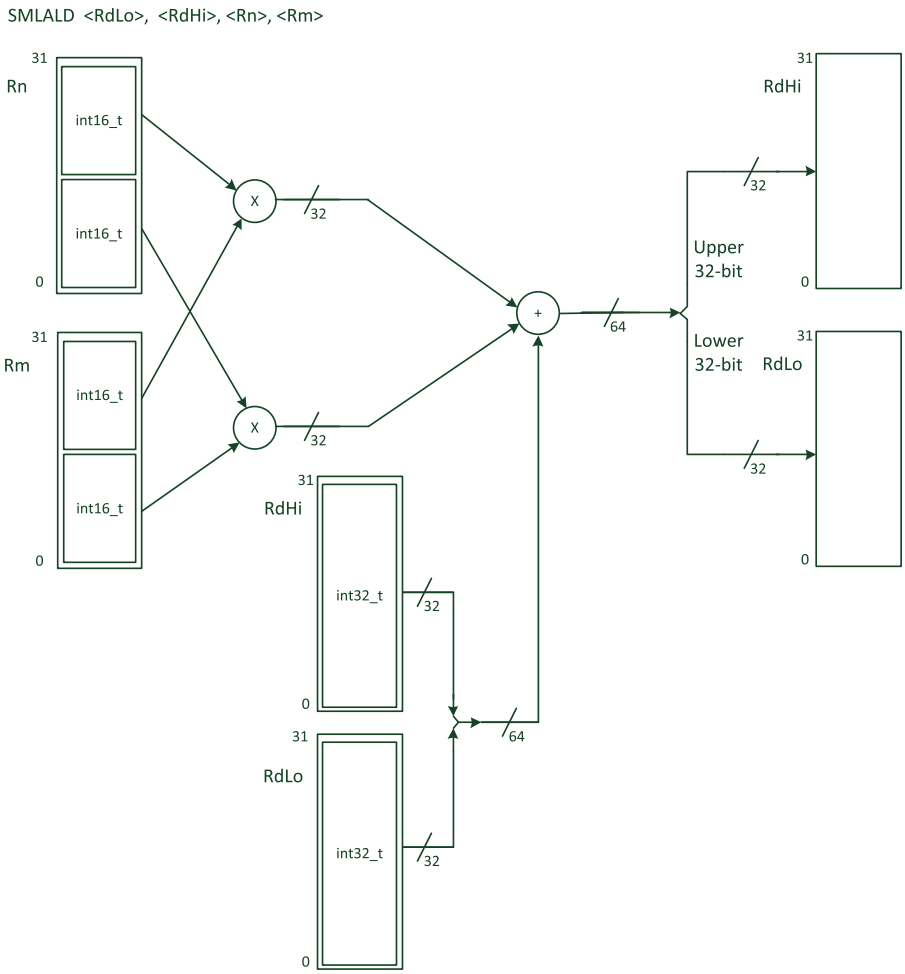

FIGURE B.54

SMLALD

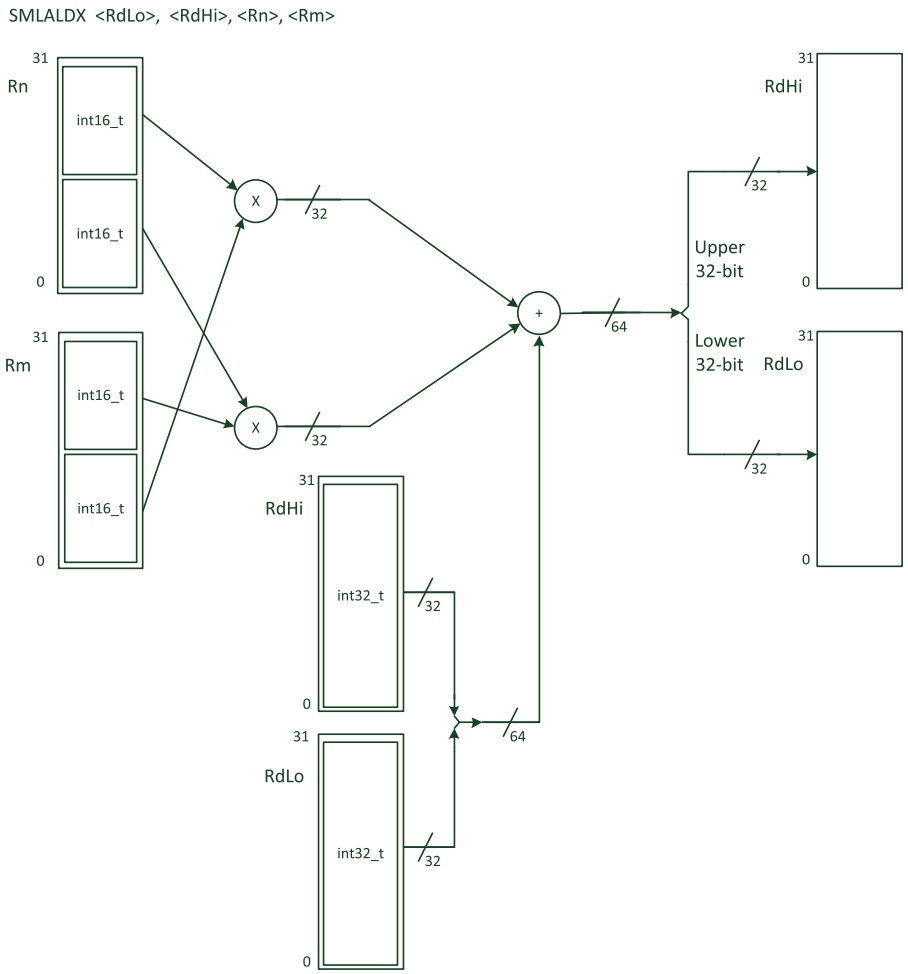

FIGURE B.55

SMLALX

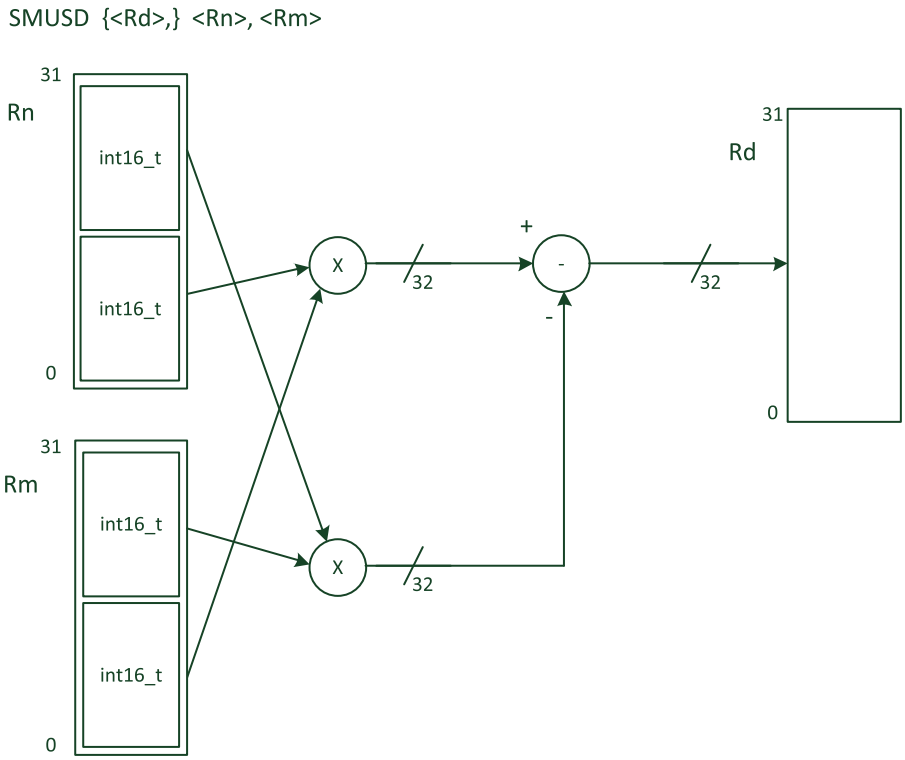

FIGURE B.56

SMUSD

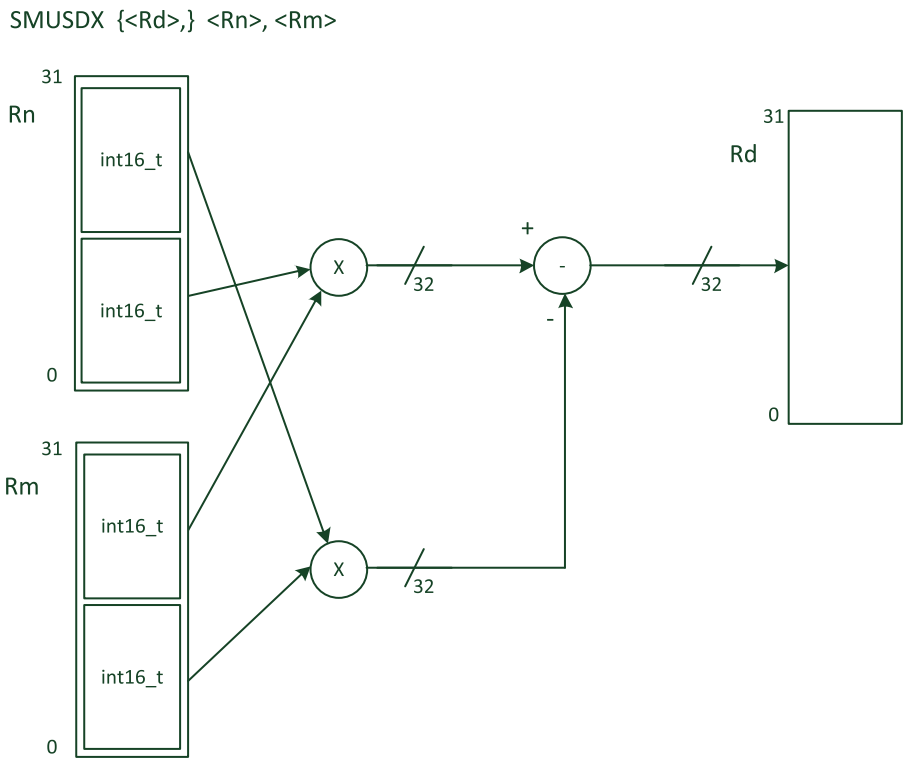

FIGURE B.57

SMUSDX

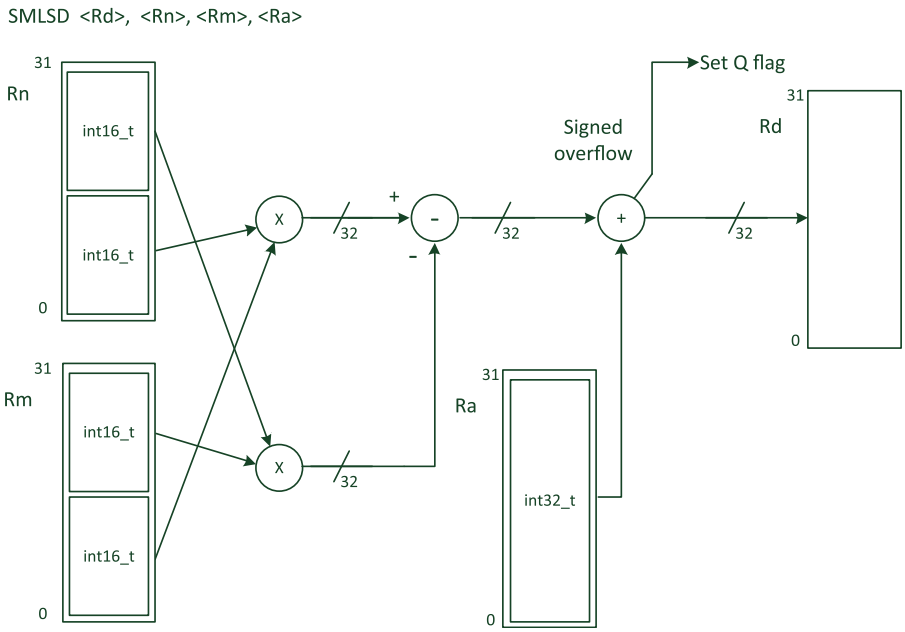

FIGURE B.58

SMLSD

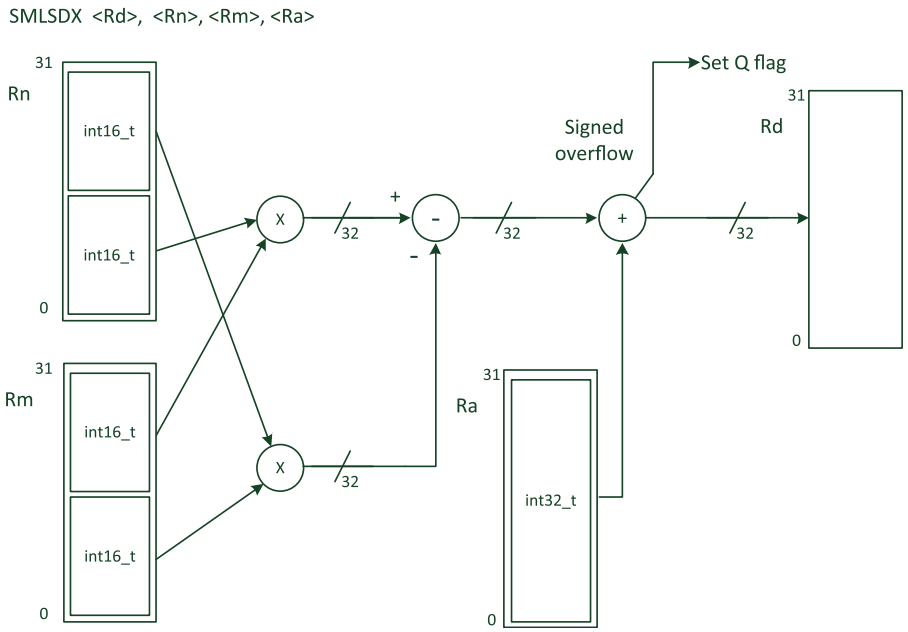

FIGURE B.59

SMLSDX

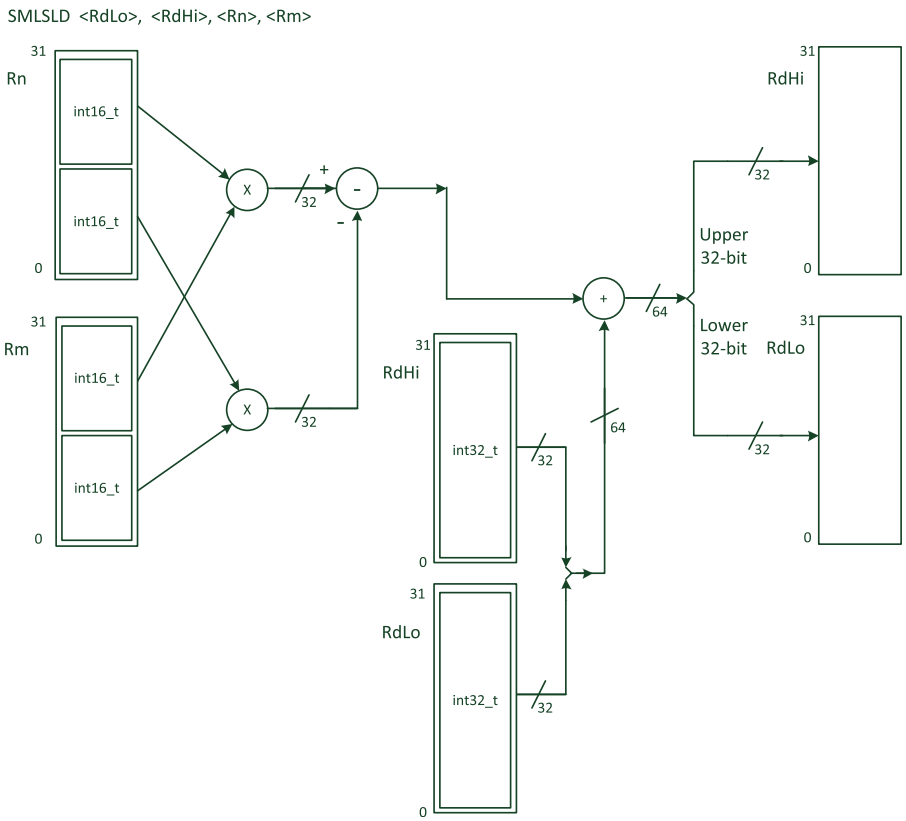

FIGURE B.60

SMLSLD

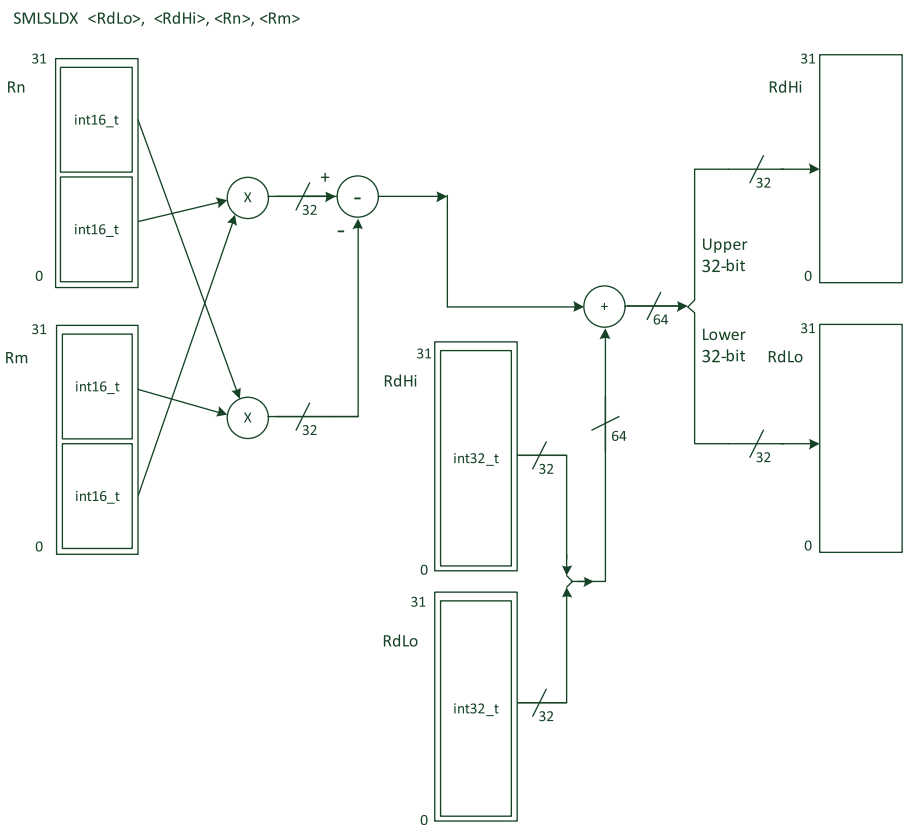

FIGURE B.61

SMLSLDX

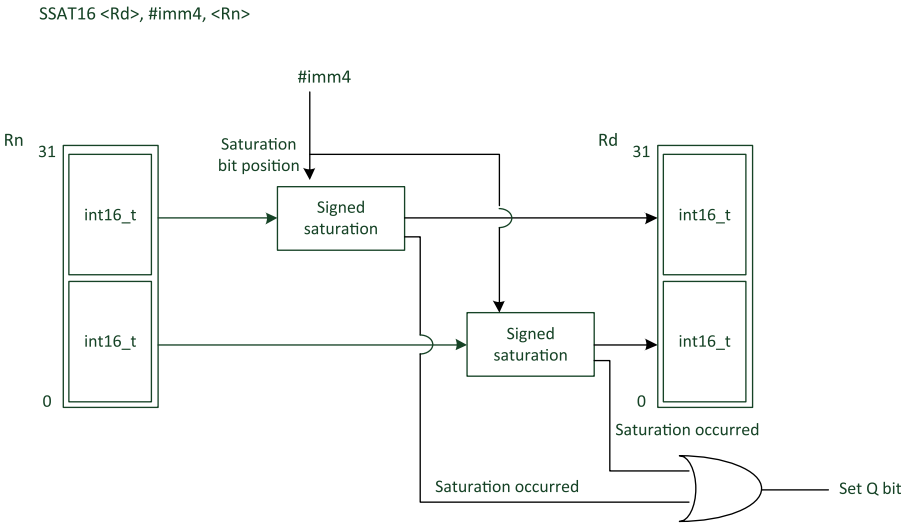

FIGURE B.62

SSAT16

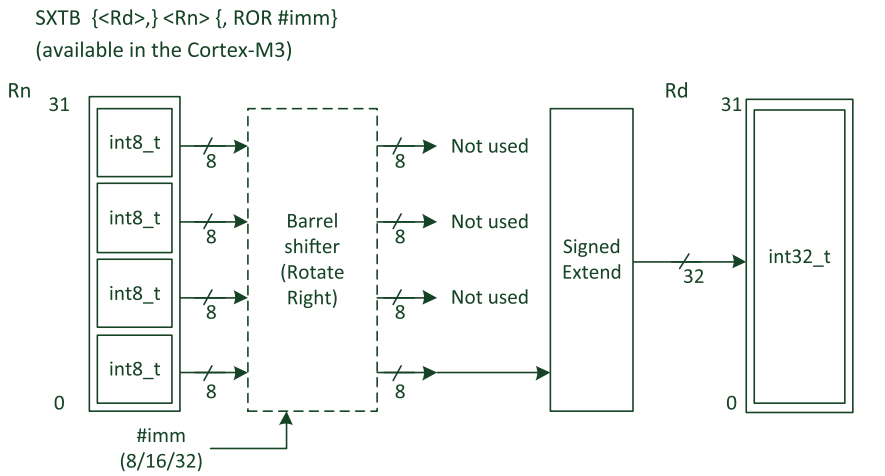

FIGURE B.63

SXTB

SXTB16 {<Rd>,} <Rn> {, ROR #imm}

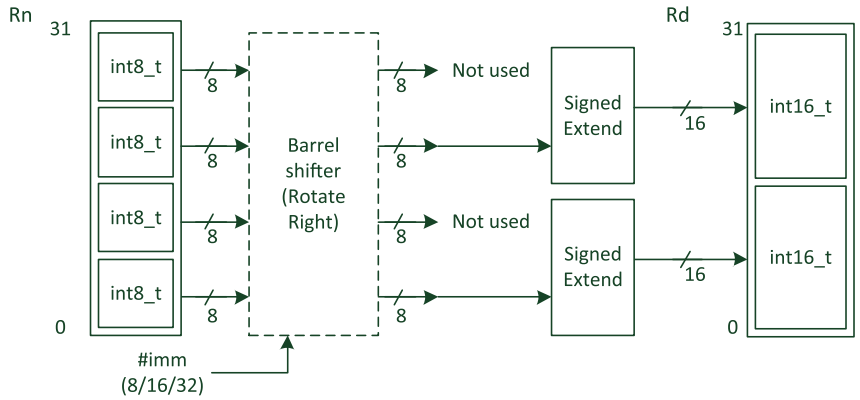

FIGURE B.64

SXTB16

SXTAB {<Rd>,} <Rn>, <Rm> {, ROR #imm}

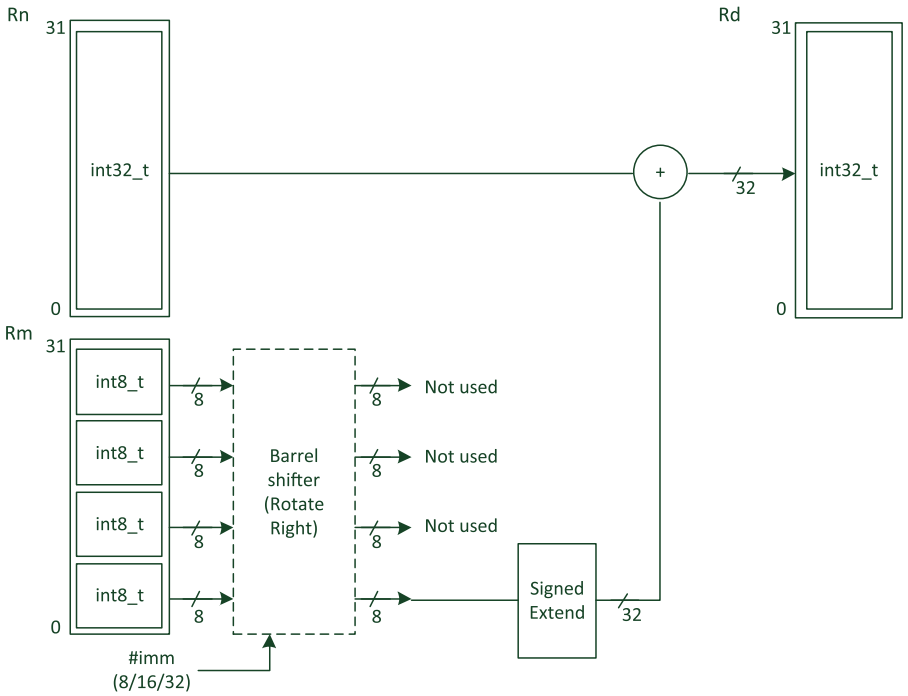

FIGURE B.65

SXTAB

SXTAB16 {<Rd>,} <Rn>, <Rm> {, ROR #imm}

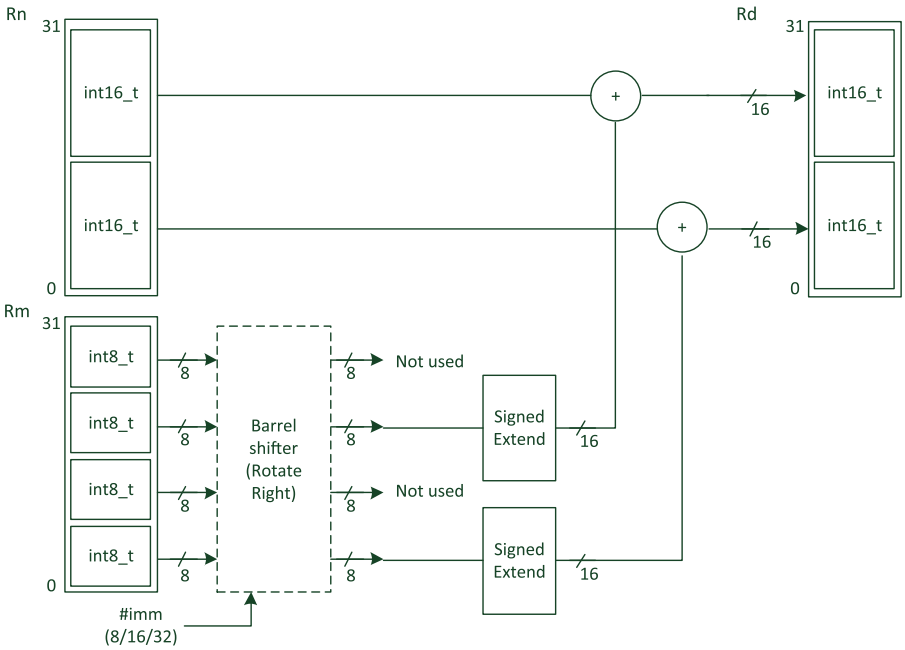

FIGURE B.66

SXTAB16

SXTH {<Rd>,} <Rn>, <Rm> {, ROR #imm}
(available in the Cortex-M3)

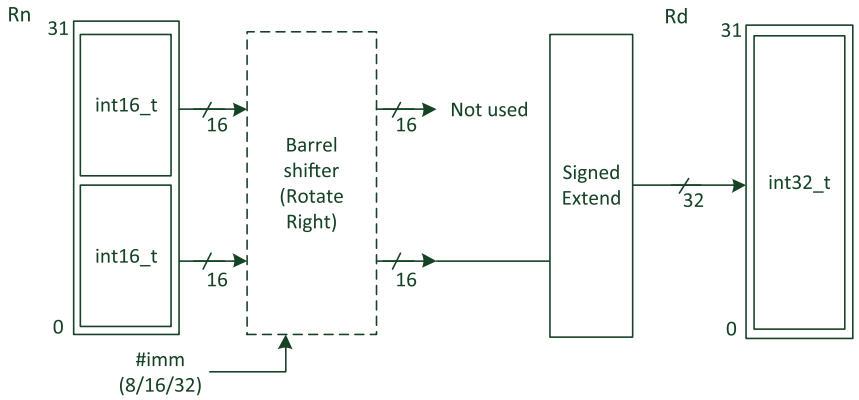

FIGURE B.67

SXTH

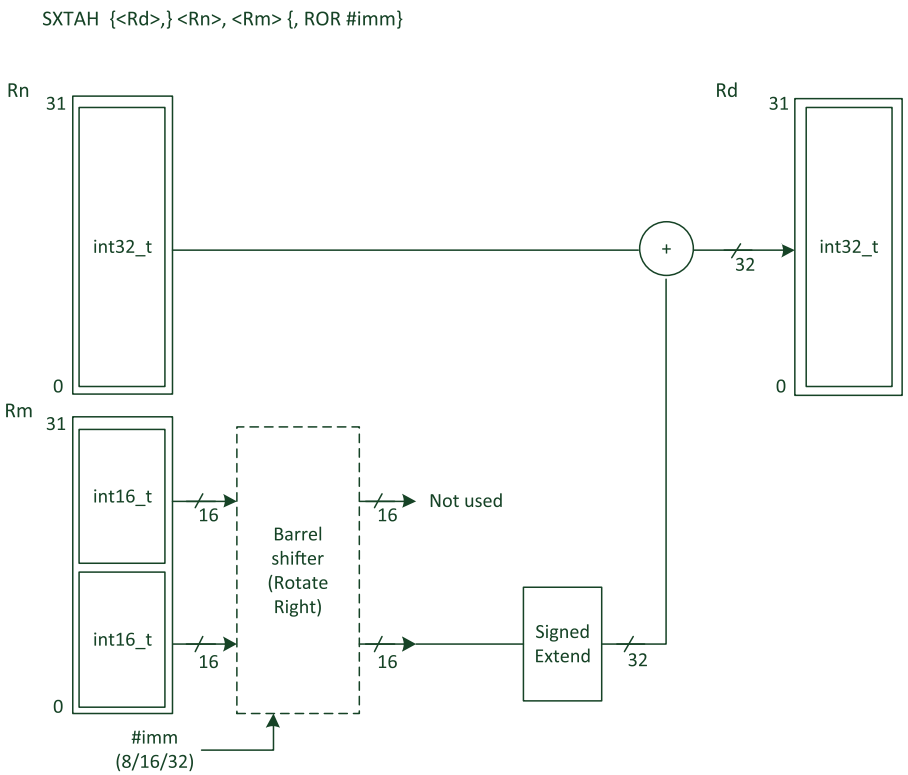

FIGURE B.68

SXTAH

UADD8 {<Rd>,} <Rn>, <Rm>

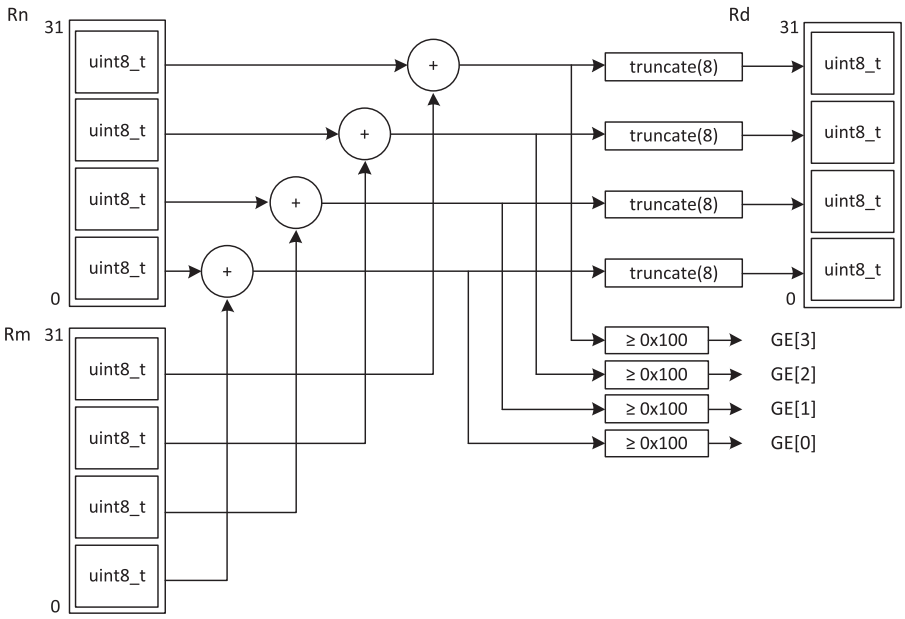

FIGURE B.69

UADD8

UADD16 {<Rd>,} <Rn>, <Rm>

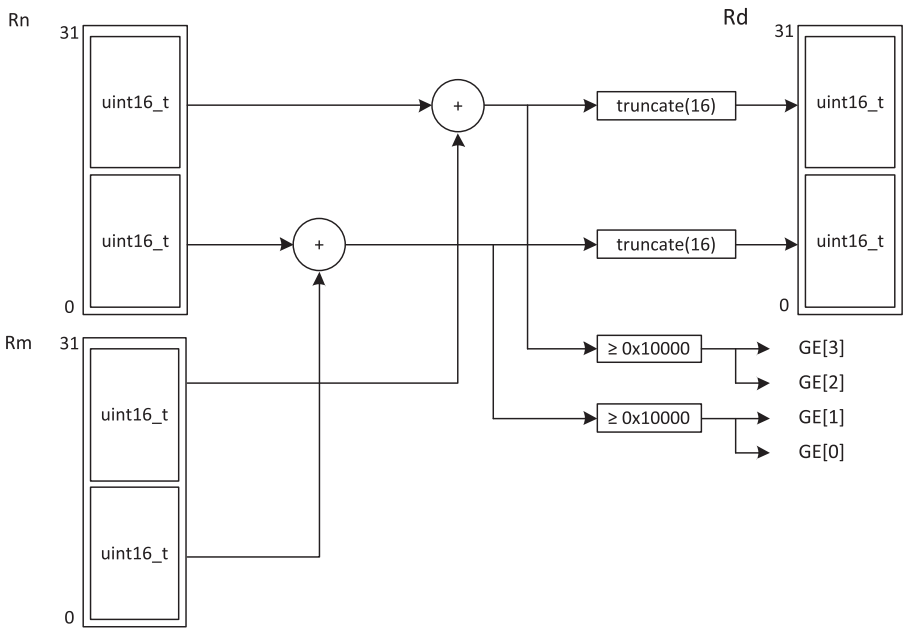

FIGURE B.70

UADD16

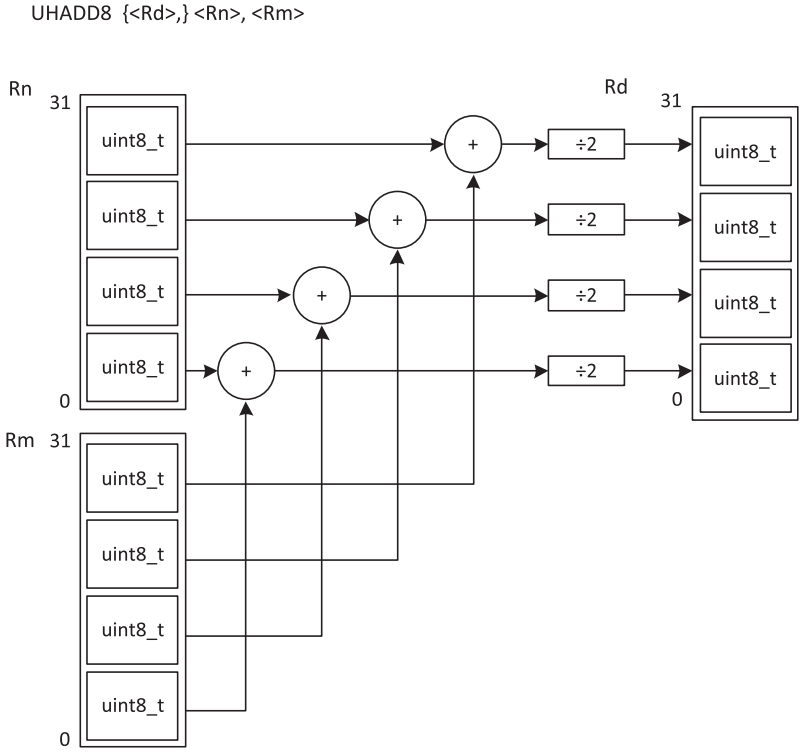

FIGURE B.71

UHADD8

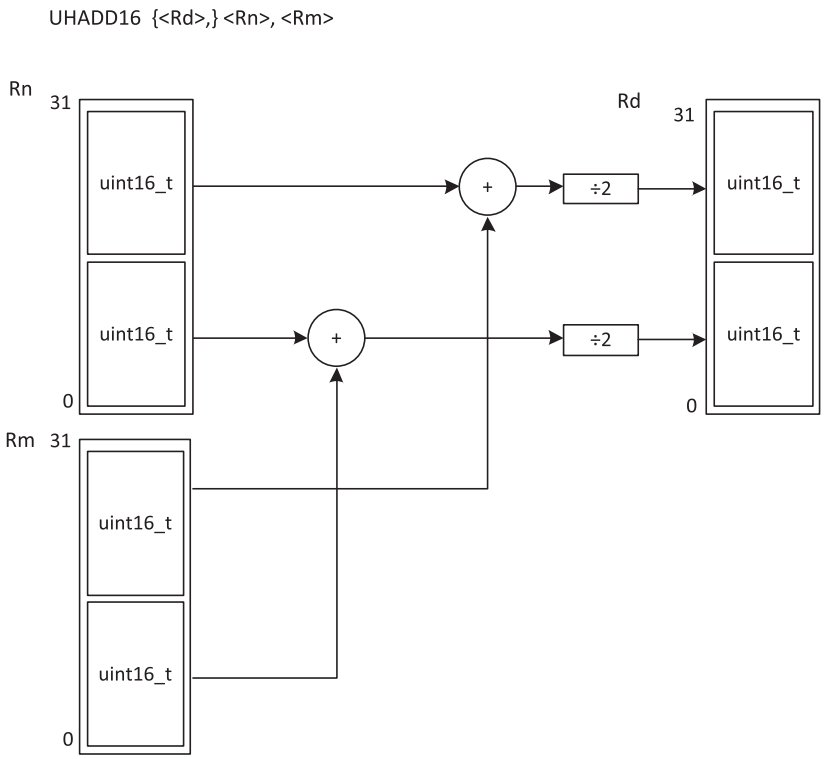

FIGURE B.72

UHADD16

USUB8 {<Rd>,} <Rn>, <Rm>

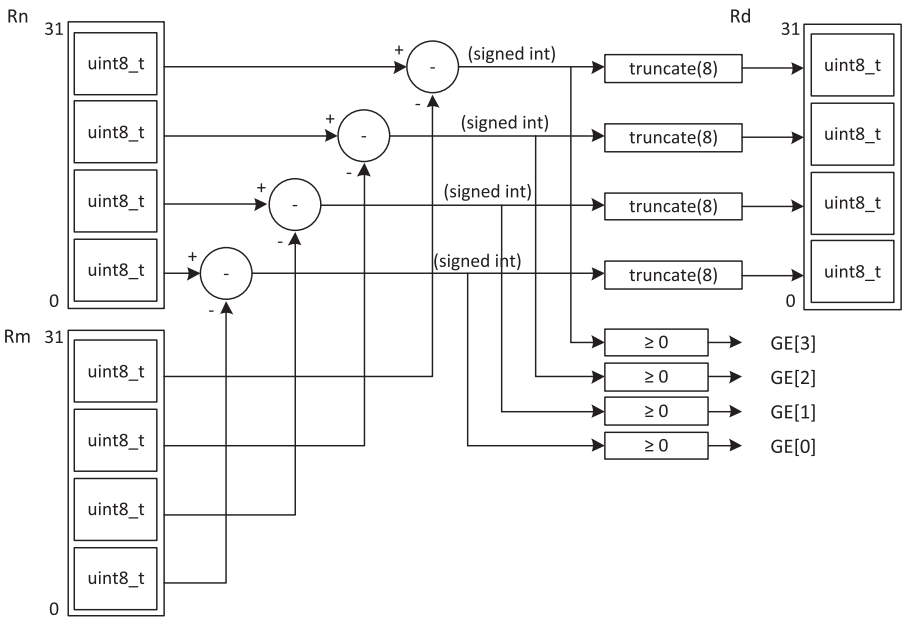

FIGURE B.73

USUB8

USUB168 {<Rd>,} <Rn>, <Rm>

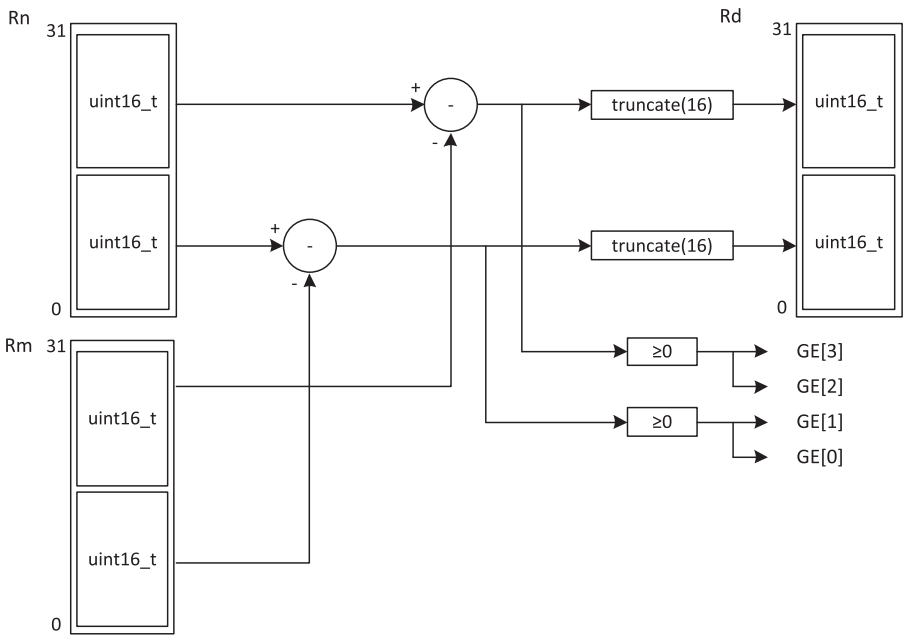

FIGURE B.74

USUB16

UHSUB8 {<Rd>,} <Rn>, <Rm>

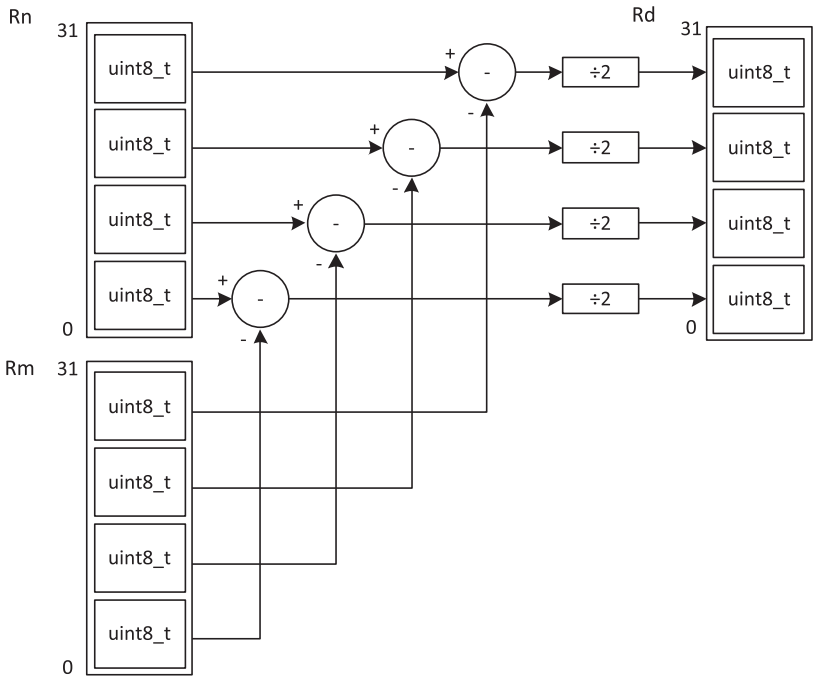

FIGURE B.75

UHSUB8

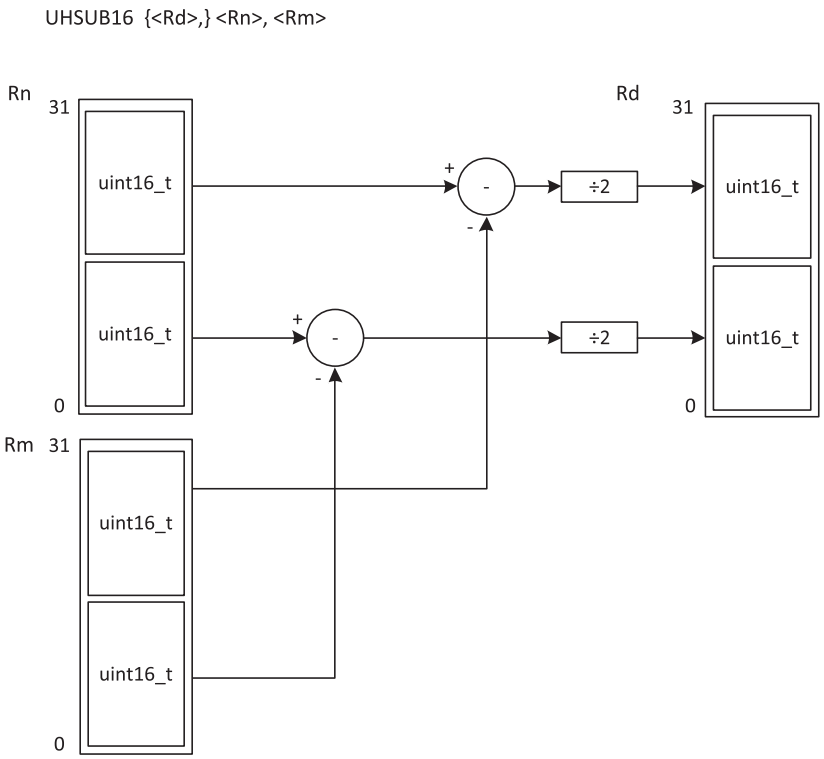

FIGURE B.76

UHSUB16

UASX {<Rd>,} <Rn>, <Rm>

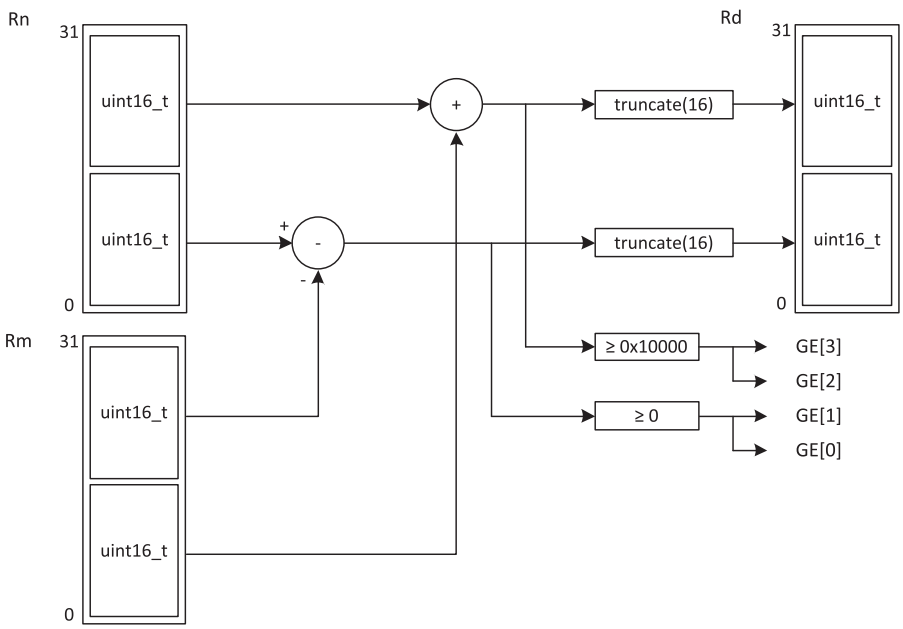

FIGURE B.77

UASX

USAX {<Rd>,} <Rn>, <Rm>

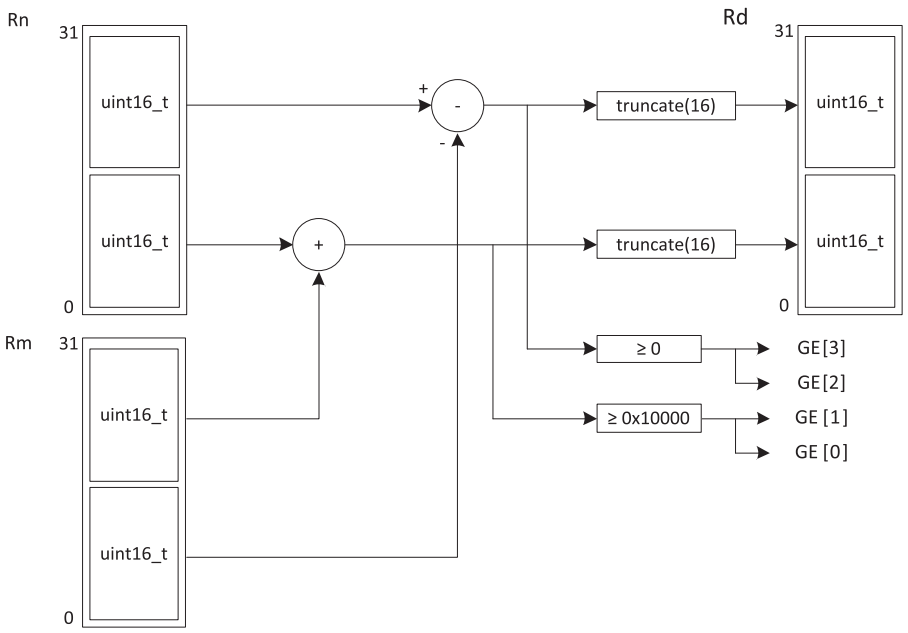

FIGURE B.78

USAX

UHASX {<Rd>,} <Rn>, <Rm>

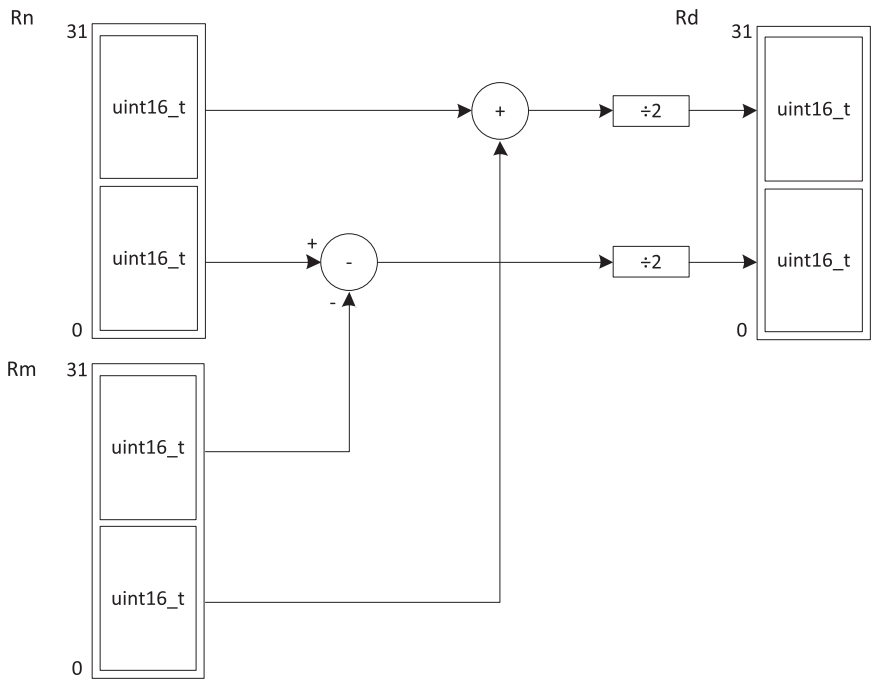

FIGURE B.79

UHASX

UHSAX {<Rd>,} <Rn>, <Rm>

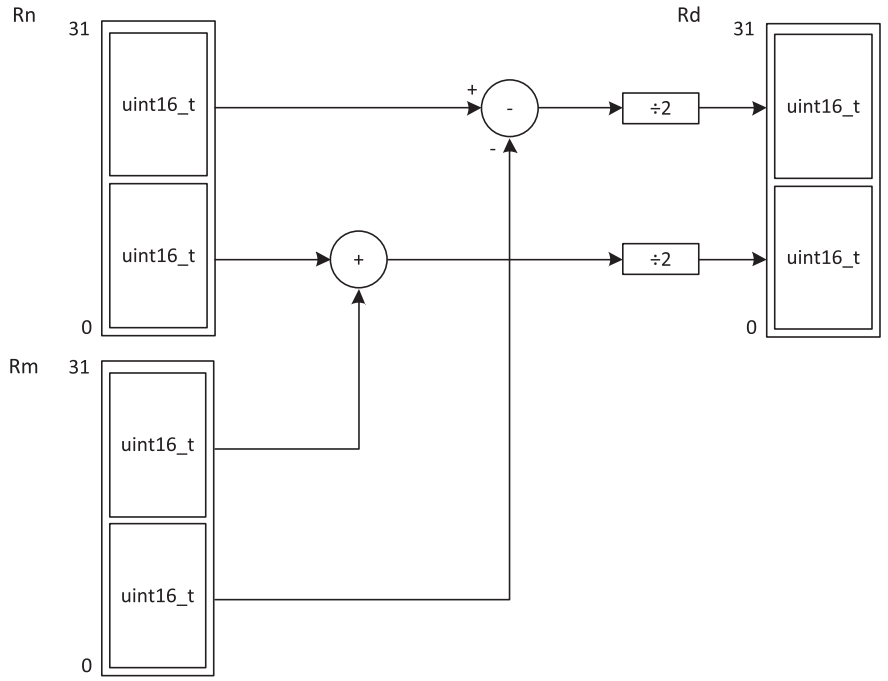

FIGURE B.80

UHSAX

USAD8 {<Rd>,} <Rn>, <Rm>

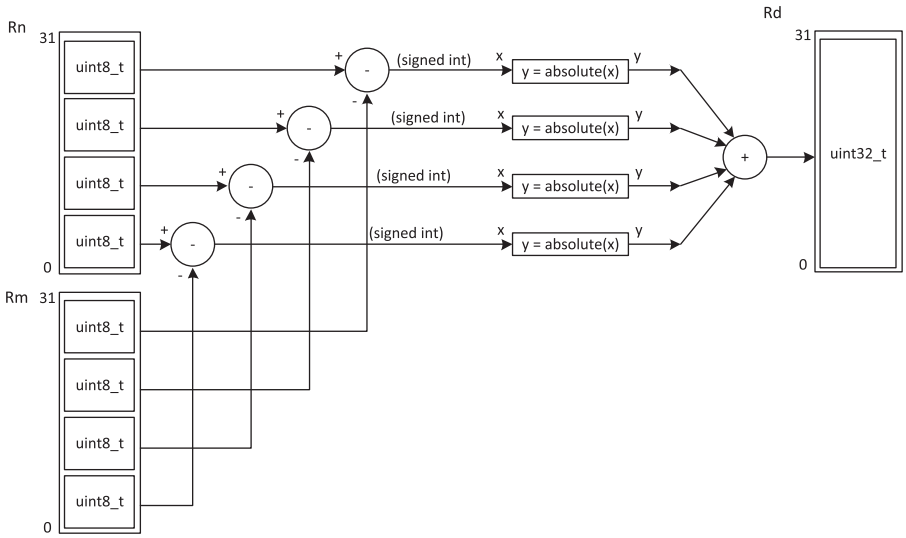

FIGURE B.81

USAD8

USADA8 {<Rd>,} <Rn>, <Rm>

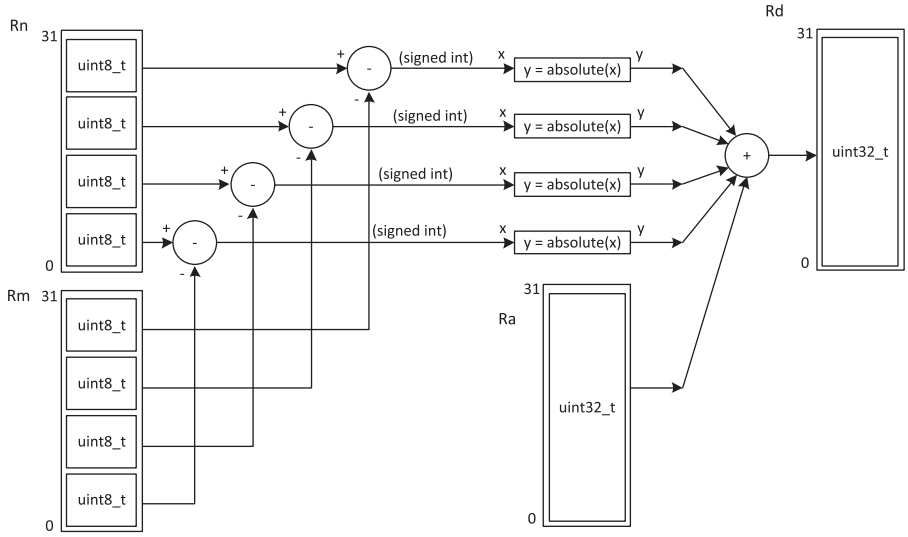

FIGURE B.82

USADA8

USAT16 <Rd>, #imm4, <Rn>

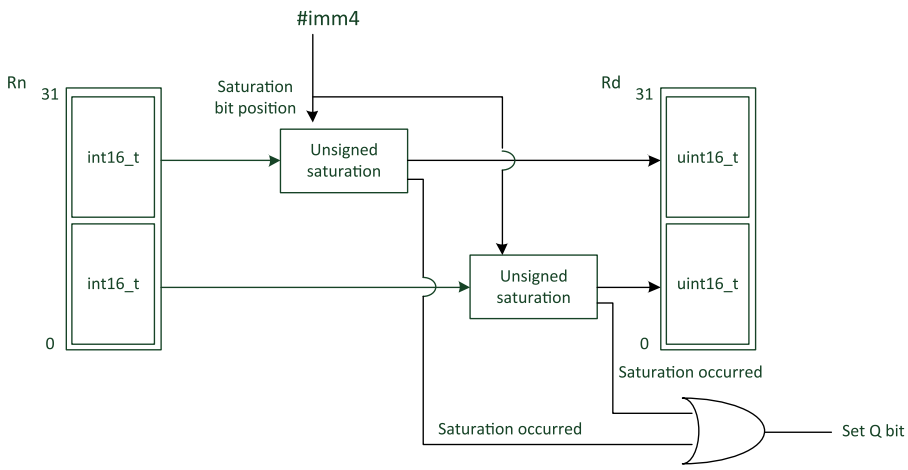

FIGURE B.83

USAT16

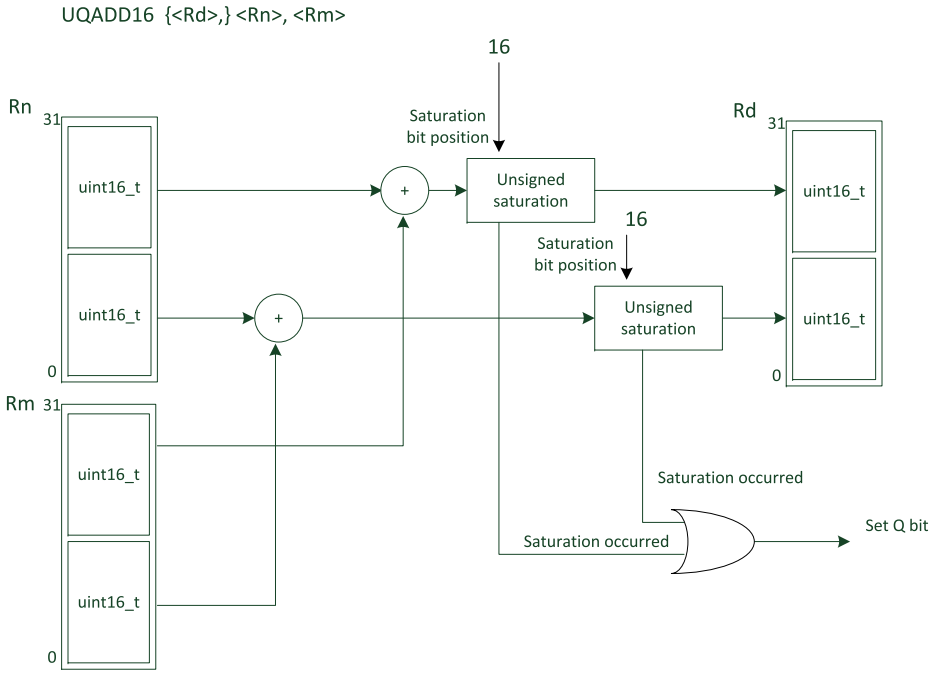

FIGURE B.84

UQADD16

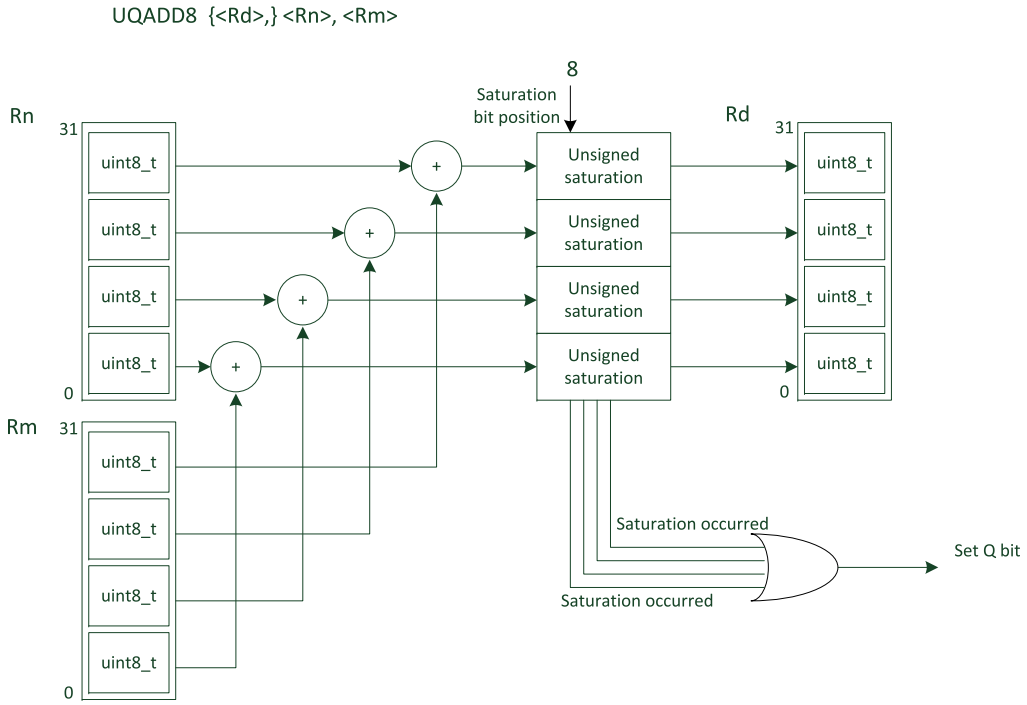

FIGURE B.85

UQADD8

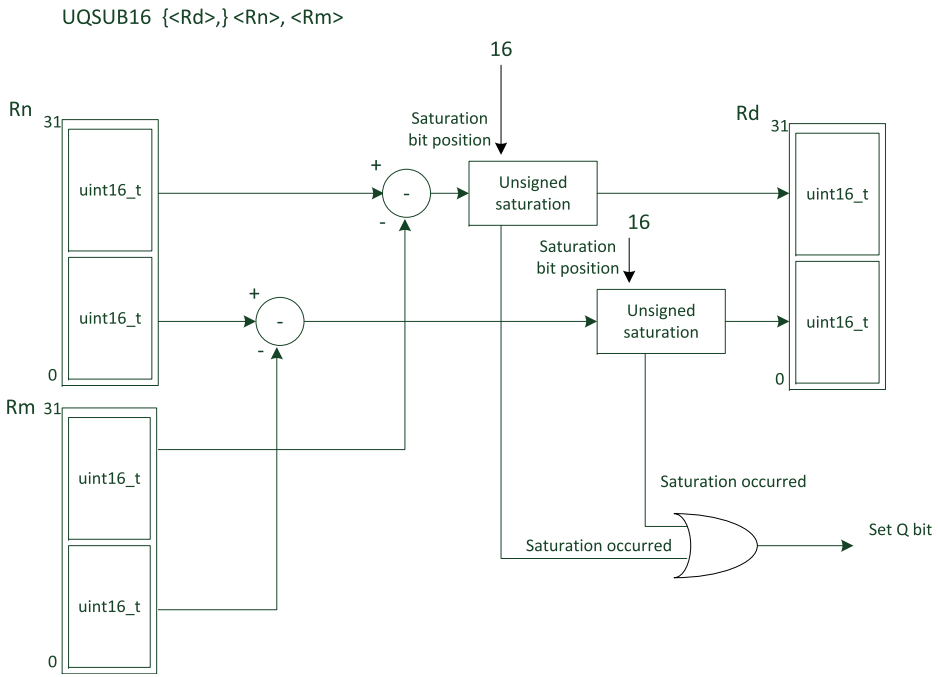

FIGURE B.86

UQSUB16

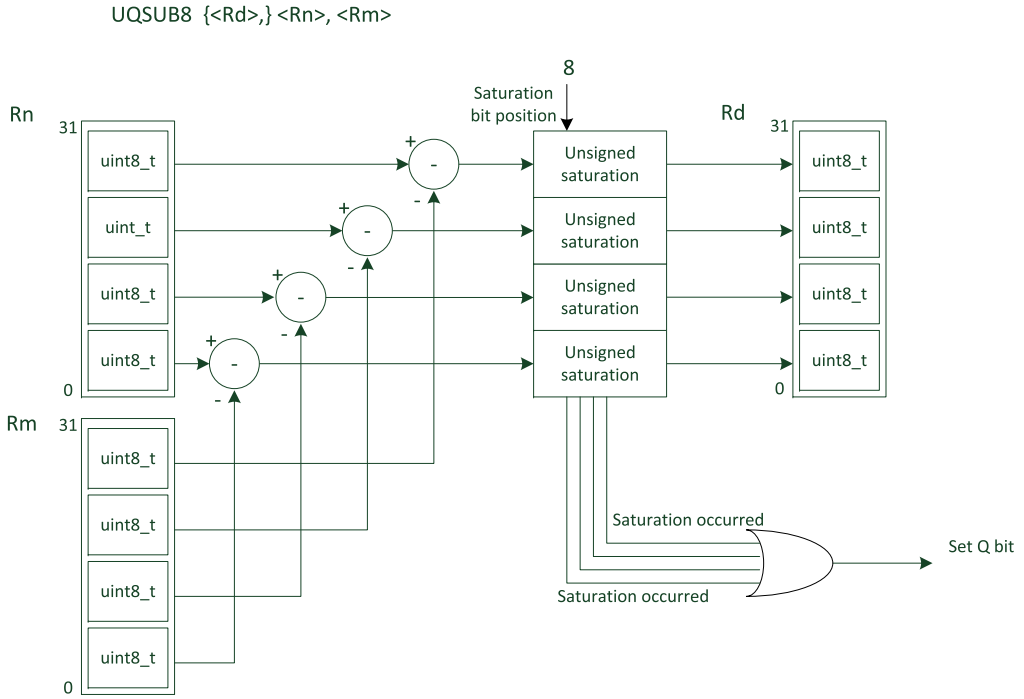

FIGURE B.87

UQSUB8

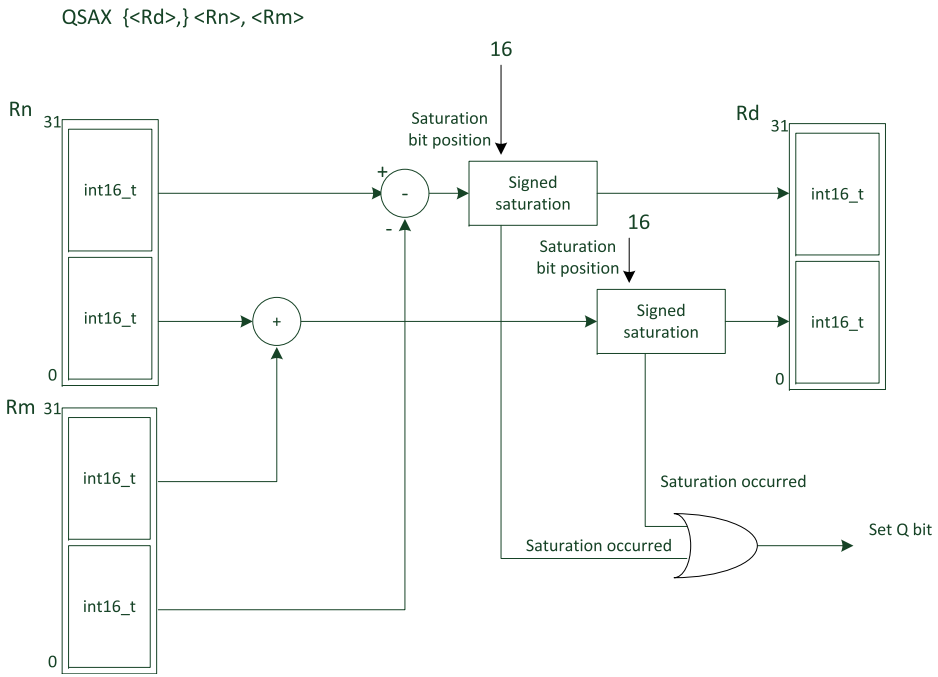

FIGURE B.88

UQASX

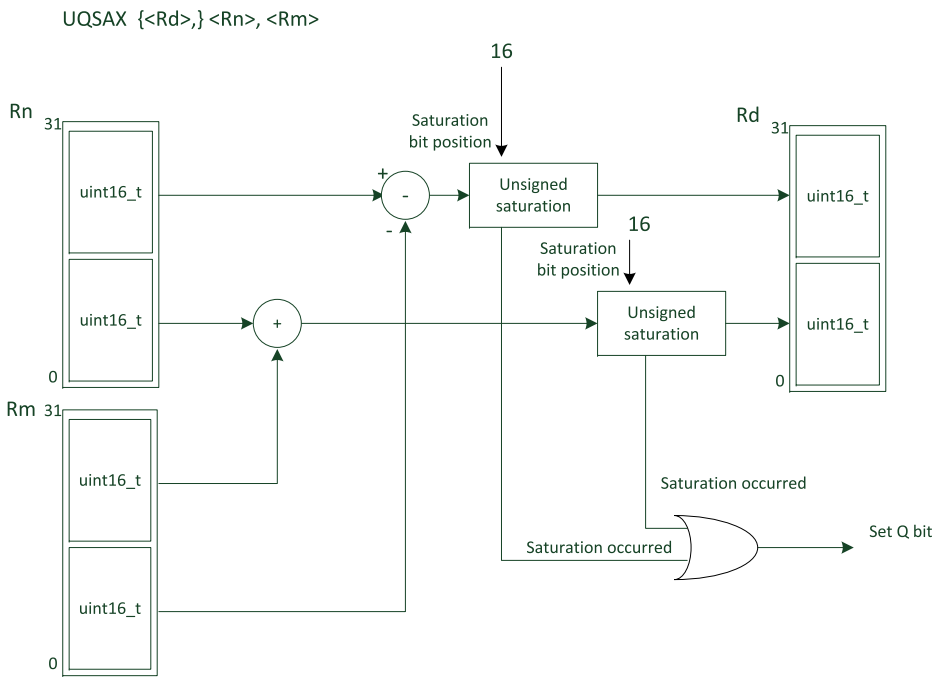

FIGURE B.89

UQSAX

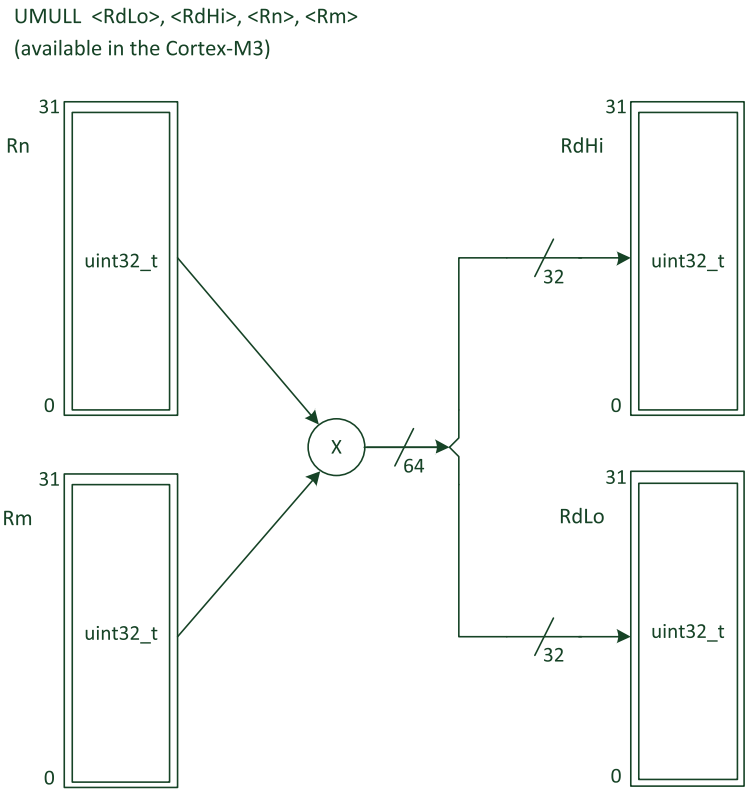

FIGURE B.90

UMULL

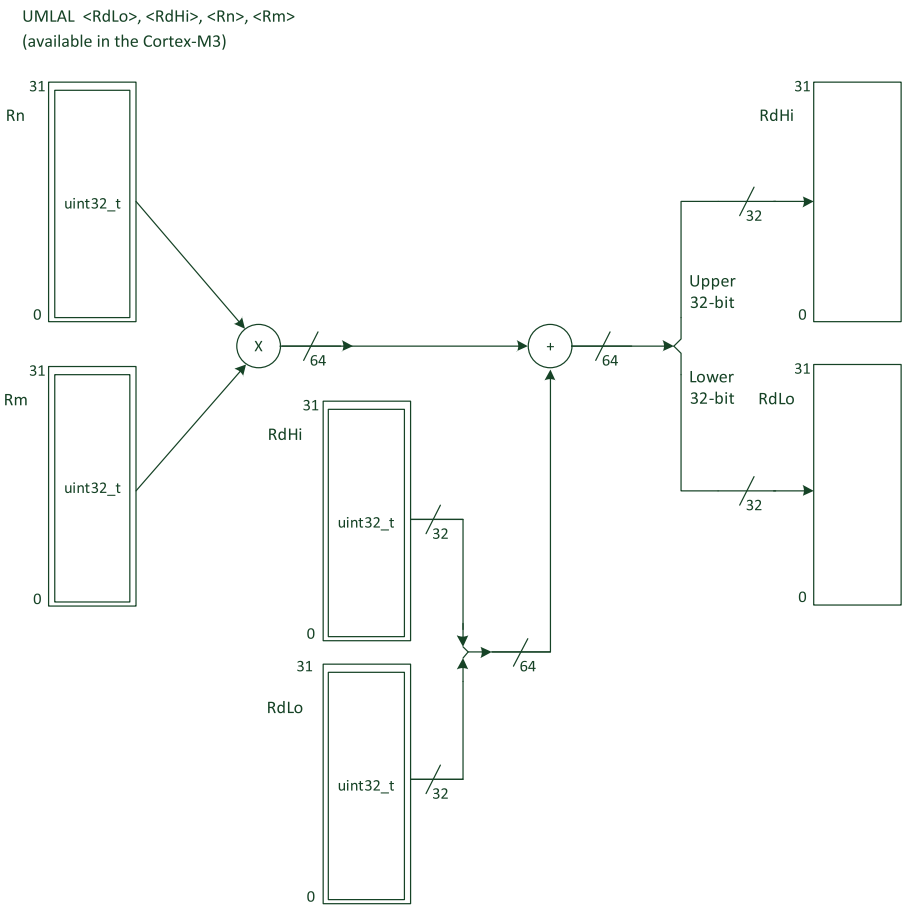

FIGURE B.91

UMLAL

UMAAL <RdLo>, <RdHi>, <Rn>, <Rm>

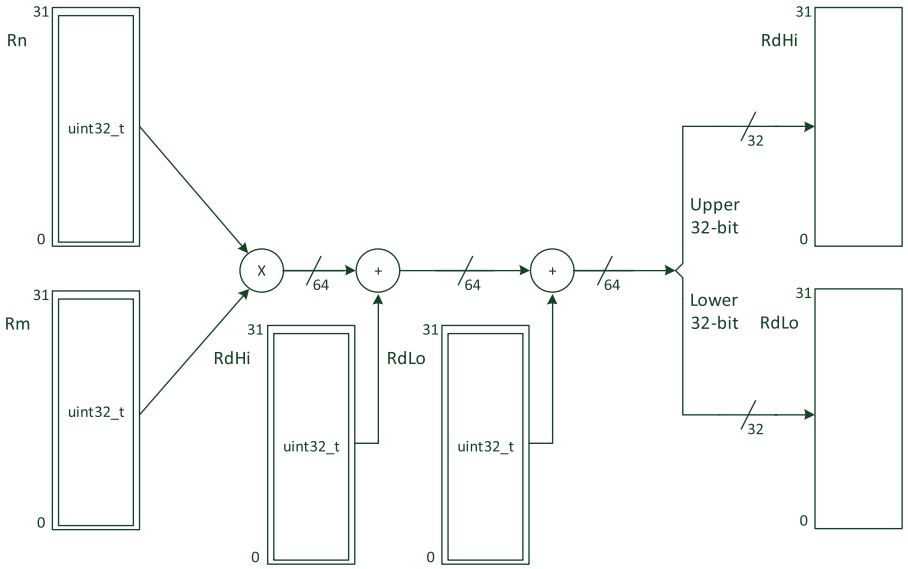

FIGURE B.92

UMAAL

UXTB {<Rd>,} <Rn> {, ROR #imm}
(available in the Cortex-M3)

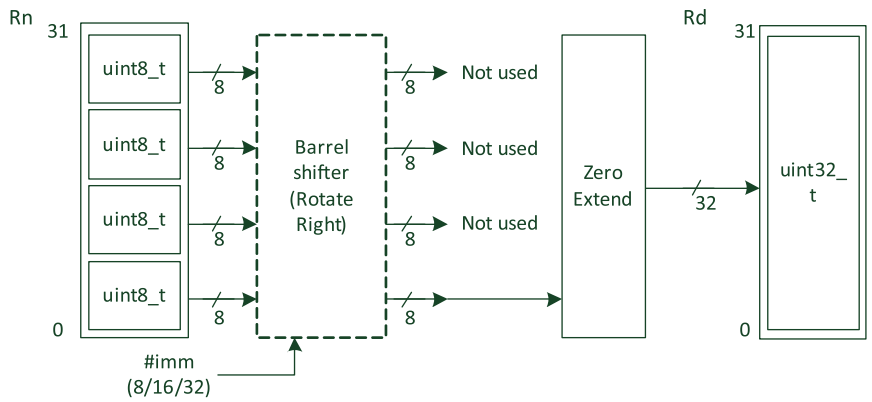

FIGURE B.93

UXTB

UXTB16 {<Rd>,} <Rn> {, ROR #imm}

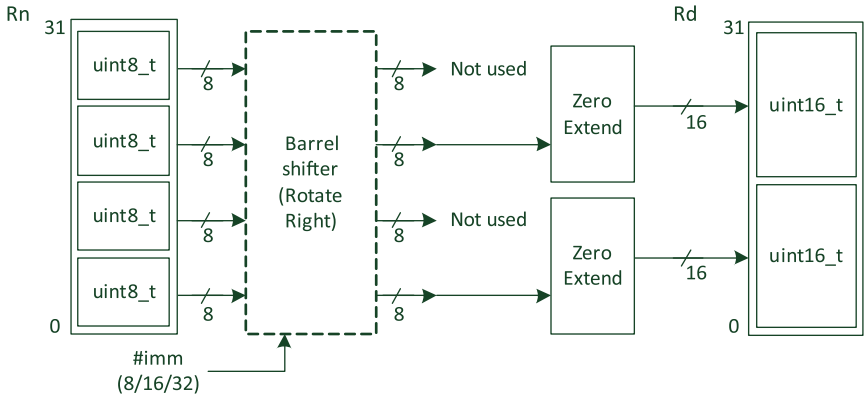

FIGURE B.94

UXTB16

UXTAB {<Rd>,} <Rn>, <Rm> {, ROR #imm}

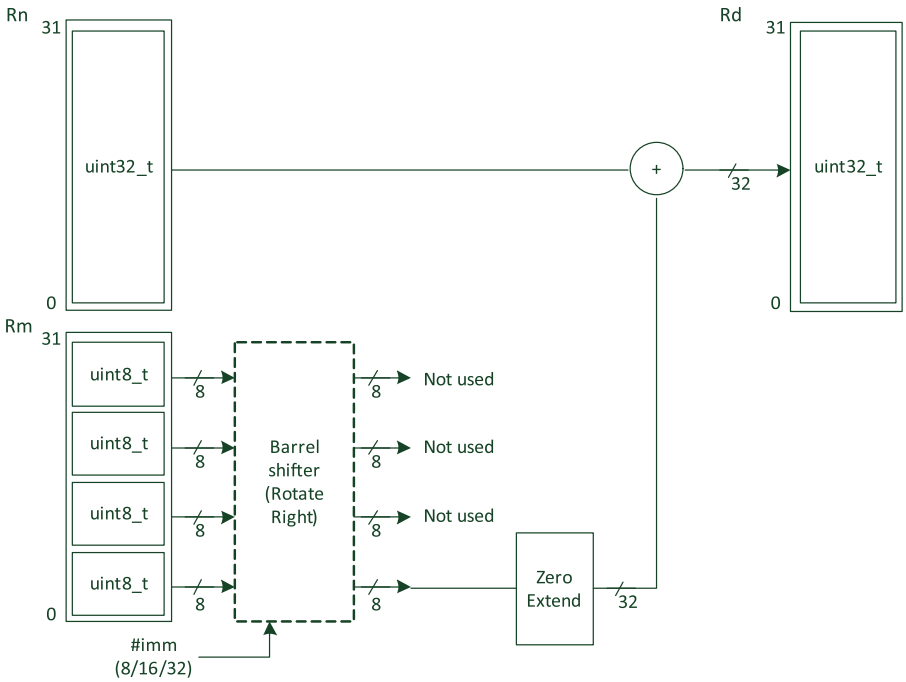

FIGURE B.95

UXTAB

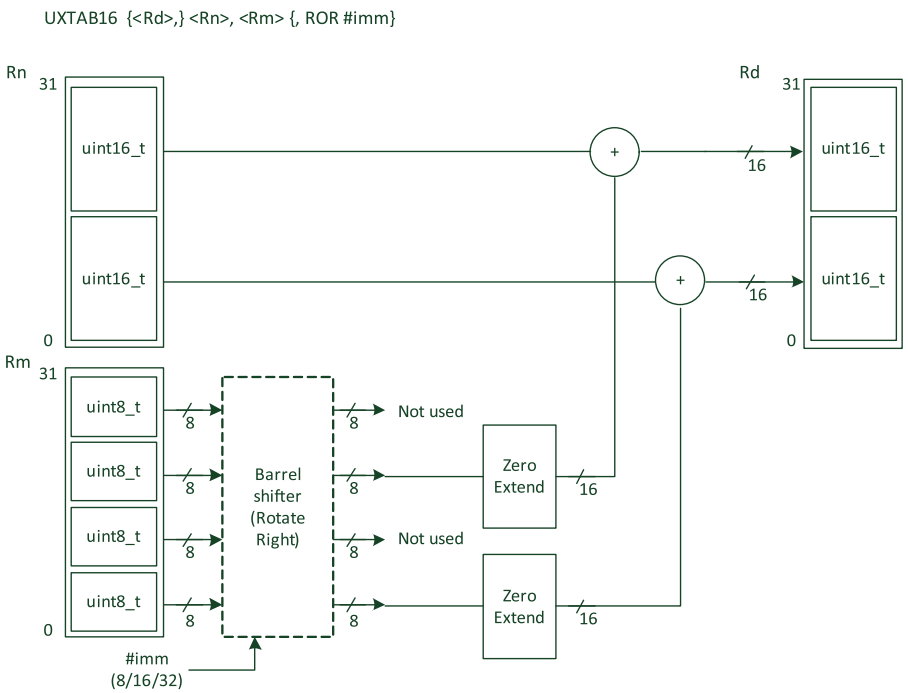

FIGURE B.96

UXTAB16

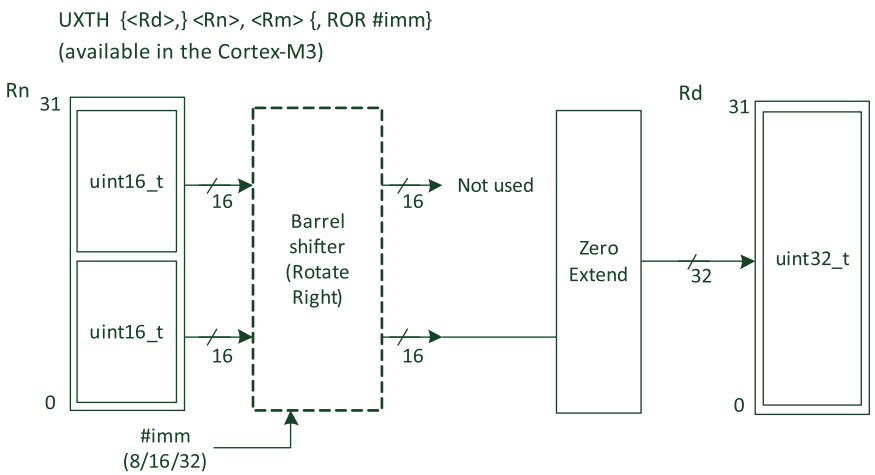

FIGURE B.97

UXTH

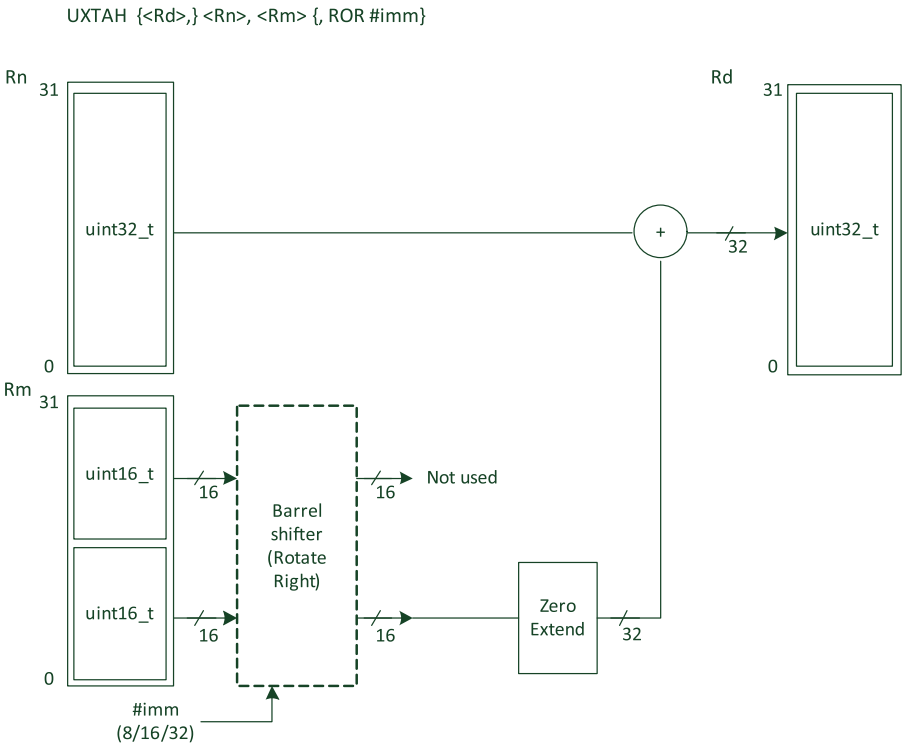

FIGURE B.98

UXTAH