Addition of 16-bit Thumb® Instructions in Recent Architecture Versions

Most of the 16-bit Thumb® instructions are available in architecture v4T (ARM7TDMI™). However, a number of them are added in architecture v5, v6, and v7. Table C.1 lists these instructions.

Table C.1 Change of 16-bit Instruction Support in Various Recent ARM® Architecture Versions

Instruction	v4T	v5	v6	v6T2	Cortex-M3/M4 (v7-M)
BKPT	N	Y	Y	Y	Y
BLX	N	Y	Y	Y	BLX ,reg. only
CBZ, CBNZ	N	N	N	Y	Y
CPS	N	N	Y	Y	CPSIE <i/f>, CPSID <i/f>
CPY	N	N	Y	Y	Y
NOP	N	N	N	Y	Y
IT	N	N	N	Y	Y
REV (various forms)	N	N	Y	Y	REV, REV16, REVSH
SEV	N	N	N	N (1)	Y
SETEND	N	N	Y	Y	N
SWI	Y	Y	Y	Y	Changed to SVC
SXTB, SXTH	N	N	Y	Y	Y
UXTB, UXTH	N	N	Y	Y	Y
WFE, WFI	N	N	N	N (1)	Y

Note 1: SEV, WFE and WFI executes as NOP in v6T2 (First implementation of Thumb 2 on ARM1156T2(F)-S™)