APPENDIX D

Cortex®-M3/M4 Exceptions Quick Reference

D.1 Exception types and enable

D.2 Stack frame format

Note: If double-word stack alignment feature is enabled and the SP was not double-word aligned when the exception occurred, a padding word is inserted to ensure the stack frame is double-word aligned.

Table D.1 Quick Summary of Cortex®-M3/M4 Exception Types and their Configurations

Exception Type	Name	CMSIS-Core Exception Enum	Priority (Level Address)	Enable
1	Reset	–	−3	Always
2	NMI	NonMaskableInt_IRQn	−2	Always
3	Hard fault	HardFault_IRQn	−1	Always
4	MemManage	MemoryManagement_IRQn	Programmable (SCB->SHP[0], 0xE000ED18)	SCB->SHCSR (0xE000ED24) bit[16]
5	BusFault	BusFault_IRQn	Programmable (SCB->SHP[1], 0xE000ED19)	SCB->SHCSR (0xE000ED24) bit[17]
6	Usage fault	UsageFault_IRQn	Programmable (SCB->SHP[2], 0xE000ED1A)	SCB->SHCSR (0xE000ED24) bit[18]
7–10	–	–	–	–
11	SVC	SVCall_IRQn	Programmable (SCB->SHP[7], 0xE000ED1F)	Always
12	Debug monitor	DebugMonitor_IRQn	Programmable (SCB->SHP[8], 0xE000ED20)	CoreDebug->DEMCR (0xE000EDFC) bit[16]
13	–	–	–	–
14	PendSV	PendSV_IRQn	Programmable (SCB->SHP[10], 0xE000ED22)	Always
15	SysTick	SysTick_IRQn	Programmable (SCB->SHP[1], 0xE000ED23)	SysTick->CTRL (0xE000E010) bit[1]
16–255	IRQ	(device specific)	Programmable (NVIC->IP[*n*], 0xE000E400)	NVIC->ISER[] (0xE000E100)

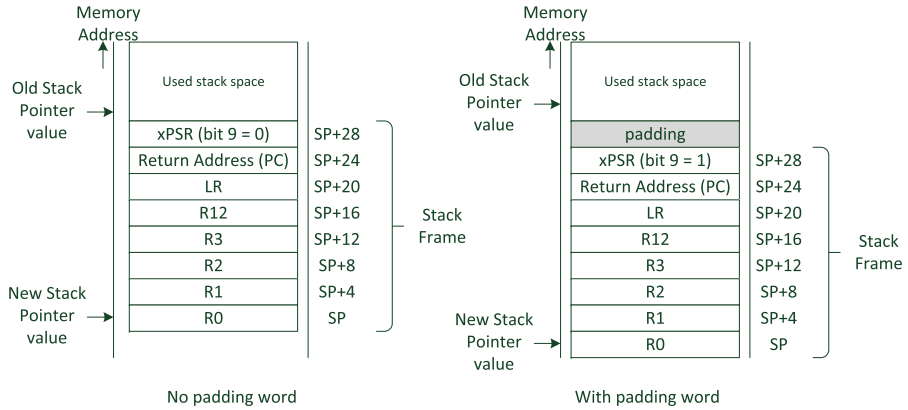

FIGURE D.1

Stack frame without floating point context (EXC_RETURN bit 4 = 1)

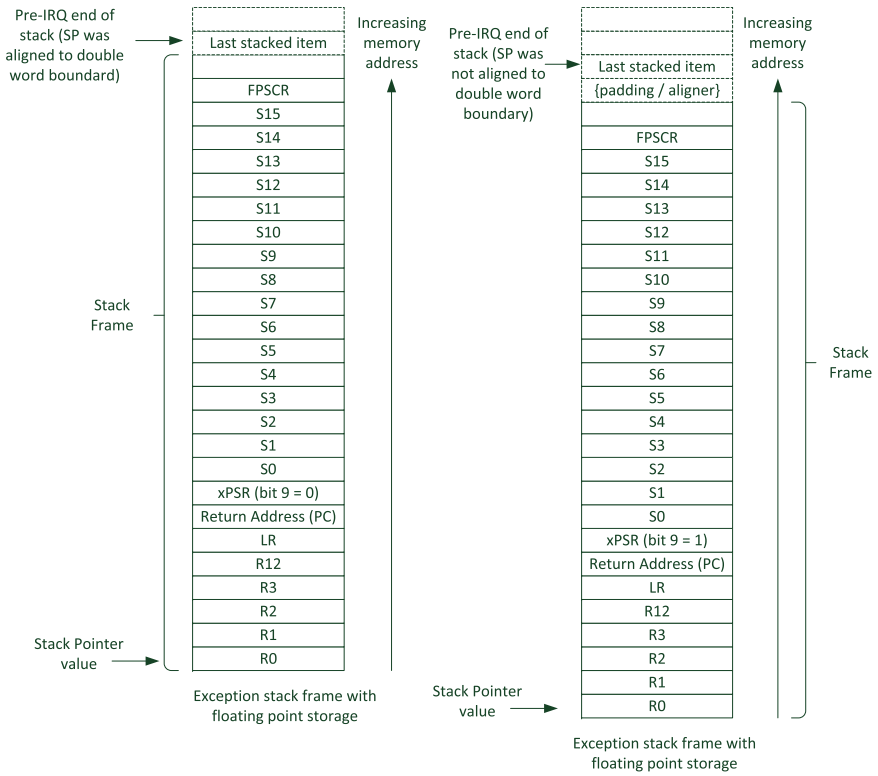

FIGURE D.2

Stack frame with floating point context (EXC_RETURN bit 4 = 0)