NVIC and SCB Registers Quick Reference

F.1 NVIC registers

F.1.1 Interrupt set enable registers

Table F.1 Interrupt Set Enable Registers (0xE000E100-0xE000E11C)

Address	Name	Type	Reset Value	Description
0xE000E100	NVIC->ISER[0]	R/W	0	Enable for external interrupt #0–31 bit[0] for interrupt #0 (exception #16) bit[1] for interrupt #1 (exception #17) … bit[31] for interrupt #31 (exception #47) Write 1 to set bit to 1; write 0 has no effect Read value indicates the current status
0xE000E104	NVIC->ISER[1]	R/W	0	Enable for external interrupt #32–63 Write 1 to set bit to 1; write 0 has no effect Read value indicates the current status
0xE000E108	NVIC->ISER[2]	R/W	0	Enable for external interrupt #64–95 Write 1 to set bit to 1; write 0 has no effect Read value indicates the current status
…	…	…	…	…

F.1.2 Interrupt clear enable registers

Table F.2 Interrupt Clear Enable Registers (0xE000E180-0xE000E19C)

Address	Name	Type	Reset Value	Description
0xE000E180	NVIC->ICER[0]	R/W	0	Clear enable for external interrupt #0–31 bit[0] for interrupt #0 bit[1] for interrupt #1 … bit[31] for interrupt #31 Write 1 to clear bit to 0; write 0 has no effect Read value indicates the current enable status
0xE000E184	NVIC->ICER[1]	R/W	0	Clear Enable for external interrupt #32–63 Write 1 to clear bit to 0; write 0 has no effect Read value indicates the current enable status
0xE000E188	NVIC->ICER[2]	R/W	0	Clear enable for external interrupt #64–95 Write 1 to clear bit to 0; write 0 has no effect Read value indicates the current enable status
…	…	…	…	…

F.1.3 Interrupt set pending registers

Table F.3 Interrupt Set Pending Registers (0xE000E200-0xE000E21C)

Address	Name	Type	Reset Value	Description
0xE000E200	NVIC->ISPR[0]	R/W	0	Pending for external interrupt #0–31 bit[0] for interrupt #0 (exception #16) bit[1] for interrupt #1 (exception #17) … bit[31] for interrupt #31 (exception #47) Write 1 to set bit to 1; write 0 has no effect Read value indicates the current status

Table F.3 Interrupt Set Pending Registers (0xE000E200-0xE000E21C)—Cont'd

Address	Name	Type	Reset Value	Description
0xE000E204	NVIC->ISPR[1]	R/W	0	Pending for external interrupt #32–63 Write 1 to set bit to 1; write 0 has no effect Read value indicates the current status
0xE000E208	NVIC->ISPR[2]	R/W	0	Pending for external interrupt #64–95 Write 1 to set bit to 1; write 0 has no effect Read value indicates the current status
…	…	…	…	…

F.1.4 Interrupt clear pending registers

Table F.4 Interrupt Clear Pending Registers (0xE000E280-0xE000E29C)

Address	Name	Type	Reset Value	Description
0xE000E280	NVIC->ICPR[0]	R/W	0	Clear pending for external interrupt #0–31 bit[0] for interrupt #0 (exception #16) bit[1] for interrupt #1 (exception #17) … bit[31] for interrupt #31 (exception #47) Write 1 to clear bit to 0; write 0 has no effect Read value indicates the current pending status
0xE000E284	NVIC->ICPR[1]	R/W	0	Clear pending for external interrupt #32–63 Write 1 to clear bit to 0; write 0 has no effect Read value indicates the current pending status

(*Continued*)

Table F.4 Interrupt Clear Pending Registers (0xE000E280-0xE000E29C)—Cont'd

Address	Name	Type	Reset Value	Description
0xE000E288	NVIC->ICPR[2]	R/W	0	Clear pending for external interrupt #64–95 Write 1 to clear bit to 1; write 0 has no effect Read value indicates the current pending status
…	…	…	…	…

F.1.5 Interrupt active status registers

Table F.5 Interrupt Active Status Registers (0xE000E300-0xE000E31C)

Address	Name	Type	Reset Value	Description
0xE000E300	NVIC-> IABR[0]	R	0	Active status for external interrupt #0–31 bit[0] for interrupt #0 bit[1] for interrupt #1 … bit[31] for interrupt #31
0xE000E304	NVIC-> IABR[1]	R	0	Active status for external interrupt #32–63
…	–	–	–	–

F.1.6 Interrupt priority level registers

Table F.6 Interrupt Priority Level Registers (0xE000E400-0xE000E4EF)

Address	Name	Type	Reset Value	Description
0xE000E400	NVIC->IP[0]	R/W	0 (8-bit)	Priority level external interrupt #0
0xE000E401	NVIC->IP[1]	R/W	0 (8-bit)	Priority level external interrupt #1
…	–	–	–	–
0xE000E41F	NVIC->IP[31]	R/W	0 (8-bit)	Priority level external interrupt #31
…	–	–	–	–

F.1.7 Software trigger interrupt register

Table F.7 Software Trigger Interrupt Register (0xE000EF00)

Bits	Name	Type	Reset Value	Description
8:0	NVIC->STIR	W	–	Writing the interrupt number sets the pending bit of the interrupt; for example, write 0 to pend external interrupt #0

F.2 SCB registers

F.2.1 CPU ID register

Table F.8 CPU ID Base Register (SCB->CPUID, 0xE000ED00)

Processor and Revisions	Implementer Bit [31:24]	Variant Bit [23:20]	Constant Bit [19:16]	PartNo Bit [15:4]	Revision Bit [3:0]
Cortex®-M0 - r0p0	0x41	0x0	0xC	0xC20	0x0
Cortex-M0+ - r0p0	0x41	0x0	0xC	0xC60	0x0
Cortex-M1 - r0p1	0x41	0x0	0xC	0xC21	0x0
Cortex-M1 - r0p1	0x41	0x0	0xC	0xC21	0x1
Cortex-M1 - r1p0	0x41	0x1	0xC	0xC21	0x0
Cortex-M3 - r0p0	0x41	0x0	0xF	0xC23	0x0
Cortex-M3 - r1p0	0x41	0x0	0xF	0xC23	0x1
Cortex-M3 - r1p1	0x41	0x1	0xF	0xC23	0x1
Cortex-M3 - r2p0	0x41	0x2	0xF	0xC23	0x0
Cortex-M3 - r2p1	0x41	0x2	0xF	0xC23	0x1
Cortex-M4 - r0p0	0x41	0x0	0xF	0xC24	0x0
Cortex-M4 - r0p1	0x41	0x0	0xF	0xC24	0x1

F.2.2 Interrupt control and state register

Table F.9 Interrupt Control and State Register (SCB->ICSR, 0xE000ED04)

Bits	Name	Type	Reset Value	Description
31	NMIPENDSET	R/W	0	NMI pended
28	PENDSVSET	R/W	0	Write 1 to pend system call Read value indicates pending status
27	PENDSVCLR	W	0	Write 1 to clear PendSV pending status
26	PENDSTSET	R/W	0	Write 1 to pend SYSTICK exception Read value indicates pending status
25	PENDSTCLR	W	0	Write 1 to clear SYSTICK pending status
23	ISRPREEMPT	R	0	Indicates that a pending interrupt is going to be active in the next step (for debug)
22	ISRPENDING	R	0	External interrupt pending (excluding system exceptions such as NMI for fault)
21:12	VECTPENDING	R	0	Pending ISR number
11	RETTOBASE	R	0	Set to 1 when the processor is running an exception handler; will return to Thread level if interrupt return and no other exceptions pending
9:0	VECTACTIVE	R	0	Current running interrupt service routine

F.2.3 Vector table offset register

Table F.10 Vector Table Offset Register in Cortex®-M4 or Cortex-M3 r2p1

Bits	Name	Type	Reset Value	Description
31:7	TBLOFF	R/W	0	Vector table offset value

Table F.11 Vector Table Offset Register in Cortex-M3 r2p0 or Earlier Versions

Bits	Name	Type	Reset Value	Description
31:30	Reserved	-	-	Not implemented, tied to 0
29	TBLBASE	R/W	0	Table base in Code (0) or RAM (1)
28:7	TBLOFF	R/W	0	Table offset value from Code region or RAM region

F.2.4 Application interrupt and reset control register

Table F.12 Application Interrupt and Reset Control Register (SCB->AIRCR, address 0xE000ED0C)

Bits	Name	Type	Reset Value	Description
31:16	VECTKEY	R/W	–	Access key; 0x05FA must be written to this field to write to this register, otherwise the write will be ignored; the read-back value of the upper half word is 0xFA05
15	ENDIANNESS	R	–	Indicates endianness for data: 1 for big endian (BE8) and 0 for little endian; this can only change after a reset
10:8	PRIGROUP	R/W	0	Priority group
2	SYSRESETREQ	W	–	Requests chip control logic to generate a reset
1	VECTCLRACTIVE	W	–	Clears all active state information for exceptions; typically used in debug or OS to allow system to recover from system error (Reset is safer)
0	VECTRESET	W	–	Resets the Cortex-M3/M4 processor (except debug logic), but this will not reset circuits outside the processor. This is intended for debug operations. Do not use this at the same time as SYSRESETREQ.

F.2.5 System control register

Table F.13 System Control Register (SCB->SCR, 0xE000ED10)

Bits	Name	Type		Reset Value	Description
4	SEVONPEND	R/W		0	Send Event on Pending; when this is set to 1, the processor wakes up from WFE if a new interrupt is pended, regardless of whether the interrupt has priority higher than the current level and whether it was enabled
3	Reserved	–		–	–
2	SLEEPDEEP	R/W		0	When set to 1, the Deep Sleep mode is selected. Otherwise the sleep mode is selected.
1	SLEEPONEXIT	R/W		0	When this bit is set to 1, it enables the Sleep-On-Exit feature, which cause the processor to enter sleep mode automatically when exiting an exception handler and is returning to Thread.
0	Reserved	–		–	–

F.2.6 Configuration control register

Table F.14 Configuration Control Register (SCB->CCR, 0xE000ED14)

Bits	Name	Type	Reset Value	Descriptions
9	STKALIGN	R/W	0 or 1	Force exception stacking start in double word aligned address. This bit is reset as zero on Cortex -M3 revision r1p0 and r1p1, and is reset as one on revision 2. Cortex-M3 Revision r0p0 does not have this feature. In Cortex-M4 this bit is reset as 1.

Table F.14 Configuration Control Register (SCB->CCR, 0xE000ED14)—Cont'd

Bits	Name	Type	Reset Value	Descriptions
8	BFHFNMIGN	R/W	0	Ignore data bus fault during HardFault and NMI handlers.
7:5	Reserved	-	-	Reserved
4	DIV_0_TRP	R/W	0	Trap on divide by 0
3	UNALIGN_TRP	R/W	0	Trap on unaligned accesses.
2	Reserved	-	-	Reserved
1	USERSETMPEND	R/W	0	If set to 1, allow unprivileged user code to write to Software Trigger Interrupt Register.
0	NONBASETHRDENA	R/W	0	Non-base thread enable. If set to 1, allows exception handler to return to thread state at any level by controlling EXC_RETURN value.

F.2.7 System handler priority registers

Table F.15 System Handler Priority Registers (SysTick->CTRL, SCB->SHP[0 to 11])

Address	Name	Type	Reset Value	Description
0xE000ED18	SCB->SHP[0]	R/W	0 (8-bit)	MemManage Fault priority level
0xE000ED19	SCB->SHP[1]	R/W	0 (8-bit)	Bus Fault Priority level
0xE000ED1A	SCB->SHP[2]	R/W	0 (8-bit)	Usage Fault priority level
0xE000ED1B	SCB->SHP[3]	–	–	– (not implemented)
0xE000ED1C	SCB->SHP[4]	–	–	– (not implemented)
0xE000ED1D	SCB->SHP[5]	–	–	– (not implemented)
0xE000ED1E	SCB->SHP[6]	–	–	– (not implemented)
0xE000ED1F	SCB->SHP[7]	R/W	0 (8-bit)	SVC Priority level
0xE000ED20	SCB->SHP[8]	R/W	0 (8-bit)	Debug Monitor priority level
0xE000ED21	SCB->SHP[9]	–	–	– (not implemented)
0xE000ED22	SCB->SHP[10]	R/W	0 (8-bit)	PendSV Priority level
0xE000ED23	SCB->SHP[11]	R/W	0 (8-bit)	SysTick Priority level

F.2.8 System handler control and state register

Table F.16 System Handler Control and State Register (SCB->SHCSR, address 0xE000ED24)

Bits	Name	Type	Reset Value	Description
18	USGFAULTENA	R/W	0	Usage fault handler enable
17	BUSFAULTENA	R/W	0	Bus fault handler enable
16	MEMFAULTENA	R/W	0	Memory management fault enable
15	SVCALLPENDED	R/W	0	SVC pended; SVCall was started but was replaced by a higher-priority exception
14	BUSFAULTPENDED	R/W	0	Bus fault pended; bus fault handler was started but was replaced by a higher-priority exception
13	MEMFAULTPENDED	R/W	0	Memory management fault pended; memory management fault started but was replaced by a higher-priority exception
12	USGFAULTPENDED	R/W	0	Usage fault pended; usage fault started but was replaced by a higher-priority exception
11	SYSTICKACT	R/W	0	Read as 1 if SYSTICK exception is active
10	PENDSVACT	R/W	0	Read as 1 if PendSV exception is active
8	MONITORACT	R/W	0	Read as 1 if debug monitor exception is active
7	SVCALLACT	R/W	0	Read as 1 if SVCall exception is active
3	USGFAULTACT	R/W	0	Read as 1 if usage fault exception is active
1	BUSFAULTACT	R/W	0	Read as 1 if bus fault exception is active
0	MEMFAULTACT	R/W	0	Read as 1 if memory management fault is Active

F.2.9 Configurable fault status register

Table F.17 Configurable Fault Status Register (SCB->CFSR)

Bits	Name	Type	Reset Value	Description
25	DIVBYZERO	R/Wc	0	Indicates a divide by zero has taken place (can be set only if DIV_0_TRP is set)
24	UNALIGNED	R/Wc	0	Indicates that an unaligned access fault has taken place
23:20	–	–	–	–
19	NOCP	R/Wc	0	Attempts to execute a co-processor instruction
18	INVPC	R/Wc	0	Attempts to do an exception with a bad value in the EXC_RETURN number
17	INVSTATE	R/Wc	0	Attempts to switch to an invalid state (e.g., ARM)
16	UNDEFINSTR	R/Wc	0	Attempts to execute an undefined instruction
15	BFARVALID	–	0	Indicates BFAR is valid
14	–	–	–	–
13	LSPERR	R/Wc	0	Floating Point lazy stacking error (available on Cortex-M4 with floating point unit only)
12	STKERR	R/Wc	0	Stacking error (Bus Error)
11	UNSTKERR	R/Wc	0	Unstacking error (Bus Error)
10	IMPRECISERR	R/Wc	0	Imprecise data access error
9	PRECISERR	R/Wc	0	Precise data access error
8	IBUSERR	R/Wc	0	Instruction access error
7	MMARVALID	–	0	Indicates the MMFAR is valid
6	–	–	– (read as 0)	Reserved
5	MLSPERR	R/Wc	0	Floating Point lazy stacking error (available on Cortex-M4 with floating point unit only)
4	MSTKERR	R/Wc	0	Stacking error
3	MUNSTKERR	R/Wc	0	Unstacking error
2	–	–	– (read as 0)	Reserved
1	DACCVIOL	R/Wc	0	Data access violation
0	IACCVIOL	R/Wc	0	Instruction access violation

F.2.10 Hard fault status register

Table F.18 Hard Fault Status Register (0xE000ED2C, SCB->HFSR)

Bits	Name	Type	Reset Value	Description
31	DEBUGEVT	R/Wc	0	Indicates hard fault is triggered by debug event
30	FORCED	R/Wc	0	Indicates hard fault is taken because of bus fault, memory management fault, or usage fault
29:2	–	–	–	–
1	VECTBL	R/Wc	0	Indicates hard fault is caused by failed vector fetch
0	–	–	–	–

F.2.11 Debug fault status register

Table F.19 Debug Fault Status Register (0xE000ED30, SCB->DFSR)

Bits	Name	Type	Reset Value	Description
31:5	-	-	-	Reserved
4	EXTERNAL	R/Wc	0	Indicates the debug event is caused by an external signal (the EDBGRQ signal is an input on the processor, typically used in multi-processor design for synchronized debug).
3	VCATCH	R/Wc	0	Indicates the debug event is caused by a vector catch, a programmable feature that allows the processor to halt automatically when entering certain type of system exception including reset.
2	DWTTRAP	R/Wc	0	Indicates the debug event is caused by a watchpoint.
1	BKPT	R/Wc	0	Indicates the debug event is caused by a breakpoint.
0	HALTED	R/Wc	0	Indicates the processor is halted is by debugger request (including single step).

F.2.12 MemManage fault address register

Table F.20 MemManage Fault Address Register (0xE000ED34, SCB->MMFAR)

Bits	Name	Type	Reset Value	Description
31:0	ADDRESS	R/W	Unpredictable	When the value of MMARVALID is 1, this field holds the address of the address location that generates the MemManage Fault.

F.2.13 Bus fault address register

Table F.21 Bus Fault Address Register (0xE000ED38, SCB->BFAR)

Bits	Name	Type	Reset Value	Description
31:0	ADDRESS	R/W	Unpredictable	When the value of BFARVALID is 1, this field holds the address of the address location that generates the Bus Fault.

F.2.14 Auxiliary fault status register

Table F.22 Auxiliary Fault Status Register (0xE000ED3C, SCB->AFSR)

Bits	Name	Type	Reset Value	Description
31:0	Implementation Defined	R/W	0	Implementation defined fault status

F.2.15 Co-processor access control register

Table F.23 Co-processor Access Control Register (SCB->CPACR, 0xE000ED88, available in Cortex-M4 with floating point unit only)

Bits	Name	Type	Reset Value	Descriptions
31:24	Reserved	-	-	Reserved. Read as Zero. Write ignore
23:22	CP11	R/W	0	Access for floating point unit
21:20	CP10	R/W	0	Access for floating point unit
19:0	Reserved	-	-	Reserved. Read as Zero. Write ignore

F.3 Other system control registers not in SCB data structure

F.3.1 Interrupt controller type register

Table F.24 Interrupt Controller Type Register (0xE000E004)

Bits	Name	Type	Reset Value	Description
4:0	INTLINESNUM	R	–	Number of interrupt inputs in step of 32 0 = 1 to 32 1 = 33 to 64 …

F.3.2 Auxiliary control register

Table F.25 Auxiliary Control Register (SCnSCB -> ACTLR, 0xE000E008) in the Cortex®-M3 Processor

Bits	Name	Type	Reset Value	Description
2	DISFOLD	R/W	0	Disable IT folding (Prevent overlap of IT instruction execution phase with following instruction)
1	DISDEFWBUF	R/W	0	Disable write buffer for default memory map (memory accesses in MPU mapped regions are not affected)
0	DISMCYCINT	R/W	0	Disable interruption of multiple cycle instructions like LDM, STM, 64-bit multiply and divide instructions.

In the Cortex®-M4 processor with floating point unit, the Auxiliary Control Register has additional bit fields, as shown in Table F.26:

Table F.26 Auxiliary Control Register (SCnSCB -> ACTLR, 0xE000E008) in the Cortex-M4 Processor with Floating Point Unit

Bits	Name	Type	Reset Value	Description
9	DISOOFP	R/W	0	Disable floating point instructions completing out of order with respect to integer instructions
8	DISFPCA	R/W	0	Disable automatic update of FPCA bit in the CONTROL register.
7:3	-	-	-	Reserved – Not used in current design.
2	DISFOLD	R/W	0	Disable IT folding (Prevent overlap of IT instruction execution phase with following instruction)
1	DISDEFWBUF	R/W	0	Disable write buffer for default memory map (memory accesses in MPU mapped regions are not affected)
0	DISMCYCINT	R/W	0	Disable interruption of multiple cycle instructions like LDM, STM, 64-bit multiply and divide instructions.

F.4 SYSTICK timer registers

F.4.1 SYSTICK control and status register

Table F.27 SYSTICK Control and Status Register (0xE000E010)

Bits	Name	Type	Reset Value	Description
16	COUNTFLAG	R	0	Read as 1 if counter reaches 0 since last time this register is read; clear to 0 automatically when read or when current counter value is cleared

(*Continued*)

Table F.27 SYSTICK Control and Status Register (0xE000E010)—Cont'd

Bits	Name	Type	Reset Value	Description
2	CLKSOURCE	R/W	0	0 = External reference clock (STCLK) 1 = Use core clock
1	TICKINT	R/W	0	1 = Enable SYSTICK interrupt generation when SYSTICK timer reaches 0 0 = Do not generate interrupt
0	ENABLE	R/W	0	SYSTICK timer enable

F.4.2 SYSTICK reload value register

Table F.28 SYSTICK Reload Value Register (SysTick->LOAD, 0xE000E014)

Bits	Name	Type	Reset Value	Description
23:0	RELOAD	R/W	0	Reload value when timer reaches 0

F.4.3 SYSTICK current value register

Table F.29 SYSTICK Current Value Register (SysTick->VAL,0xE000E018)

Bits	Name	Type	Reset Value	Description
23:0	CURRENT	R/Wc	0	Read to return current value of the timer. Write to clear counter to 0. Clearing of current value also clears COUNTFLAG in SYSTICK Control and Status Register

F.4.4 SYSTICK calibration value register

Table F.30 SYSTICK Calibration Value Register (SysTick->CALIB,0xE000E01C)

Bits	Name	Type	Reset Value	Description
31	NOREF	R	–	1 = No external reference clock (STCLK not available) 0 = External reference clock available
30	SKEW	R	–	1 = Calibration value is not exactly 10 ms 0 = Calibration value is accurate
23:0	TENMS	R	0	Calibration value for 10 ms; chip designer should provide this value via Cortex-M3/M4 input signals. If this value is read as 0, calibration value is not available

F.5 Memory protection unit

F.5.1 MPU type register

Table F.31 MPU Type Register (MPU->TYPE, 0xE000ED90)

Bits	Name	Type	Reset Value	Description
23:16	IREGION	R	0	Number of instruction regions supported by this MPU; because ARMv7-M architecture uses a unified MPU, this is always 0
15:8	DREGION	R	0 or 8	Number of regions supported by this MPU; in the Cortex-M3 or Cortex-M4 this is either 0 (MPU not present) or 8 (MPU present)
0	SEPARATE	R	0	This is always 0 as the MPU is unified

F.5.2 MPU control register

Table F.32 MPU Control Register (MPU->CTRL, 0xE000ED94)

Bits	Name	Type	Reset Value	Description
2	PRIVDEFENA	R/W	0	Privileged default memory map enable. When set to 1 and if the MPU is enabled, the default memory map will be used for privileged accesses as a background region. If this bit is not set, the background region is disabled and any access not covered by any enabled region will cause a fault.
1	HFNMIENA	R/W	0	If set to 1, it enables the MPU during the HardFault handler and NMI handler; otherwise, the MPU is not enabled for the HardFault handler and NMI.
0	ENABLE	R/W	0	Enables the MPU if set to 1.

F.5.3 MPU region number register

Table F.33 MPU Region Number Register (MPU->RNR, 0xE000ED98)

Bits	Name	Type	Reset Value	Description
7:0	REGION	R/W	—	Select the region that is being programmed. Since eight regions are supported in the MPU, only bit[2:0] of this register is implemented.

F.5.4 MPU region base address register

Table F.34 MPU Region Base Address Register (MPU->RBAR, 0xE000ED9C)

Bits	Name	Type	Reset Value	Description
31:N	ADDR	R/W	—	Base address of the region; N is dependent on the region size – for example, a 64 k size region will have a base address field of [31:16].
4	VALID	R/W	—	If this is 1, the REGION defined in bit[3:0] will be used in this programming step; otherwise, the region selected by the MPU Region Number register is used.
3:0	REGION	R/W	—	This field overrides the MPU Region Number register if VALID is 1; otherwise it is ignored. Since eight regions are supported in the Cortex-M3/M4 MPU, the region number override is ignored if the value of the REGION field is larger than 7.

F.5.5 MPU region base attribute and size register

Table F.35 MPU Region Base Attribute and Size Register (MPU->RASR, 0xE000EDA0)

Bits	Name	Type	Reset Value	Description
31:29	Reserved	—	—	—
28	XN	R/W	—	Instruction Access Disable (1 = Disable instruction fetch from this region; an attempt to do so will result in a memory management fault)
27	Reserved	—	—	—
26:24	AP	R/W	—	Data Access Permission field (see Table 11.8)
23:22	Reserved	—	—	—
21:19	TEX	R/W	—	Type Extension field (see Table 11.9)

(*Continued*)

Table F.35 MPU Region Base Attribute and Size Register (MPU->RASR, 0xE000EDA0)—Cont'd

Bits	Name	Type	Reset Value	Description
18	S	R/W	—	Shareable (see Table 11.9)
17	C	R/W	—	Cacheable (see Table 11.9)
16	B	R/W	—	Bufferable (see Table 11.9)
15:8	SRD	R/W	—	Sub-region disable
7:6	Reserved	—	—	—
5:1	REGION SIZE	R/W	—	MPU Protection Region size (see Table 11.7)
0	ENABLE	R/W	—	Region enable

F.5.6 MPU Alias registers

Table F.35 MPU Alias Registers

Address	Register	CMSIS-Core Symbol	Function
0xE000EDA4	MPU Alias 1 Region Base Address Register	MPU->RBAR_A1	Alias of MPU->RBAR
0xE000EDA8	MPU Alias 1 Region Base Attribute and Size Register	MPU->RASR_A1	Alias of MPU->RASR
0xE000EDAC	MPU Alias 2 Region Base Address Register	MPU->RBAR_A2	Alias of MPU->RBAR
0xE000EDB0	MPU Alias 2 Region Base Attribute and Size Register	MPU->RASR_A2	Alias of MPU->RASR
0xE000EDB4	MPU Alias 3 Region Base Address Register	MPU->RBAR_A3	Alias of MPU->RBAR
0xE000EDB8	MPU Alias 3 Region Base Attribute and Size Register	MPU->RASR_A3	Alias of MPU->RASR

F.6 Floating point unit

F.6.1 Floating point context control register

Table F.36 Floating Point Context Control Register (FPU->FPCCR, 0xE000EF34)

Bits	Name	Type	Reset Value	Descriptions
31	ASPEN	R/W	1	Enable/disable automatic setting of FPCA (bit 2 of the CONTROL register). When this is set (default), it enables the automatic state preservation and restoration of S0–S15 & FPSCR on exception entry and exception exit. When it is clear to 0, automatic saving of FPU registers are disabled. Software using FPU might need to manage context saving manually.
30	LSPEN	R/W	1	Enable/disable lazy stacking (state preservation) for S0–S15 & FPSCR. When this is set (default), the exception sequence use lazy stacking feature to ensure low interrupt latency.
29:9	-	-	-	Reserved
8	MONRDY		0	0 = DebugMonitor is disabled or priority did not permit setting MON_PEND when the floating-point stack frame was allocated. 1 = DebugMonitor is enabled and priority permits setting MON_PEND when the floating-point stack frame was allocated.
7	-	-	-	Reserved
6	BFRDY	R?	0	0 = BusFault is disabled or priority did not permit setting the BusFault handler to the pending state when the floating-point stack frame was allocated. 1 = BusFault is enabled and priority permitted setting the BusFault handler to the pending state when the floating-point stack frame was allocated.

(*Continued*)

Table F.36 Floating Point Context Control Register (FPU->FPCCR, 0xE000EF34)—Cont'd

Bits	Name	Type	Reset Value	Descriptions
5	MMRDY	R?	0	0 = MemManage is disabled or priority did not permit setting the MemManage handler to the pending state when the floating-point stack frame was allocated. 1 = MemManage is enabled and priority permitted setting the MemManage handler to the pending state when the floating-point stack frame was allocated.
4	HFRDY	R?	0	0 = Priority did not permit setting the HardFault handler to the pending state when the floating-point stack frame was allocated. 1 = Priority permitted setting the HardFault handler to the pending state when the floating-point stack frame was allocated.
3	THREAD	R?	0	0 = Mode was not Thread Mode when the floating-point stack frame was allocated. 1 = Mode was Thread Mode when the floating-point stack frame was allocated.
2	-	-	-	Reserved
1	USER	R?	00	0 = Mode was not Thread Mode when the floating-point stack frame was allocated. 1 = Mode was Thread Mode when the floating-point stack frame was allocated.
0	LSPACT	R?	0	0 = Lazy state preservation is not active. 1 = Lazy state preservation is active. Floating-point stack frame has been allocated but saving state to it has been deferred.

F.6.2 Floating point context address register

Table F.37 Floating Point Context Address Register (FPU->FPCAR, 0xE000EF38)

Bits	Name	Type	Reset Value	Descriptions
31:3	ADDRESS	R/W	-	The location of the unpopulated floating-point register space allocated on an exception stack frame.
2:0	Reserved	-	-	Always 0

F.6.3 Floating point default status control register

Table F.38 Floating Point Default Status Control Register (FPU->FPDSCR, 0xE000EF3C)

Bits	Name	Type	Reset Value	Descriptions
31:27	Reserved	-	-	-
26	AHP	R/W	0	Default value for FPSCR.AHP – alternate half precision (see Table 13.4)
25	DN	R/W	0	Default value for FPSCR.DN – default NaN (see Table 13.4)
24	FZ	R/W	0	Default value for FPSCR.FZ – Flush to zero (see Table 13.4)
23:22	RMode	R/W	0	Default value for FPSCR.RMode – Rounding mode (see Table 13.4)
21:0	Reserved	-	-	-

F.7 SCS Peripheral and Component ID Registers

Table F.39 Peripheral ID and Component ID Registers of the System Control Space

Address	Name	Type	Reset Value	Descriptions
0xE000EFD0	PERIPHID4	R	0x04	Peripheral ID register
0xE000EFD4	PERIPHID5	R	0x00	Peripheral ID register
0xE000EFD8	PERIPHID6	R	0x00	Peripheral ID register
0xE000EFDC	PERIPHID7	R	0x00	Peripheral ID register
0xE000EFE0	PERIPHID0	R	0x00 (no FPU)/0x0C (if FPU is present)	Peripheral ID register
0xE000EFE4	PERIPHID1	R	0xB0	Peripheral ID register
0xE000EFE8	PERIPHID2	R	0x-B	Peripheral ID register
0xE000EFEC	PERIPHID3	R	0x00	Peripheral ID register
0xE000EFF0	PCELLID0	R	0x0D	Component ID register
0xE000EFF4	PCELLID1	R	0xE0	Component ID register
0xE000EFF8	PCELLID2	R	0x05	Component ID register
0xE000EFFC	PCELLID0	R	0xB1	Component ID register