Memory Systems

CH008

Figure 8.1 The memory interface

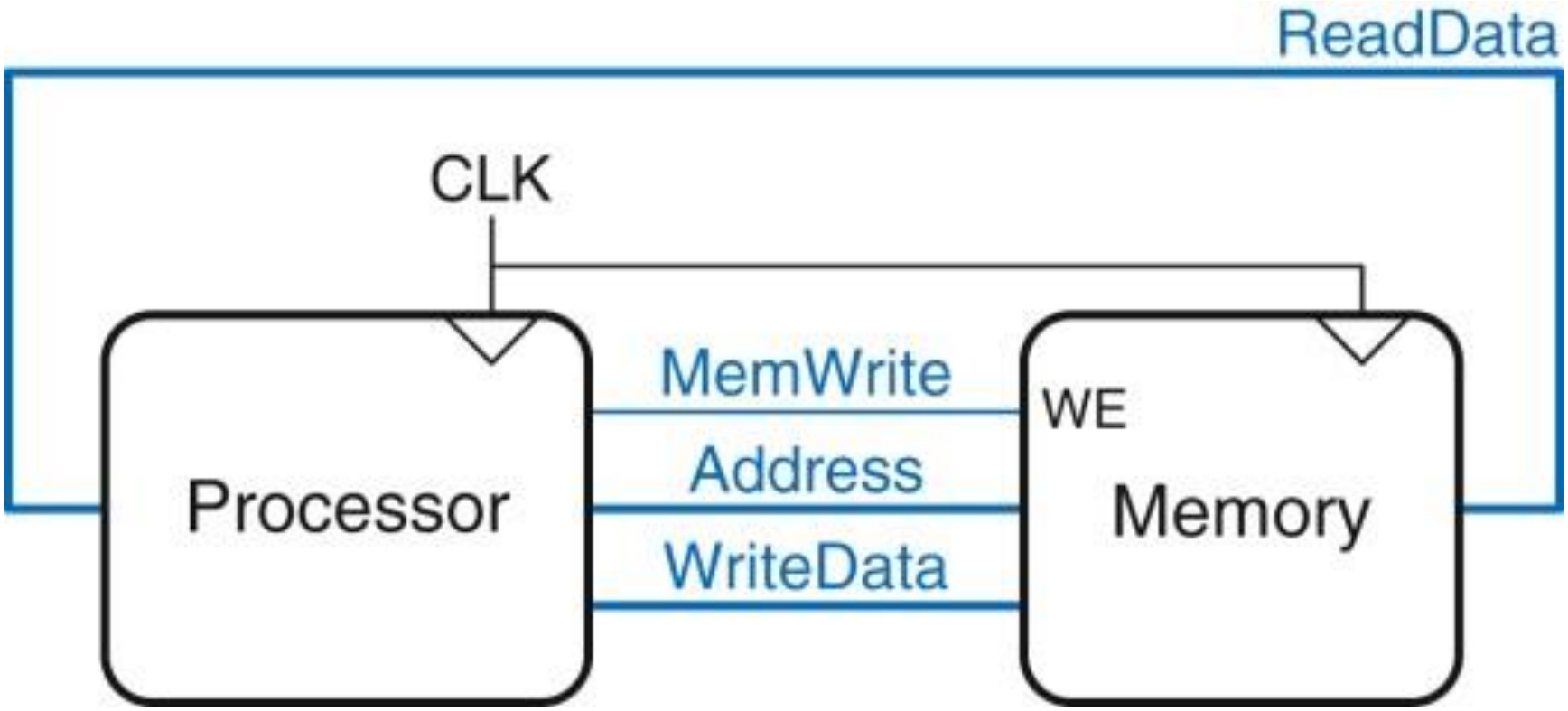


Figure 8.2 Diverging processor and memory performance.
Adapted with permission from Hennessy and Patterson, *Computer Architecture: A Quantitative Approach*, 5th ed., Morgan Kaufmann, 2011.

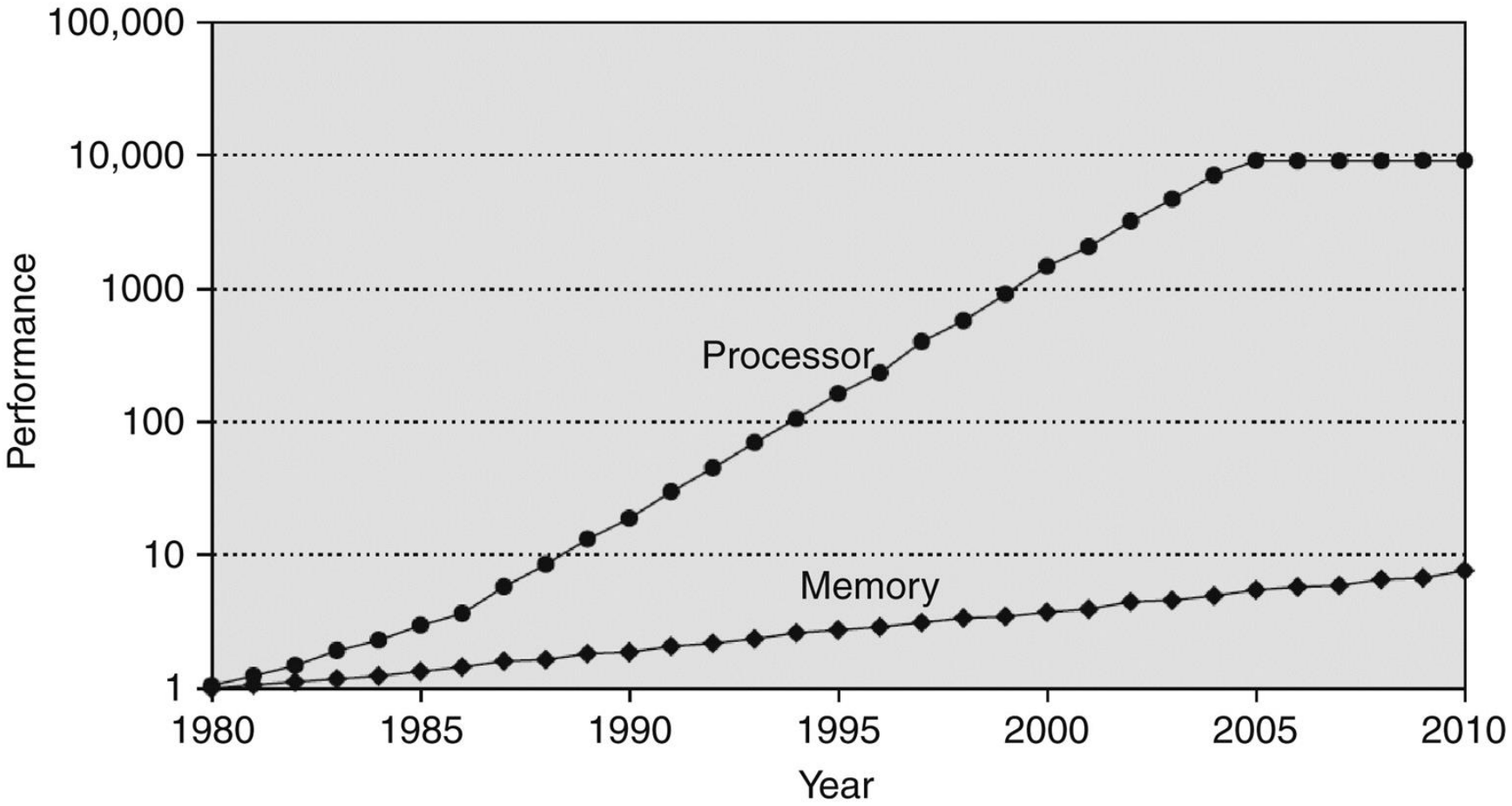


Figure 8.3 A typical memory hierarchy

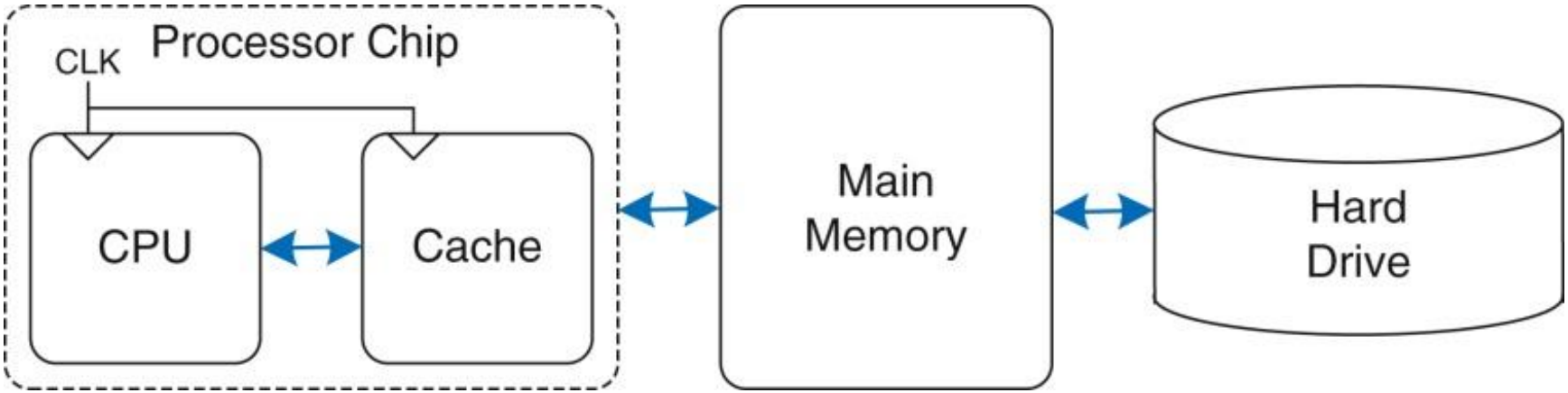
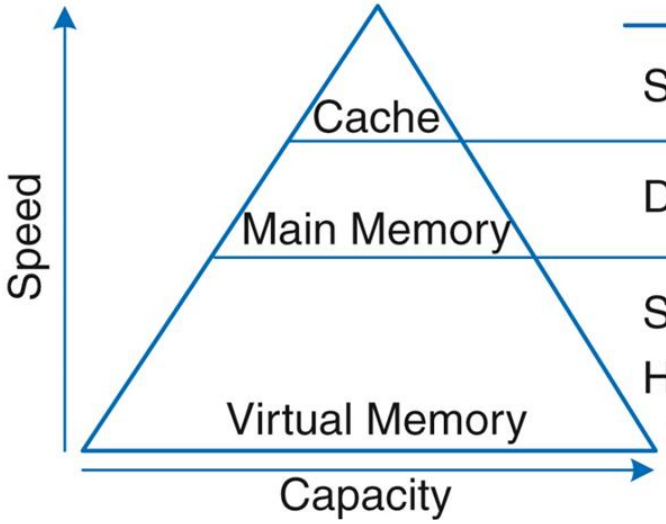


Figure 8.4 Memory hierarchy components, with typical characteristics in 2015



Technology	Price / GB	Access Time (ns)	Bandwidth (GB/s)
SRAM	$5,000	0.5	25+
DRAM	$7	10–50	10
SSD	$0.40	20,000	0.5
HDD	$0.05	5,000,000	0.75

Figure 8.5 Mapping of main memory to a direct mapped cache

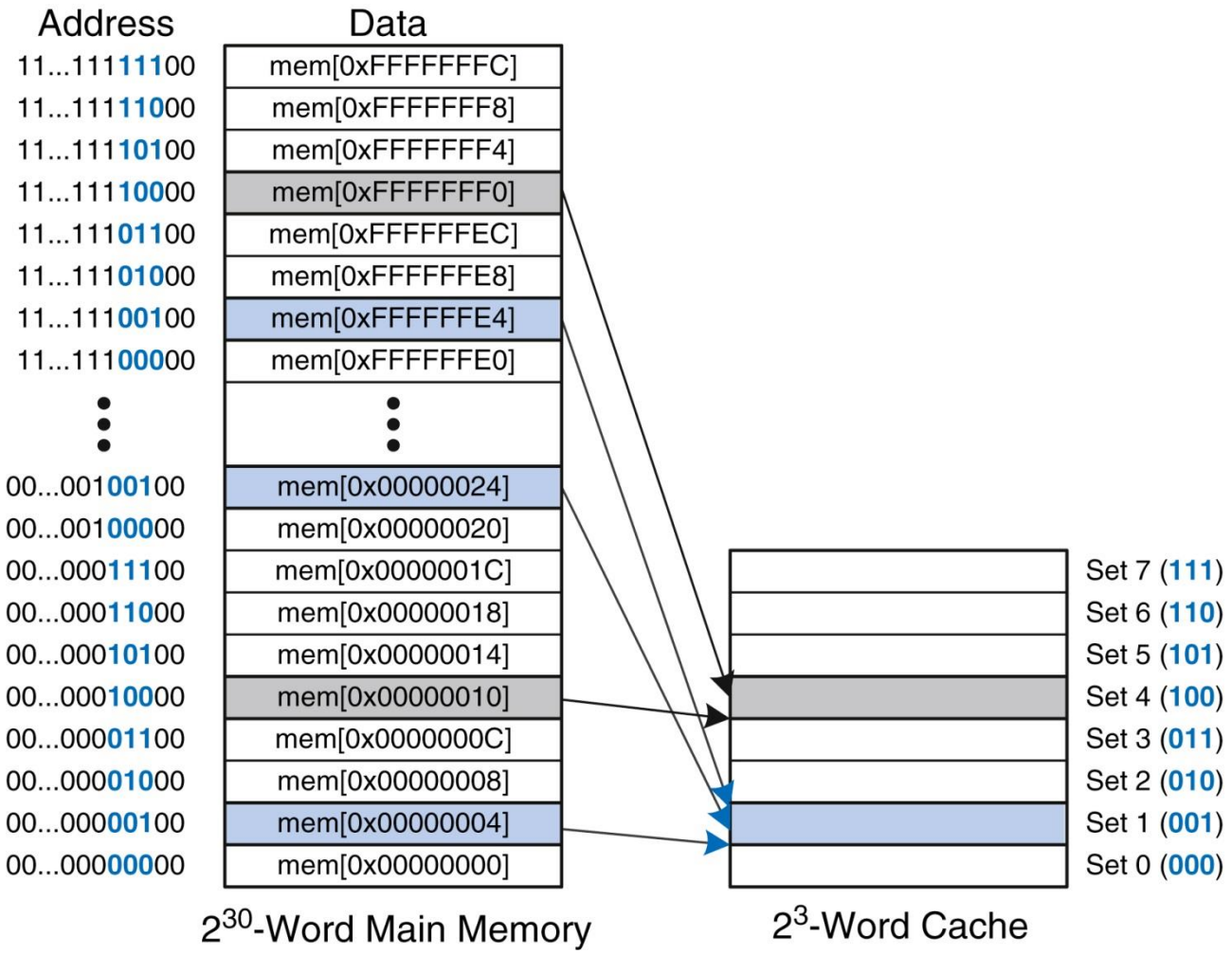


Figure 8.6 Cache fields for address 0xFFFFFFE4 when mapping to the cache in Figure 8.5

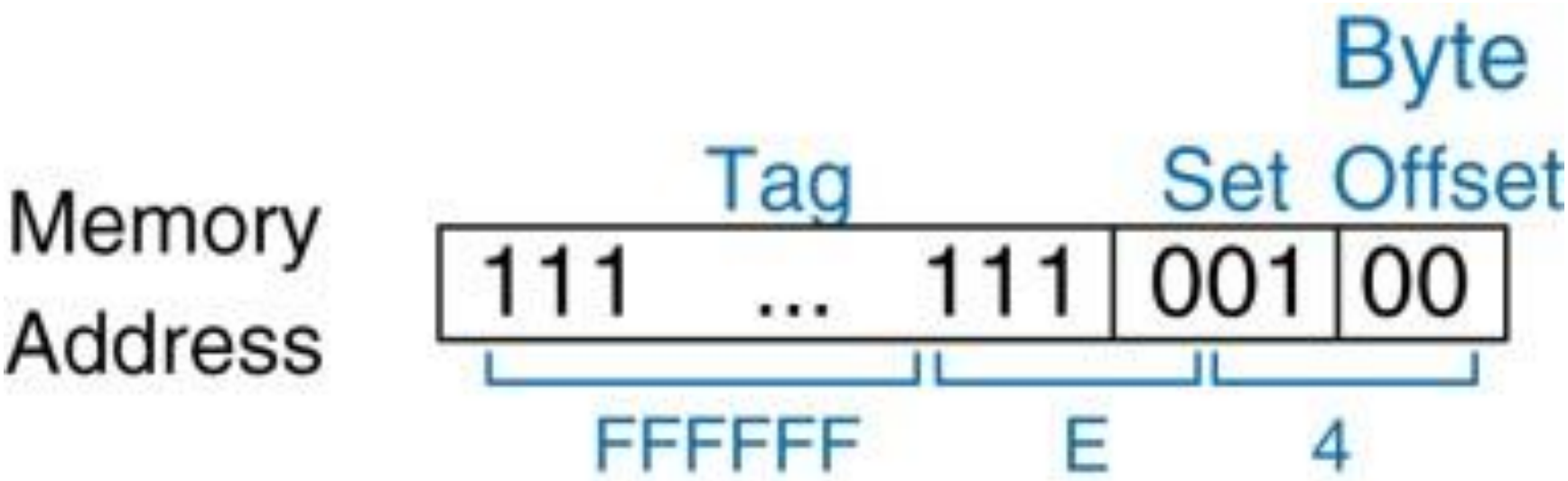


Figure 8.7 Direct mapped cache with 8 sets

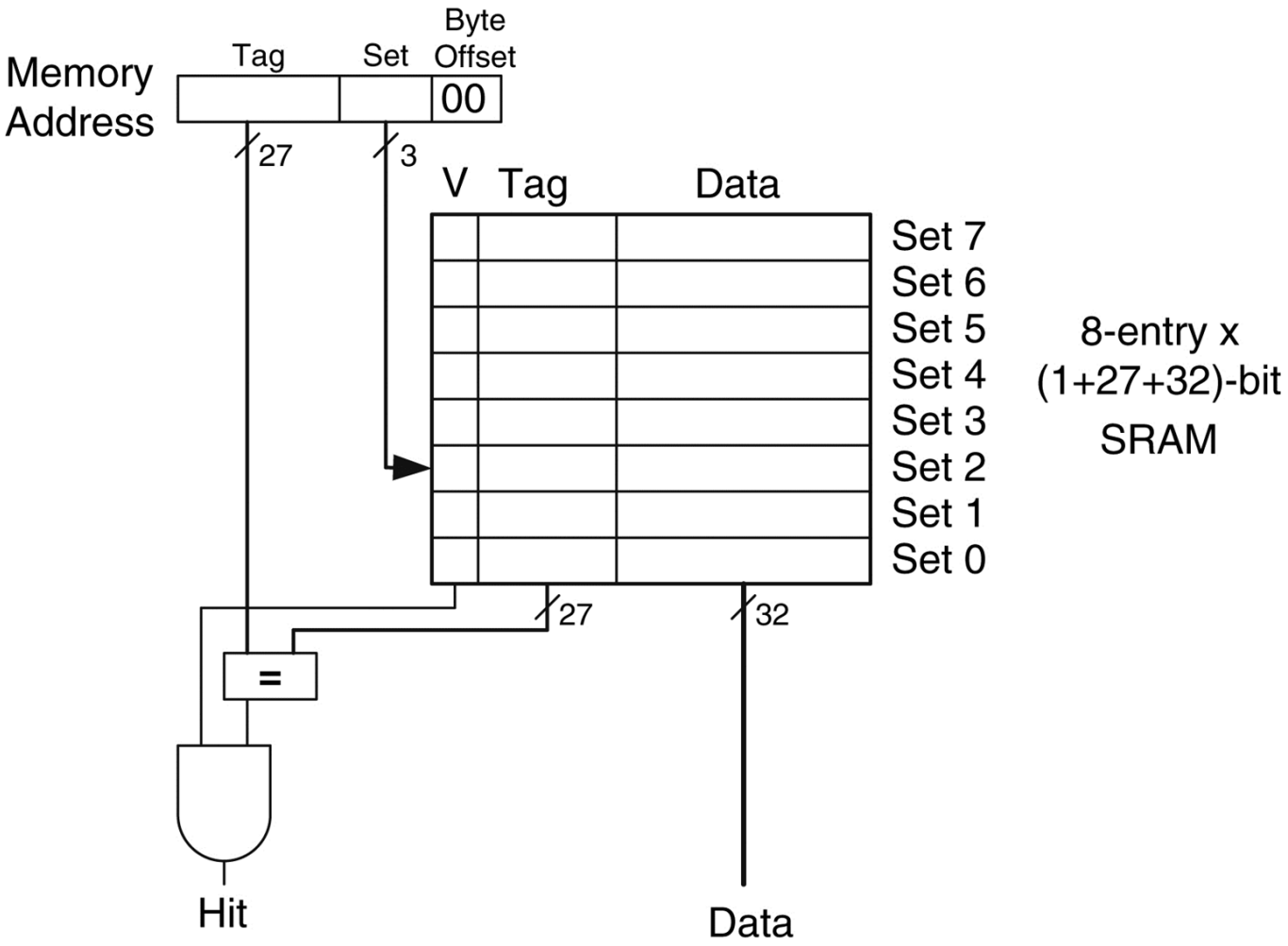


Figure 8.8 Direct mapped cache contents

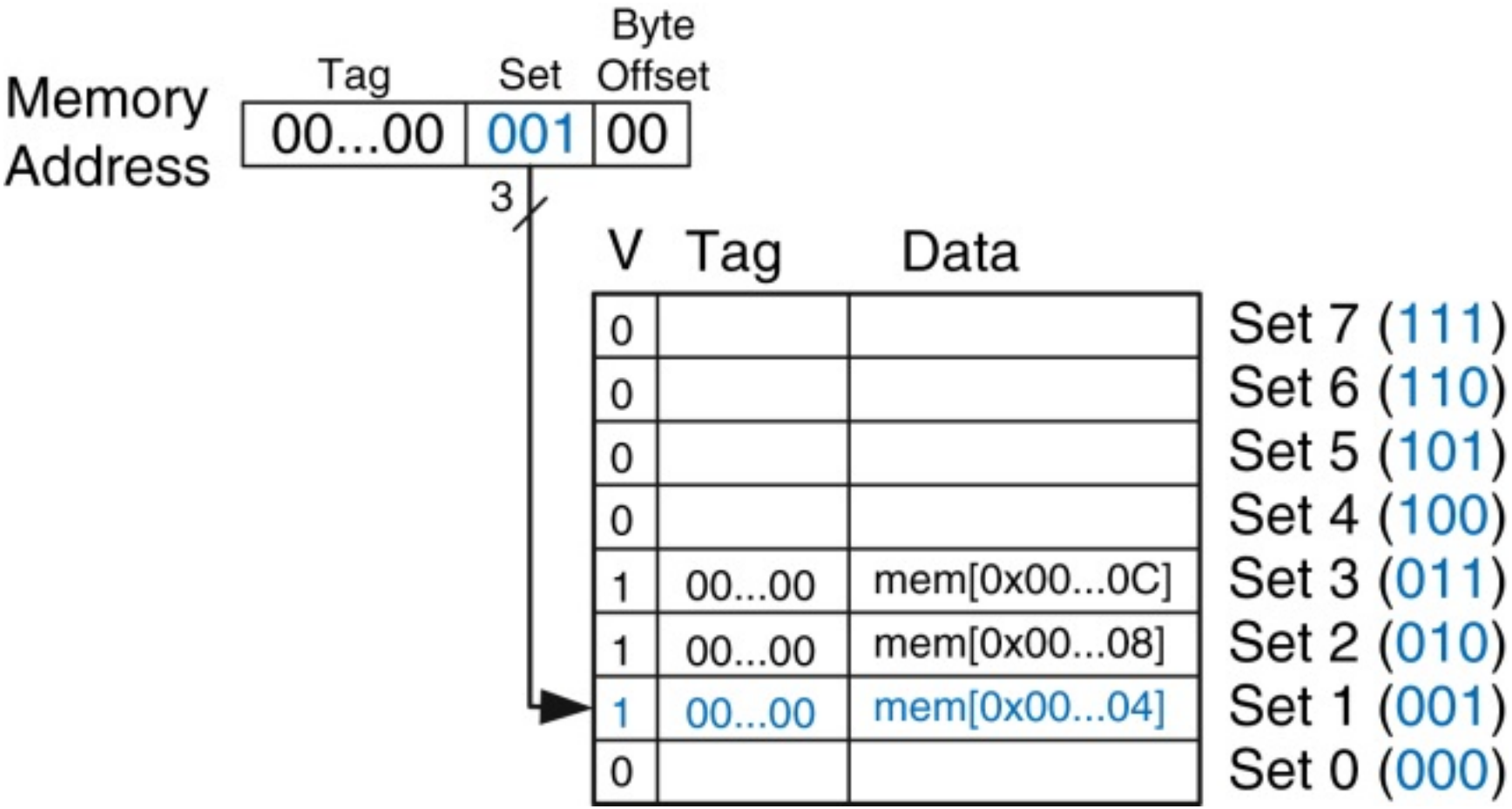


Figure 8.9 Two-way set associative cache

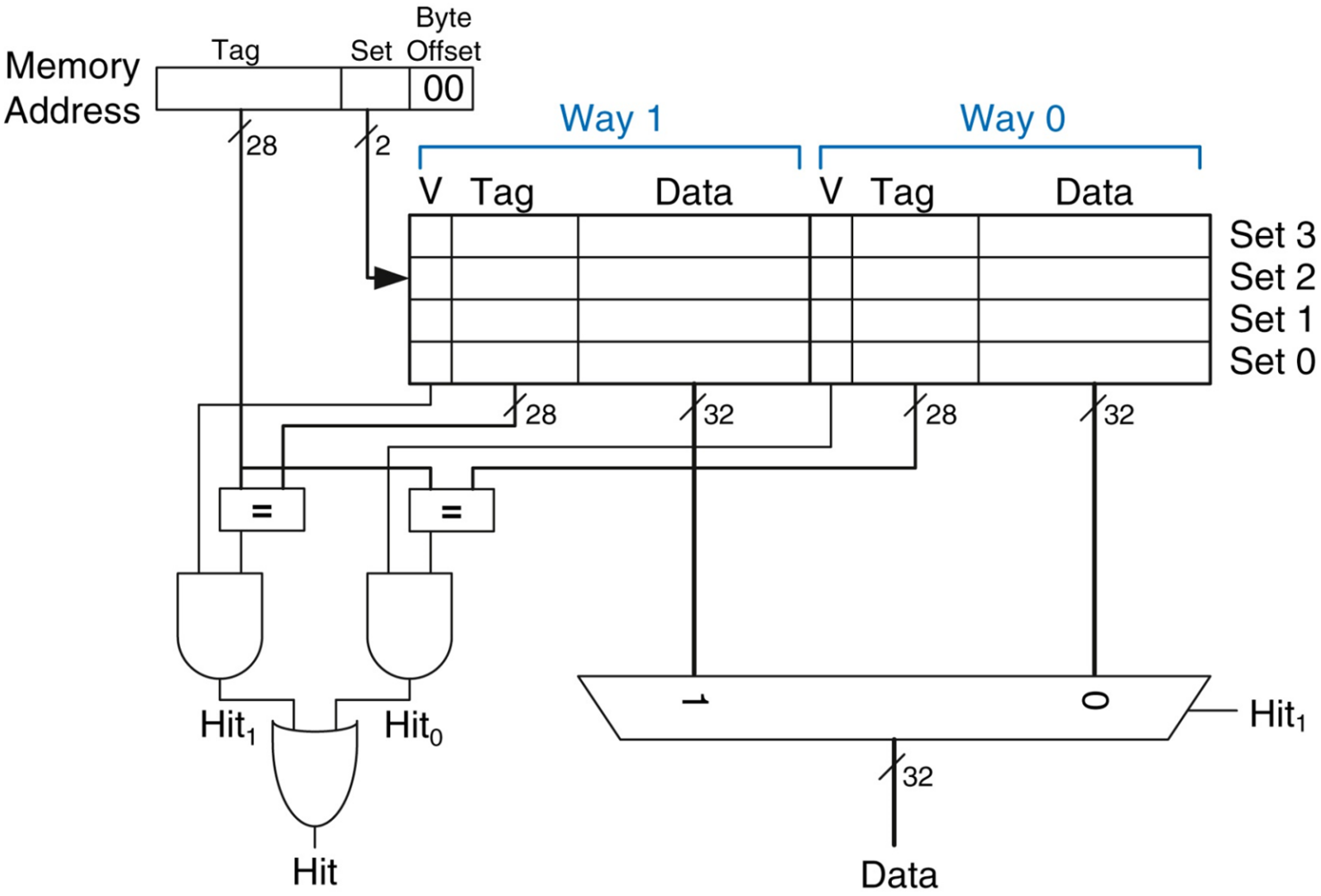


Figure 8.10 Two-way set associative cache contents

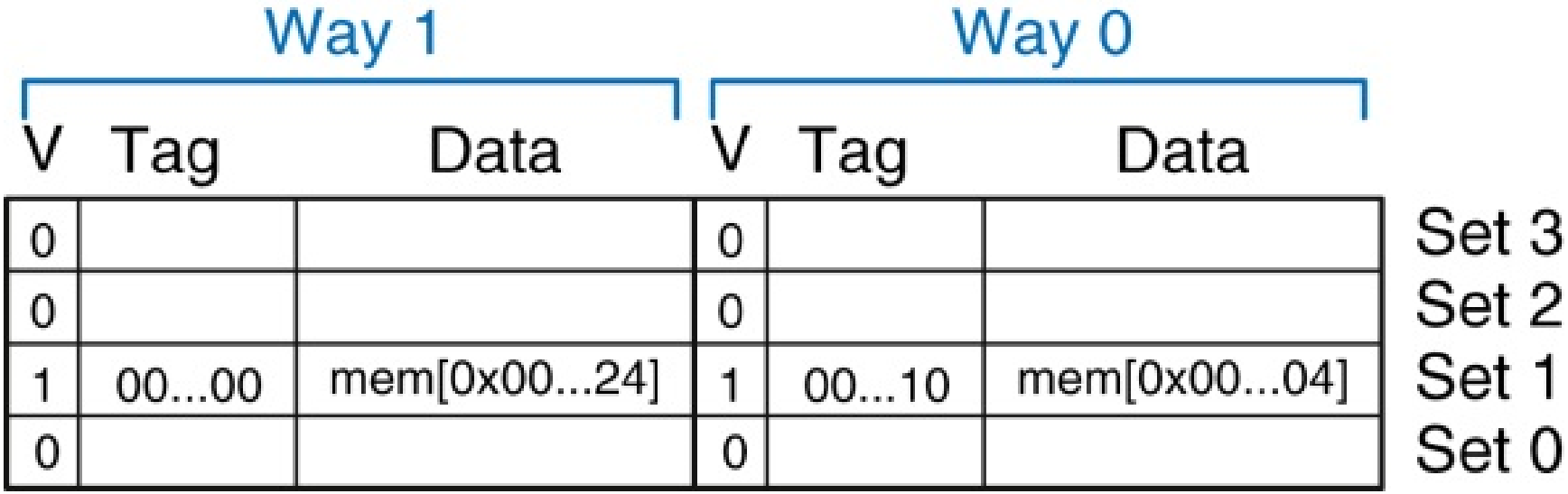


Figure 8.11 Eight-block fully associative cache

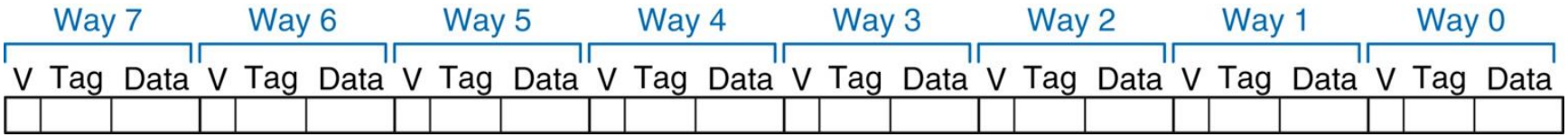


Figure 8.12 Direct mapped cache with two sets and a four-word block size

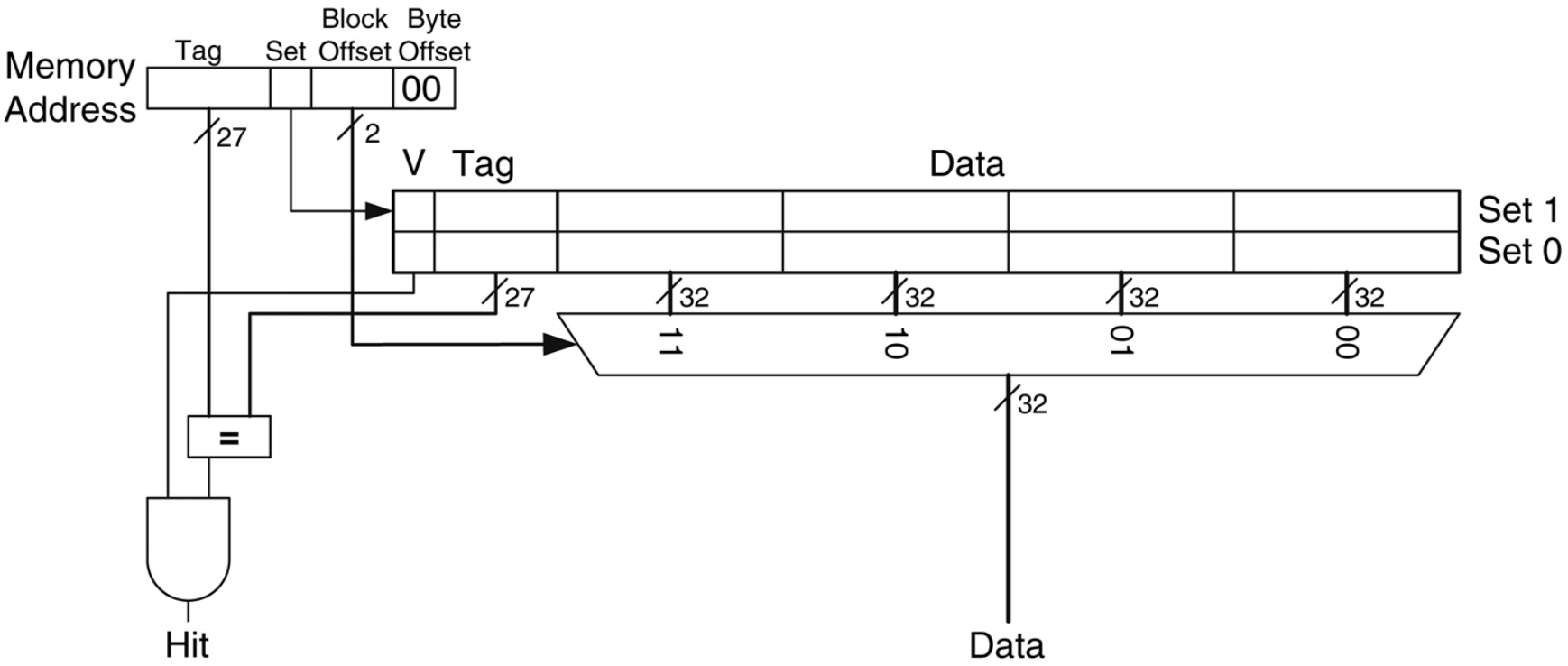


Figure 8.13 Cache fields for address 0x8000009C when mapping to the cache of Figure 8.12

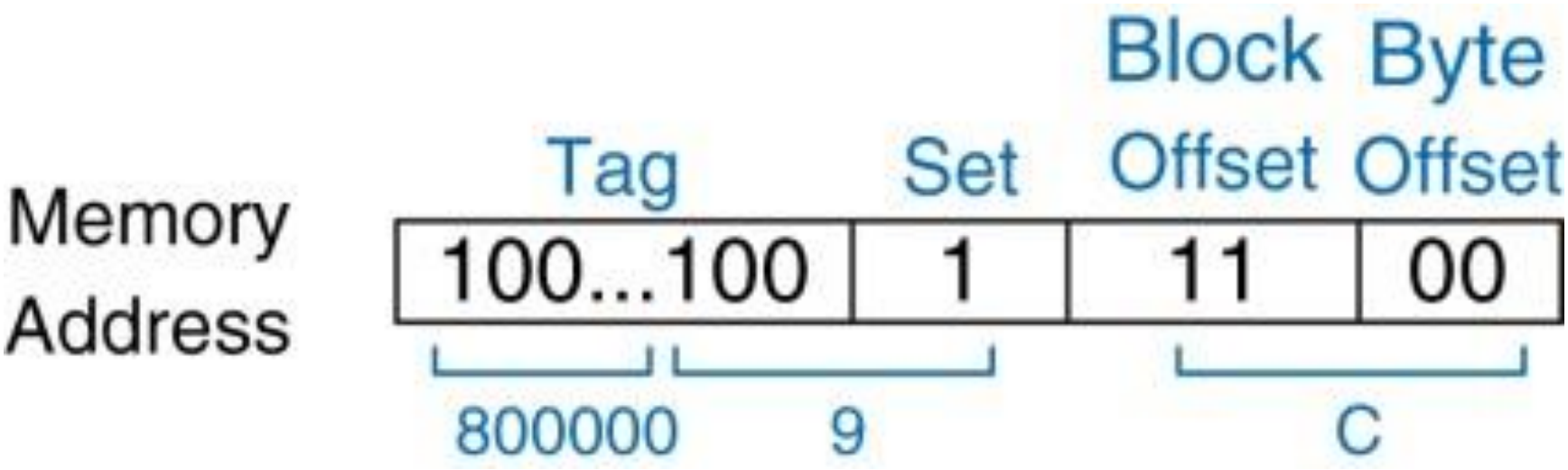


Figure 8.14 Cache contents with a block size *b* of four words

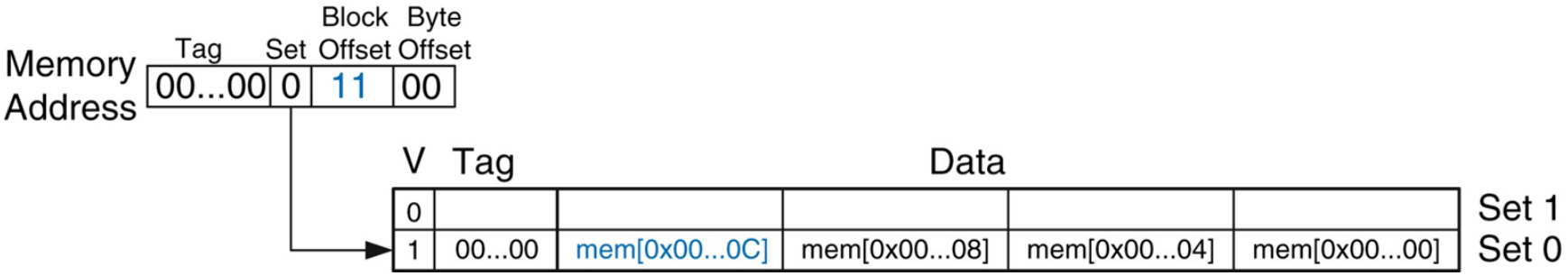


Figure 8.15 Two-way associative cache with LRU replacement

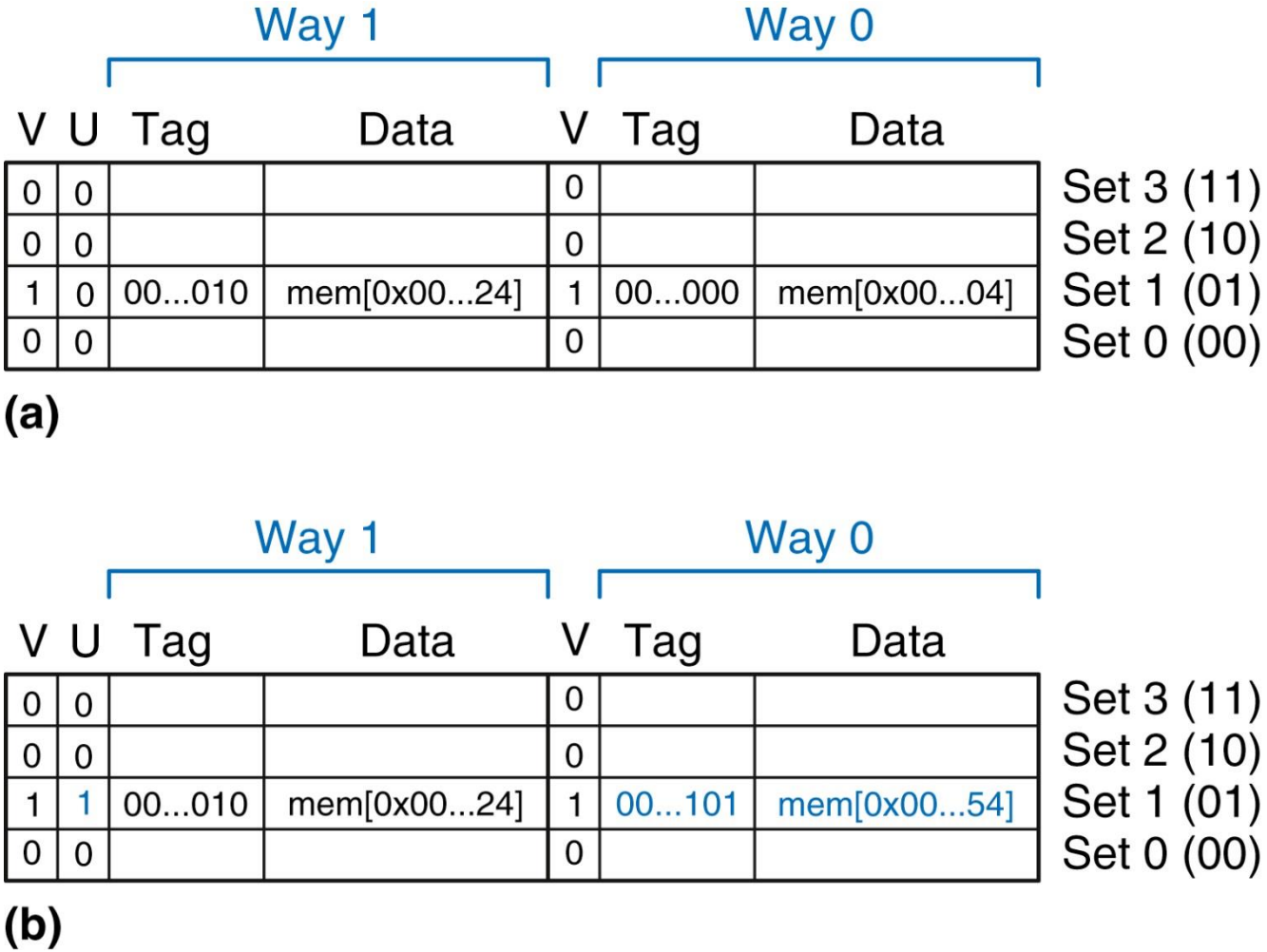


Figure 8.16 Memory hierarchy with two levels of cache

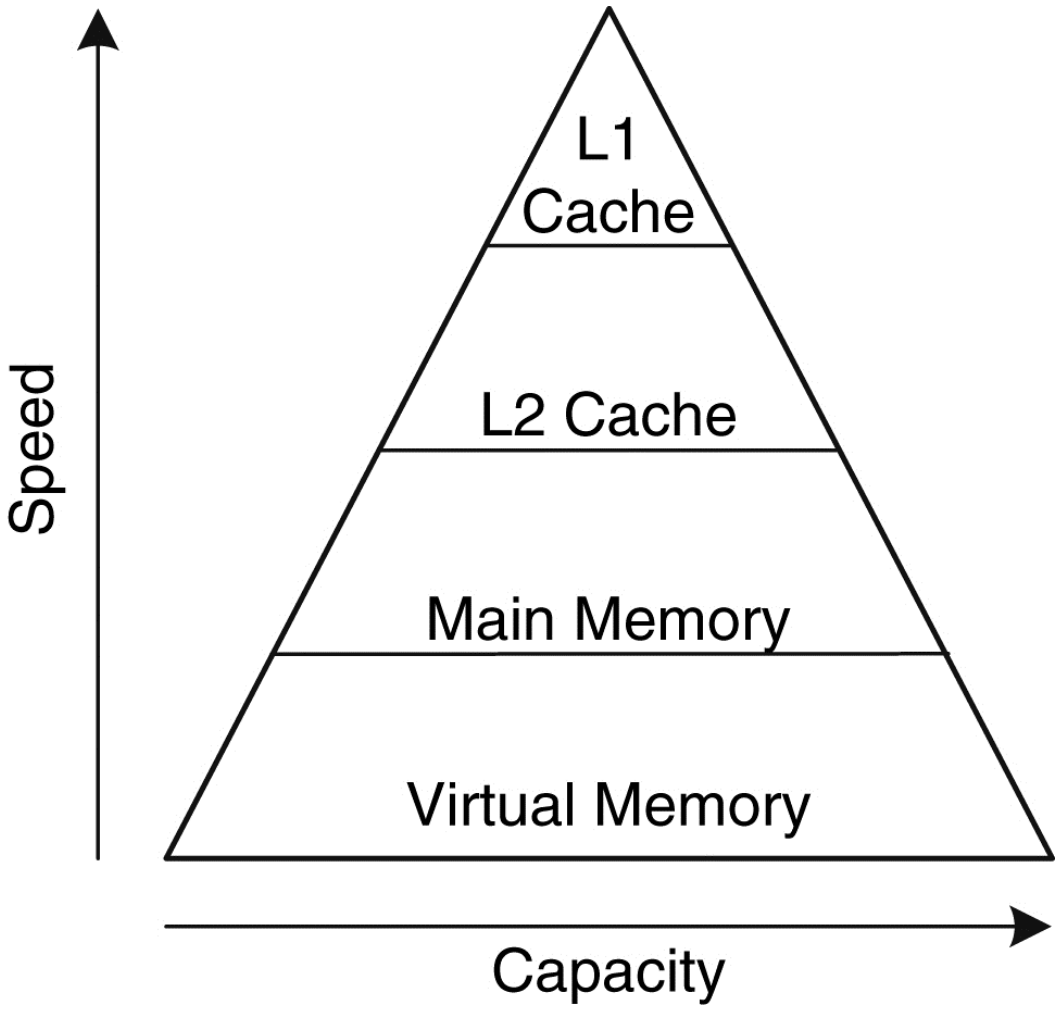


Figure 8.17 Miss rate versus cache size and associativity on SPEC2000 benchmark. (Adapted with permission from Hennessy and Patterson, *Computer Architecture: A Quantitative Approach*, 5th ed., Morgan Kaufmann, 2012.)

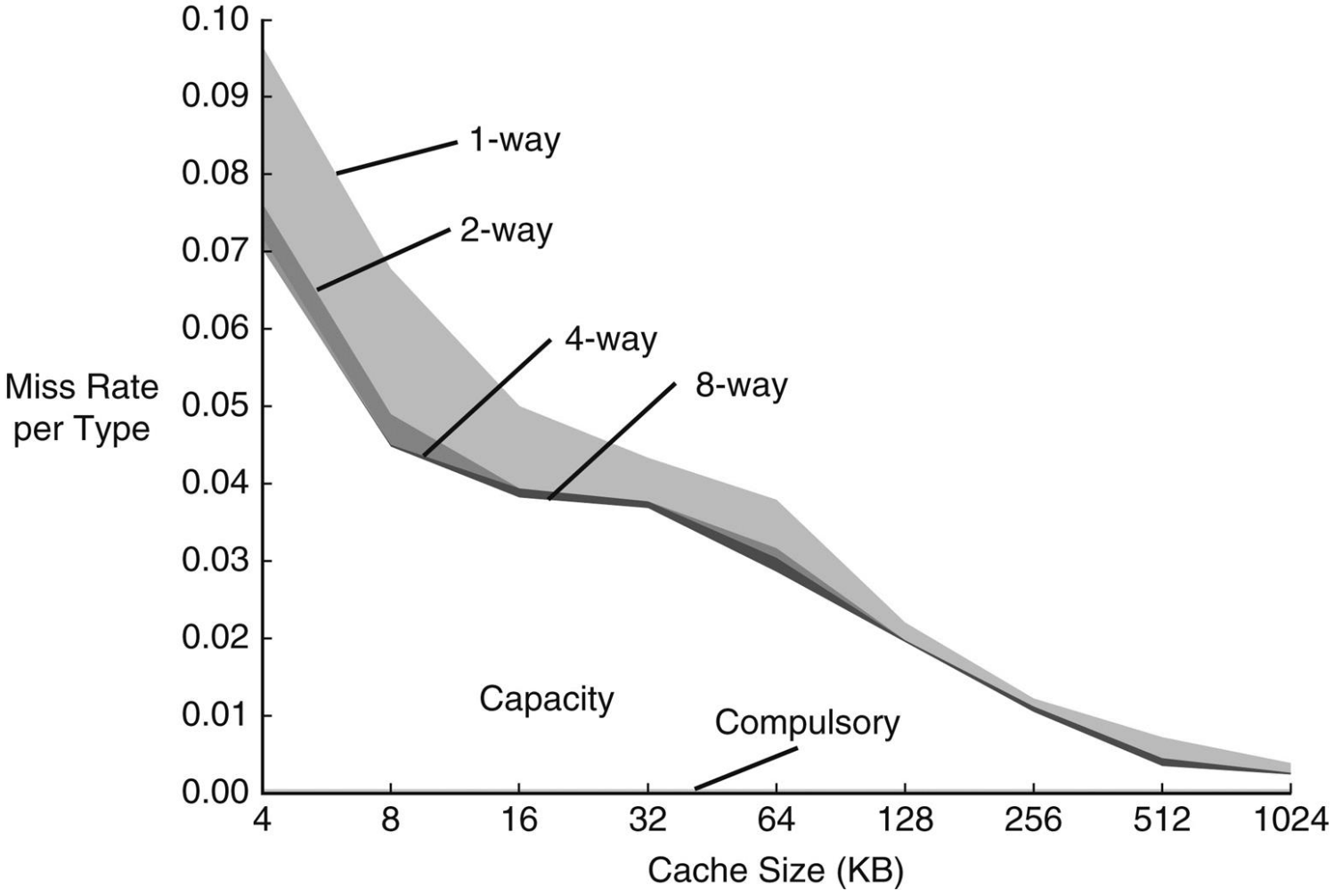


Figure 8.18 Miss rate versus block size and cache size on SPEC92 benchmark. (Adapted with permission from Hennessy and Patterson, *Computer Architecture: A Quantitative Approach*, 5th ed., Morgan Kaufmann, 2012.)

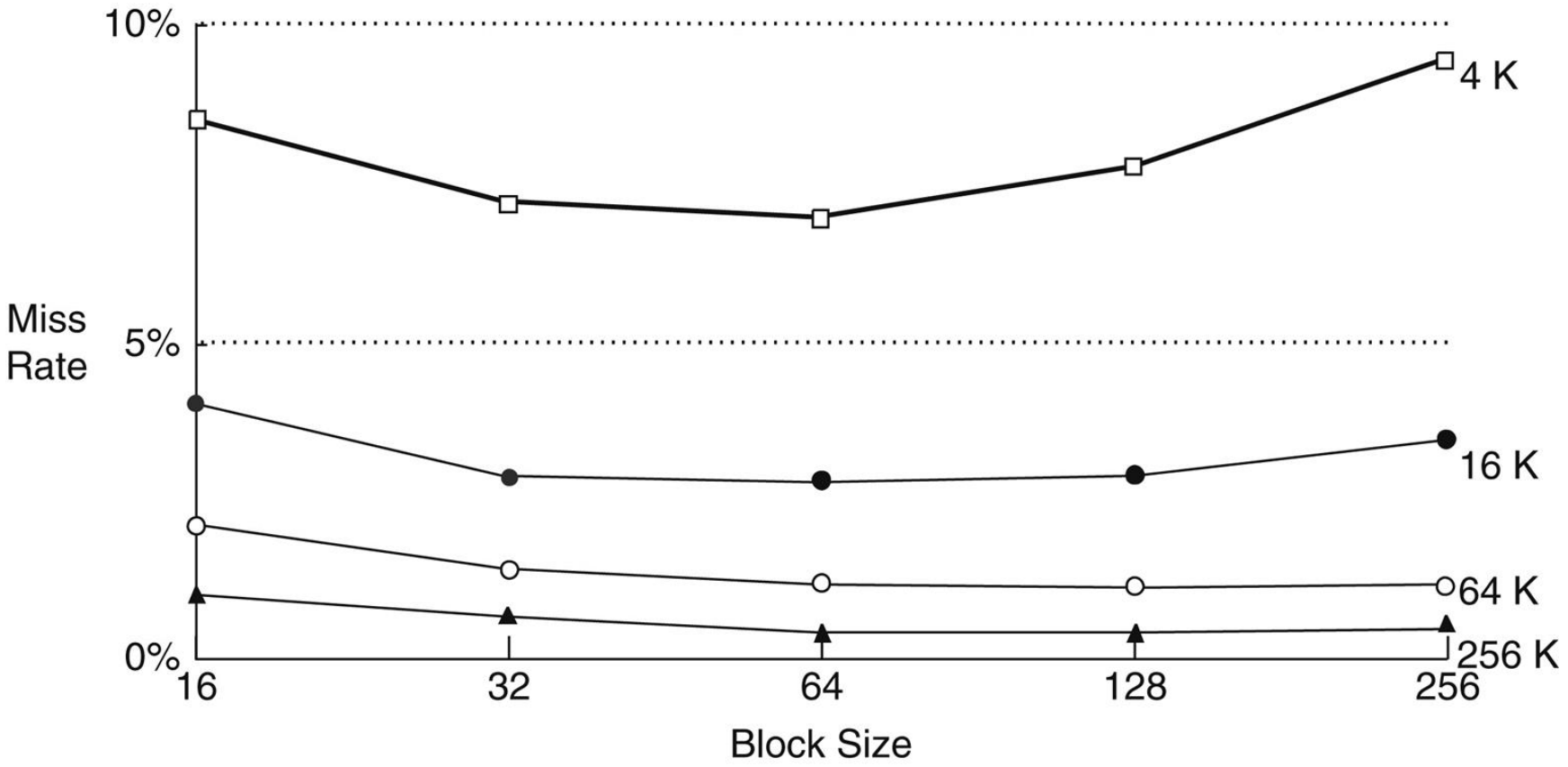


Figure 8.19 Hard disk

Figure 8.20 Virtual and physical pages

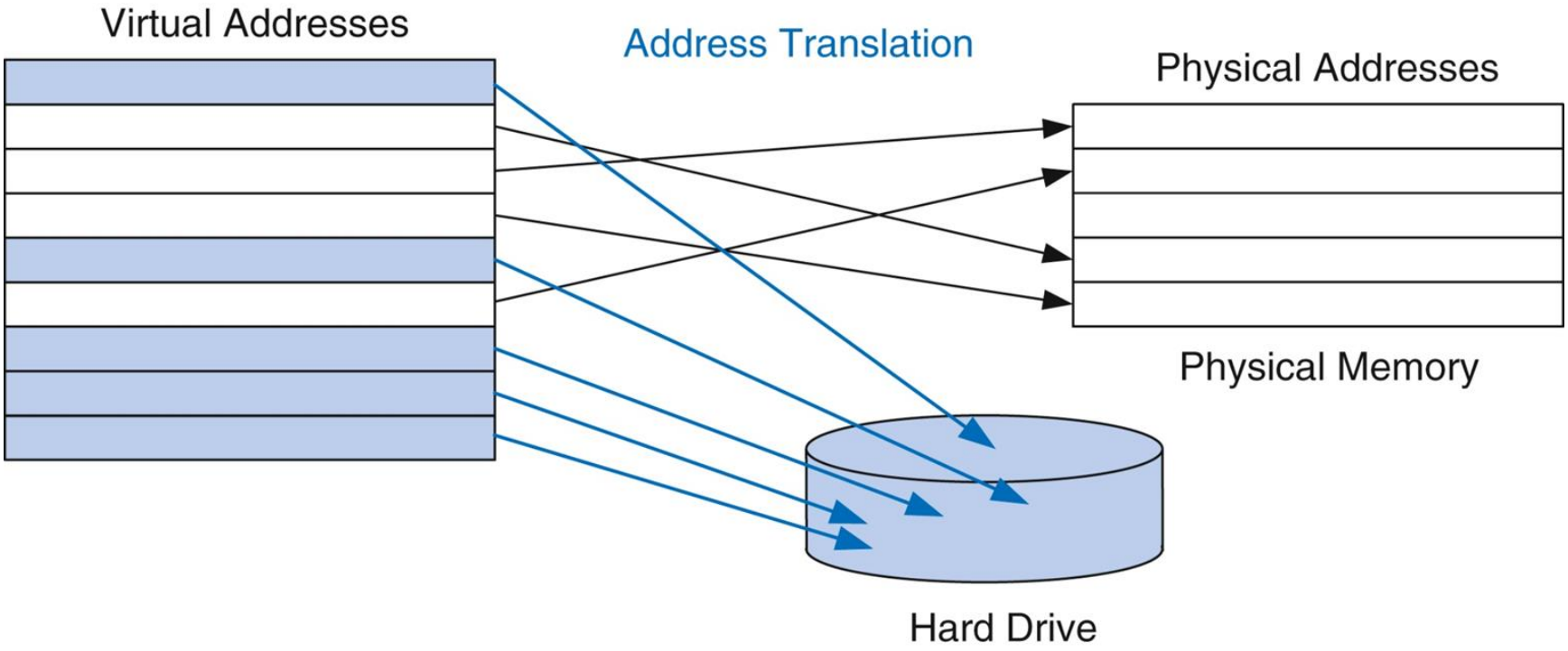


Figure 8.21 Physical and virtual pages

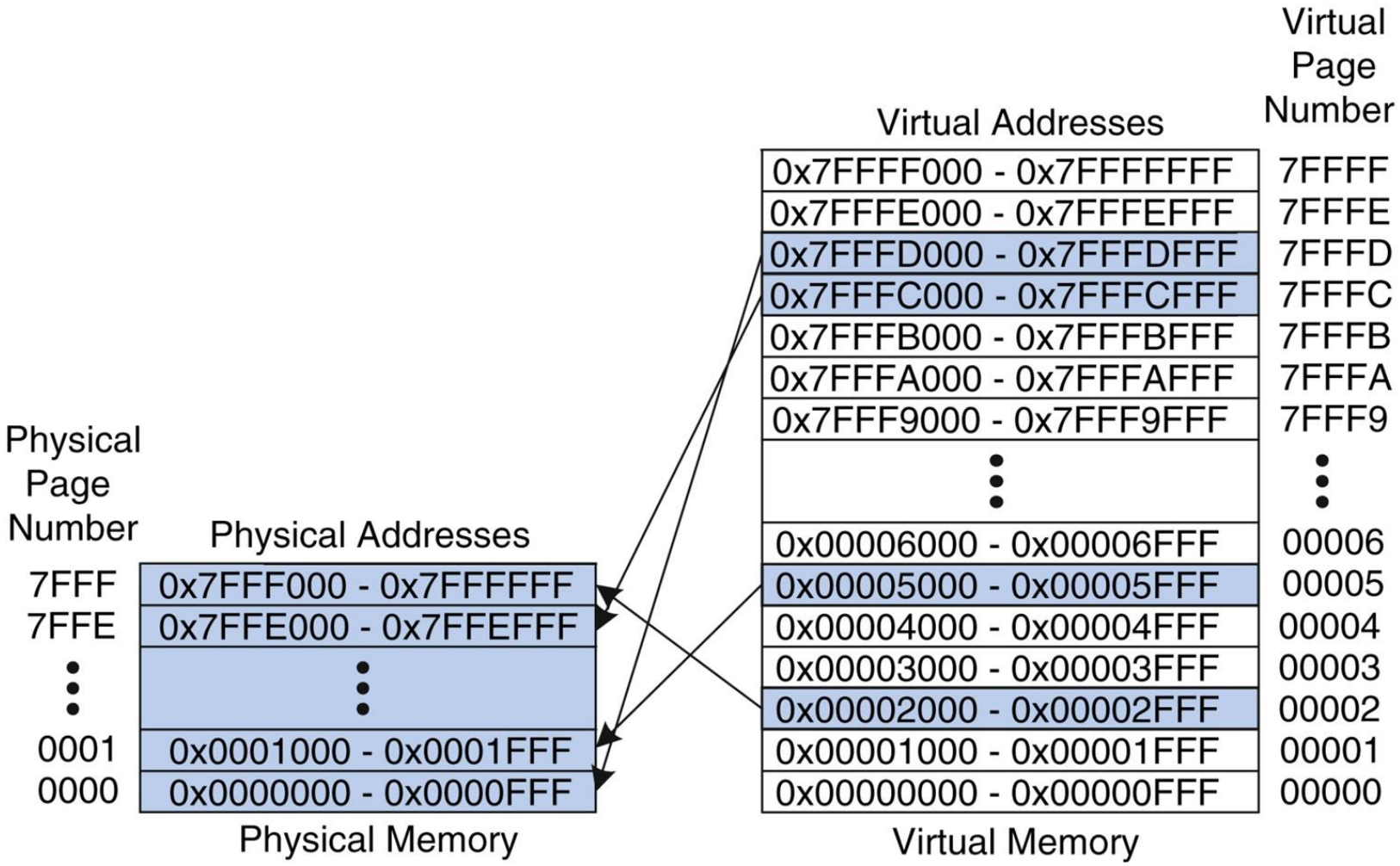


Figure 8.22 Translation from virtual address to physical address

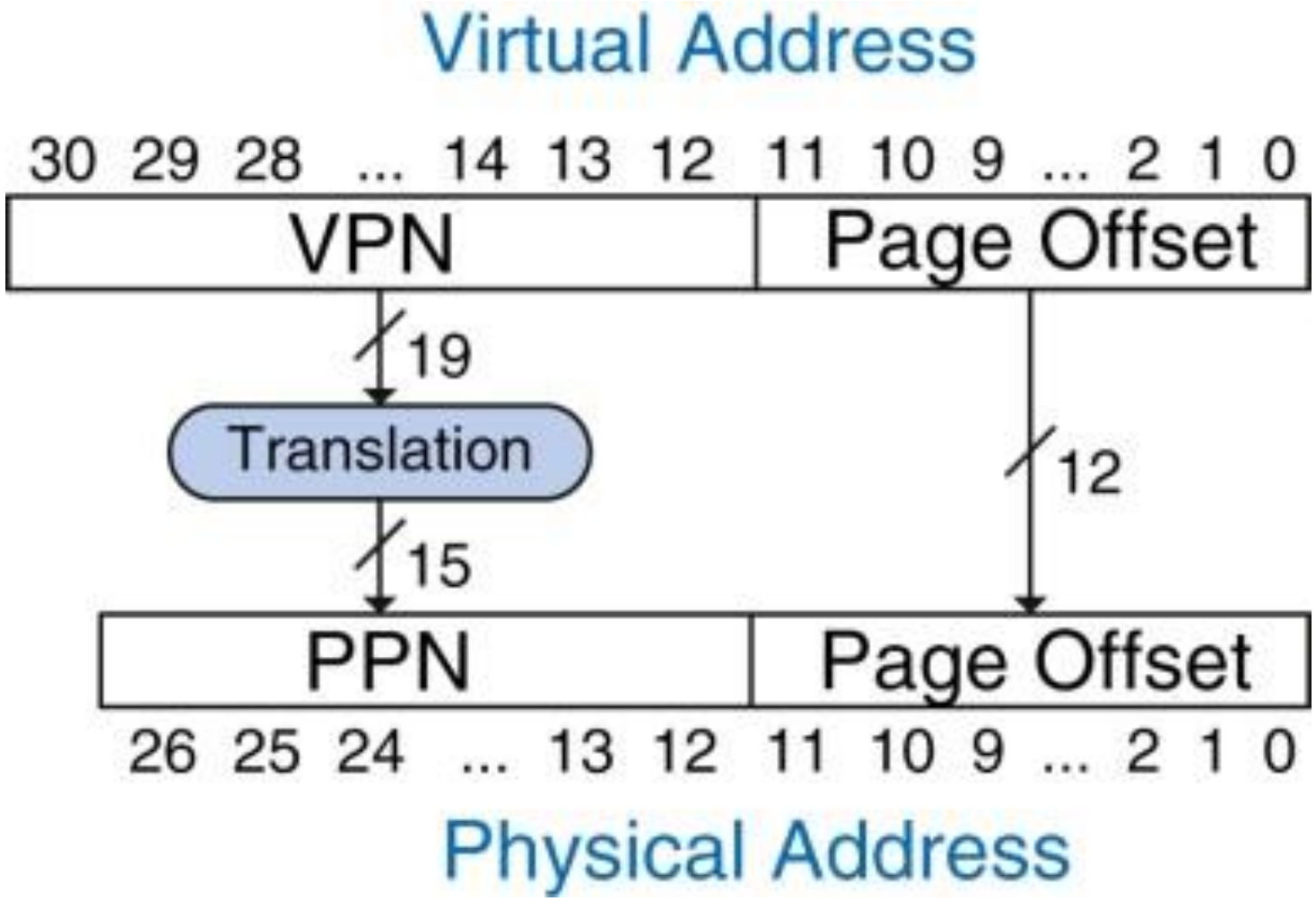


Figure 8.23 The page table for Figure 8.21

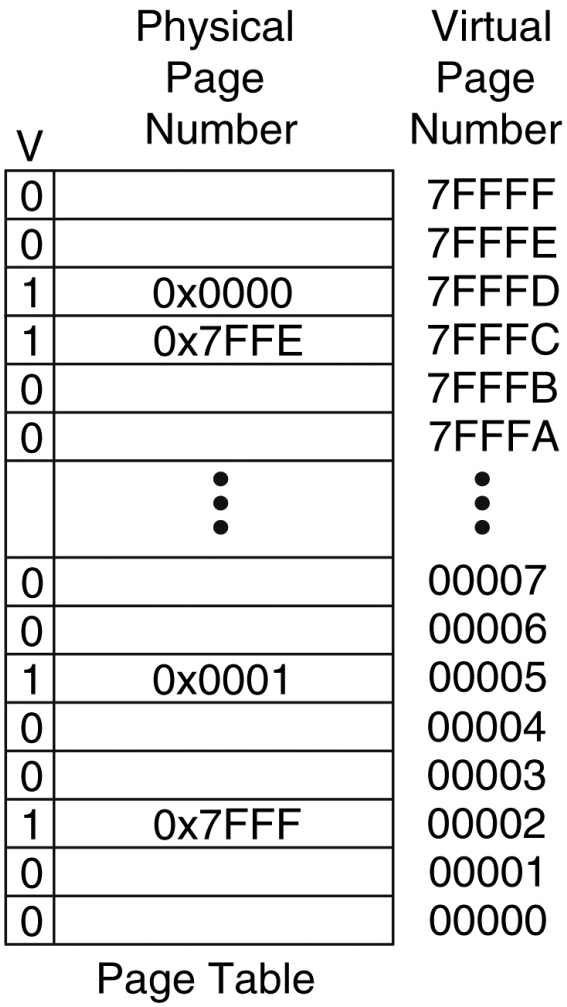


Figure 8.24 Address translation using the page table

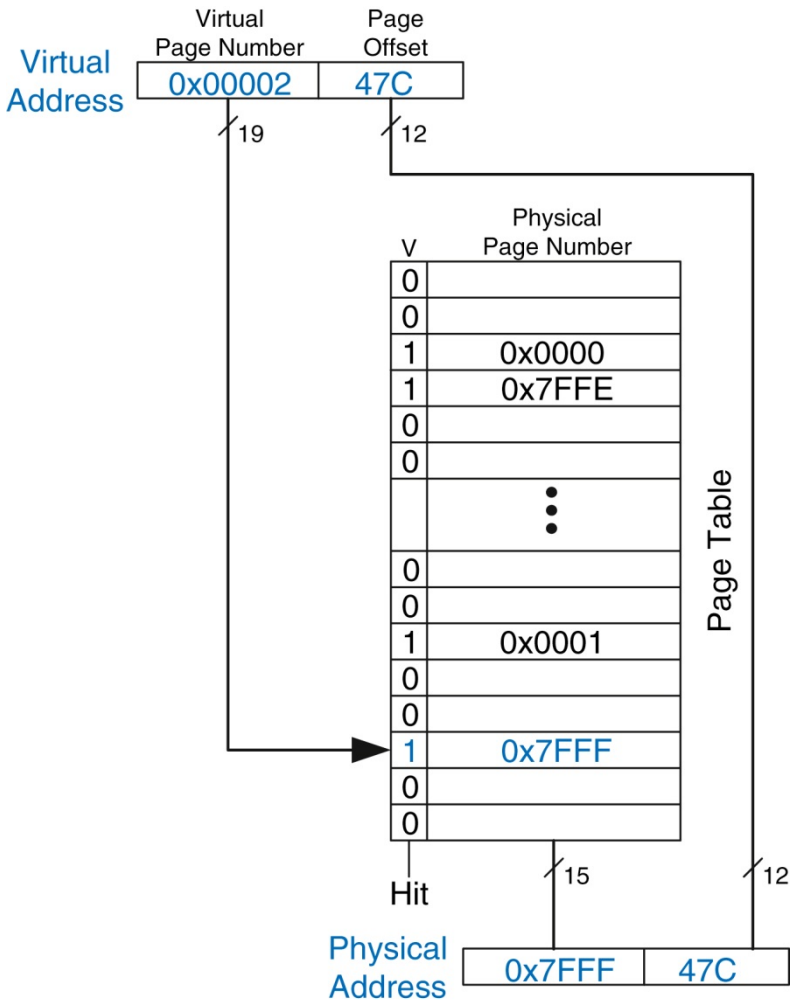


Figure 8.25 Address translation using a two-entry TLB

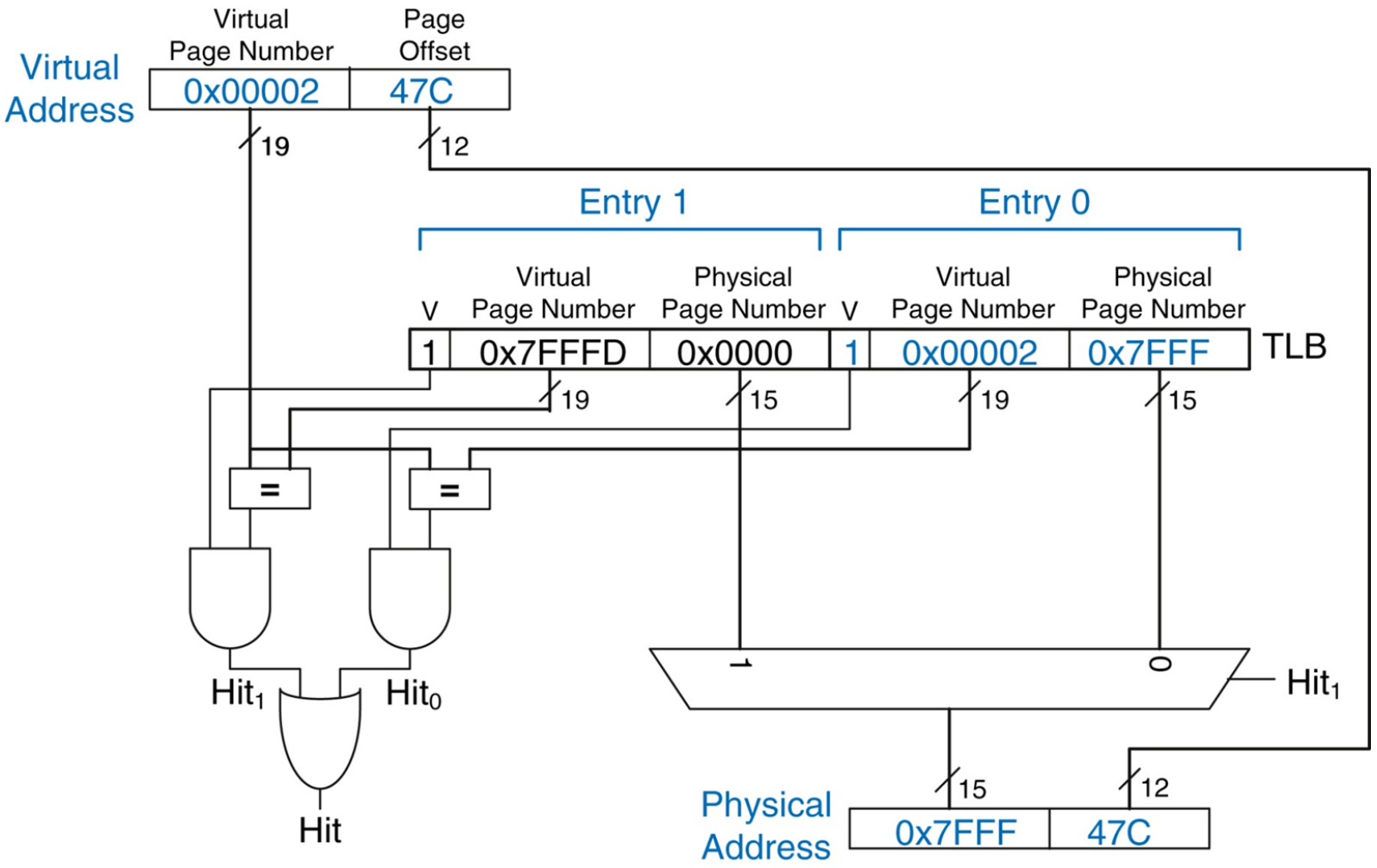


Figure 8.26 Hierarchical page tables

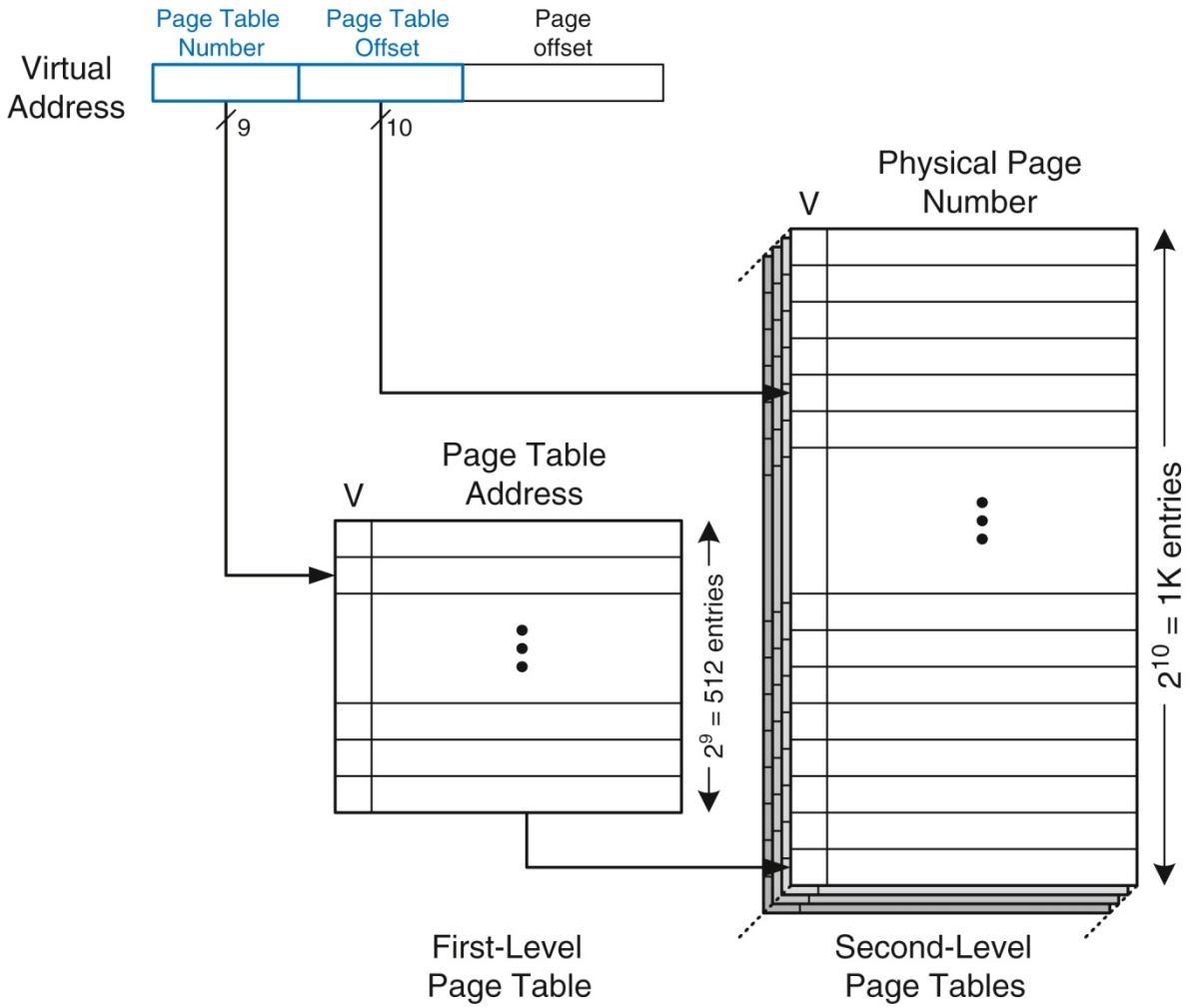


Figure 8.27 Address translation using a two-level page table

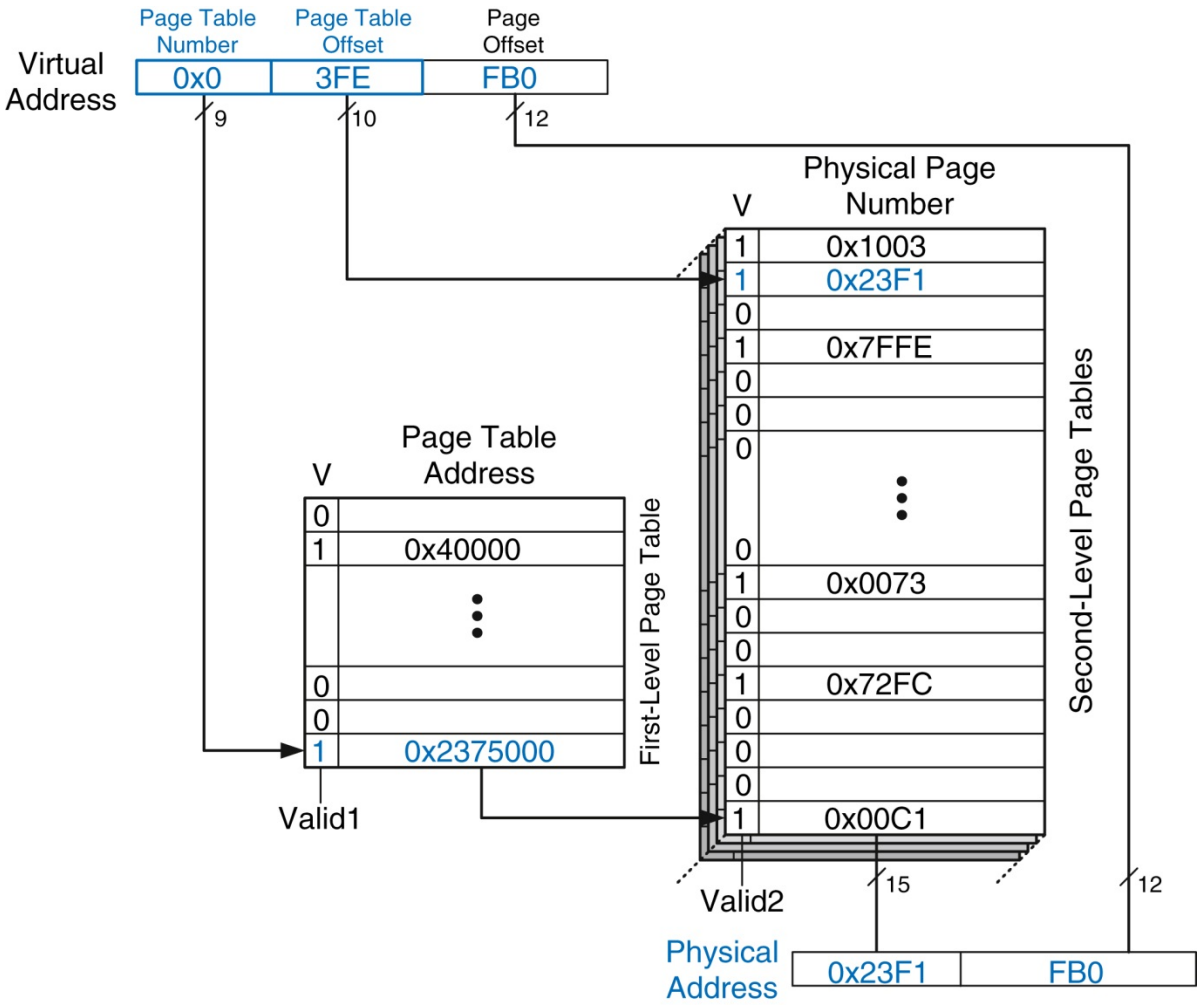


Figure 8.28 Building blocks

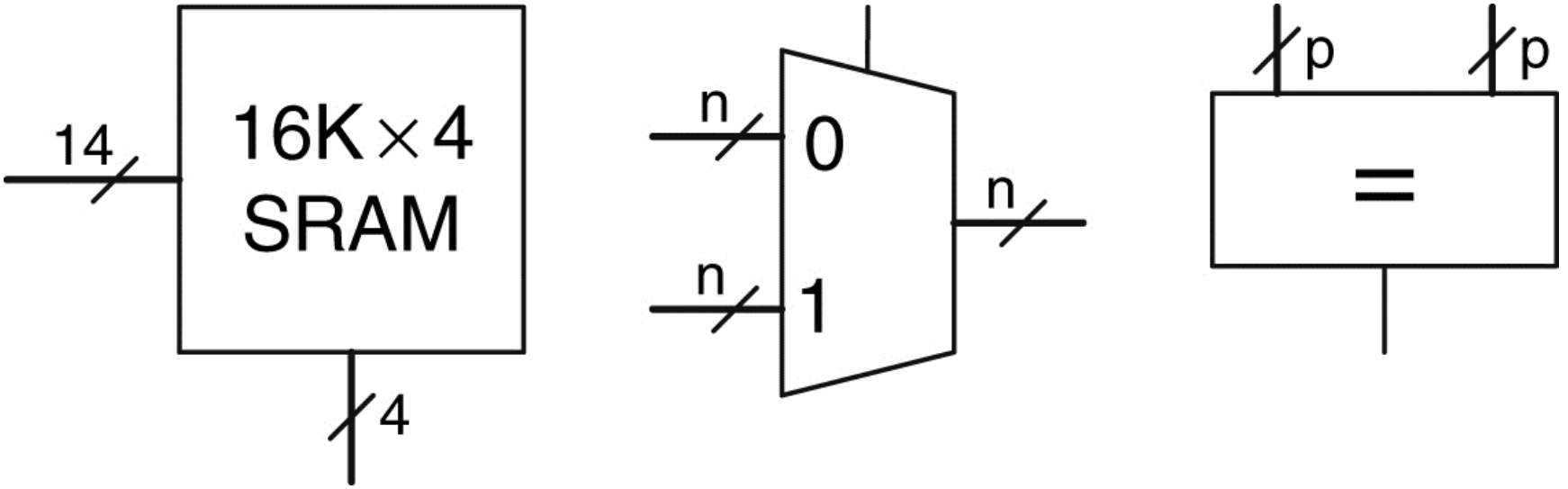
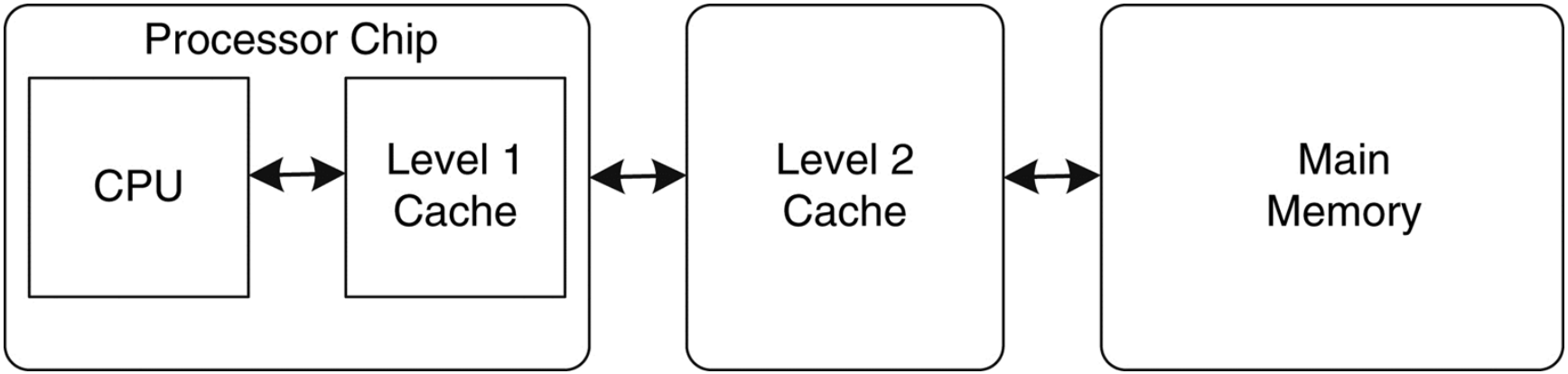
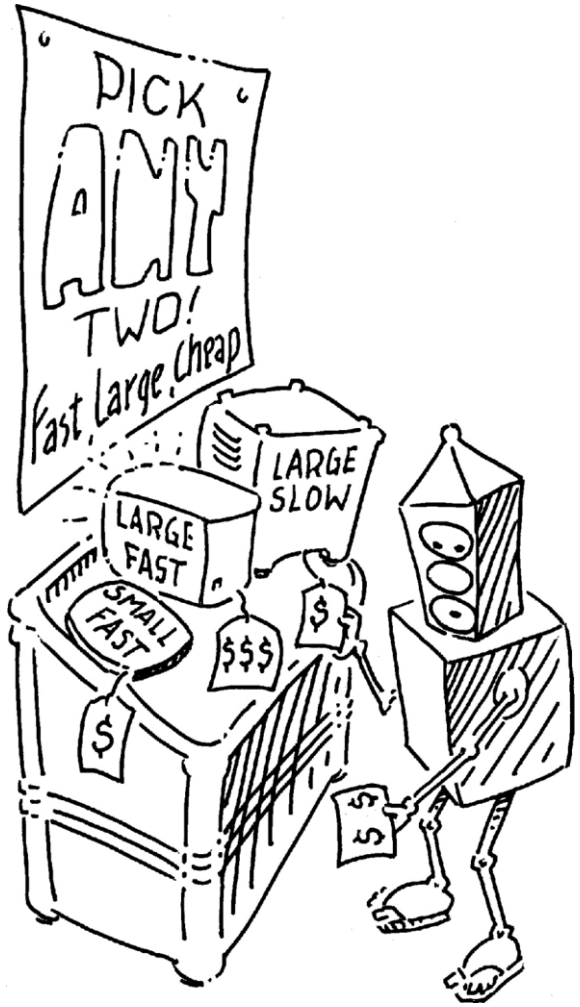


Figure 8.29 Computer system





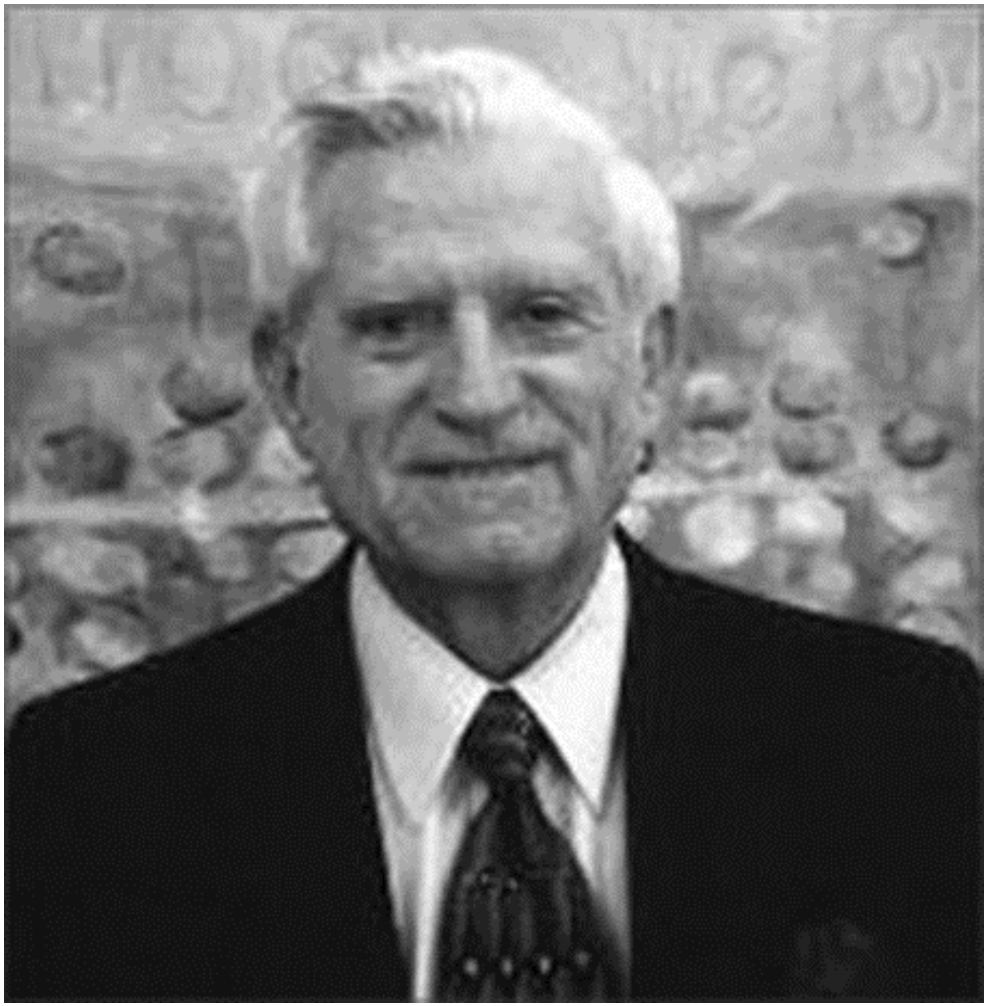


Fig u08-01