APPENDIX D

Advanced Topics

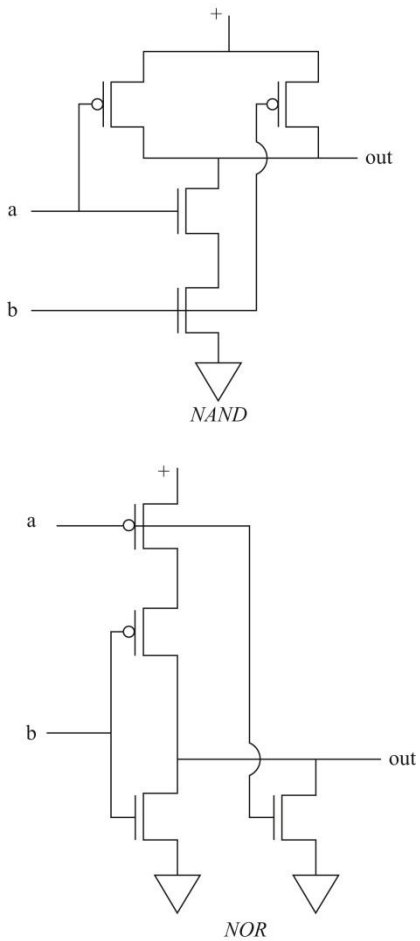

FIGURE D.1: Two-input NAND and NOR complementary logic gates..

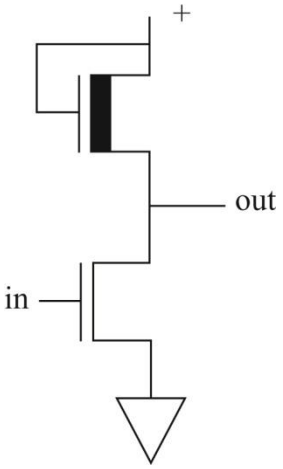

FIGURE D.2:: An nMOS inverter..

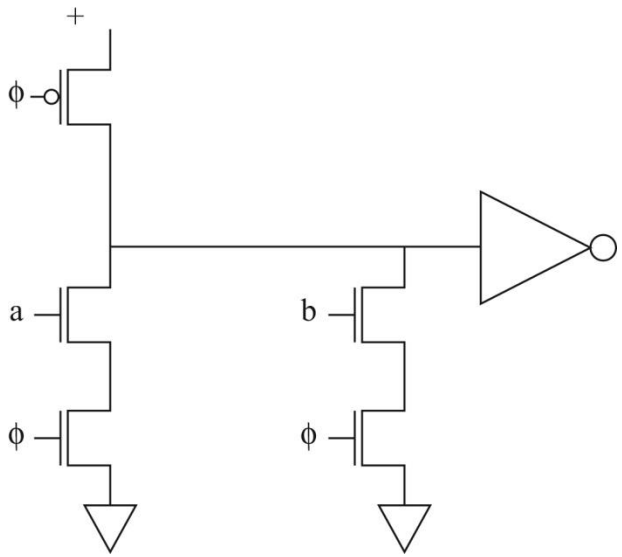

FIGURE D.3:: A domino logic gate.

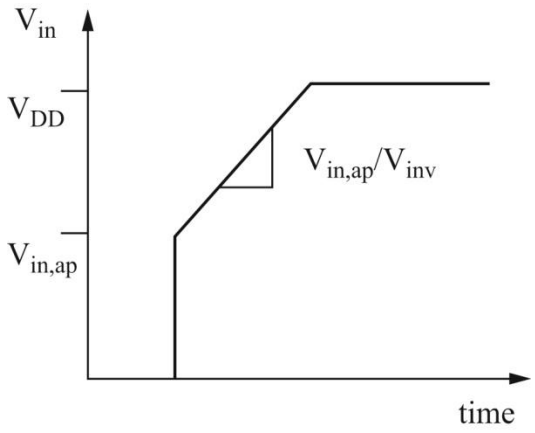

FIGURE D.2:: SakuraieNewton model for gate input voltage.

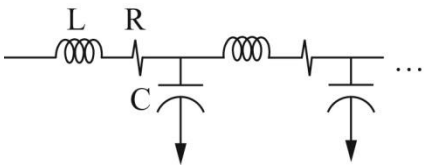

Figure 1.5: Organization of a Turing machine.