Chapter 2

Transistors and Integrated Circuits

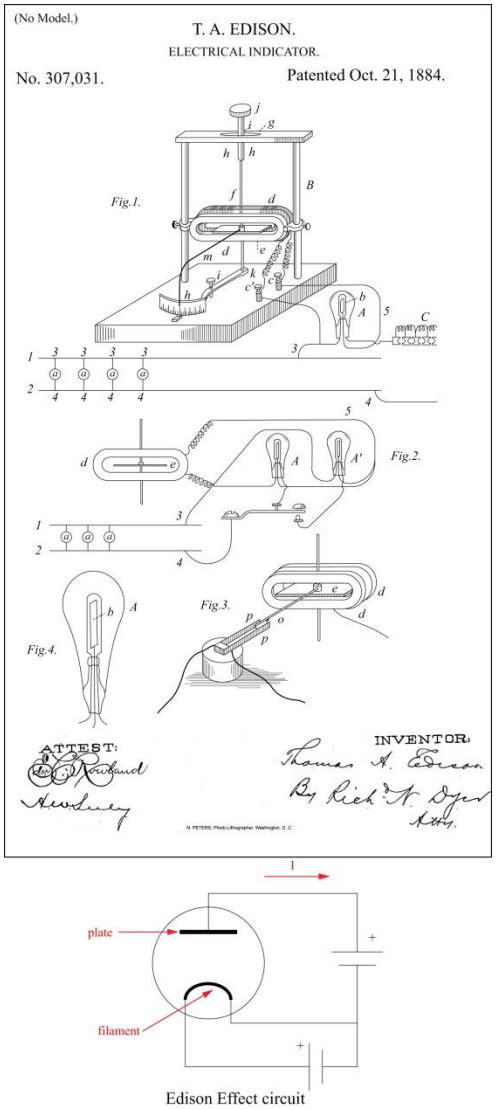


Figure 2.1: Operation of an Edison Effect device.

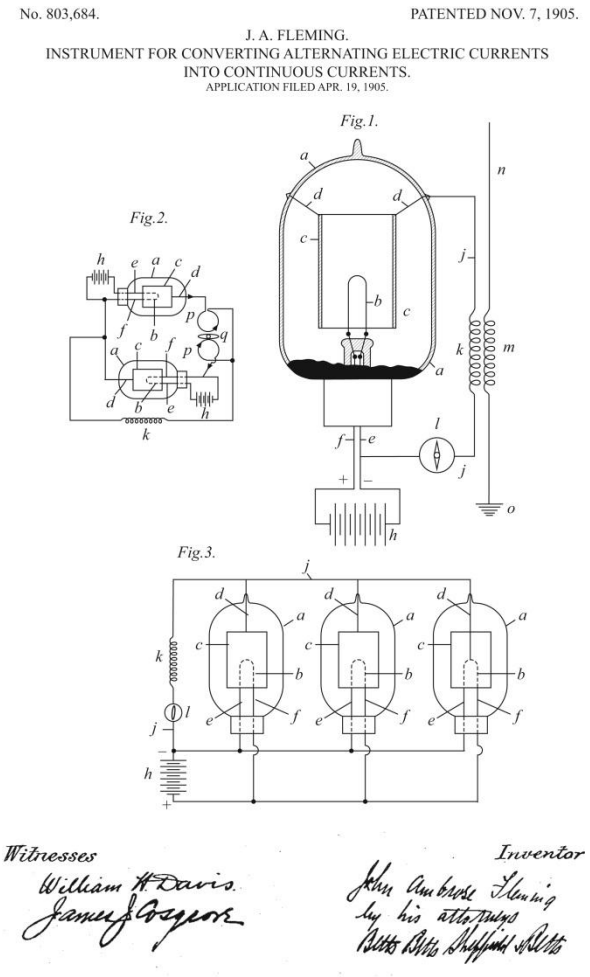


Figure 2.2: The Fleming valve.

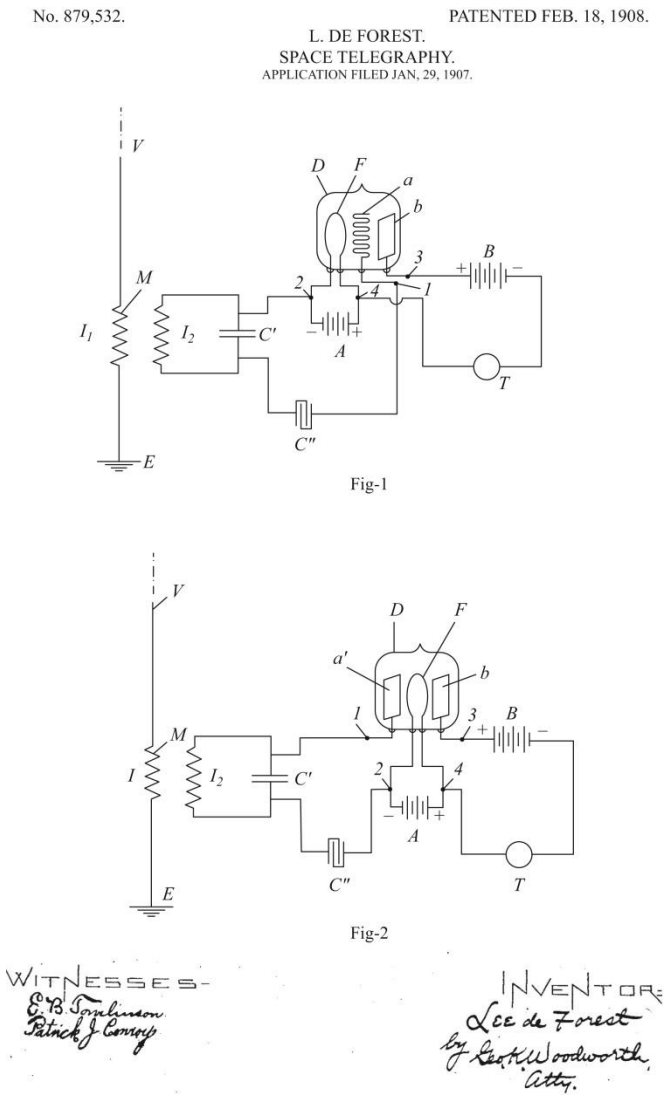


Figure 2.3: The De Forest triode.

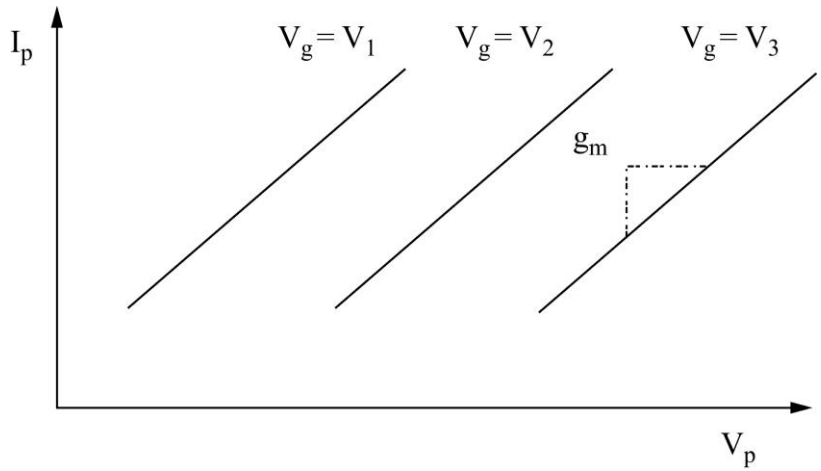


Figure 2.4: Idealized characteristics of a vacuum tube triode..

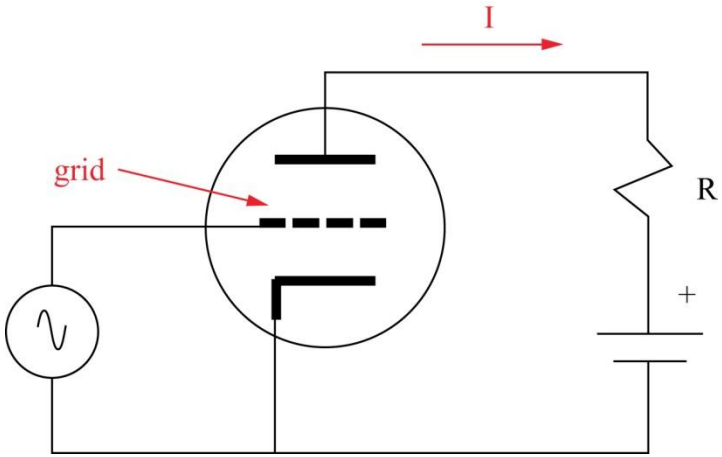


Figure 2.5: A vacuum tube amplifier.

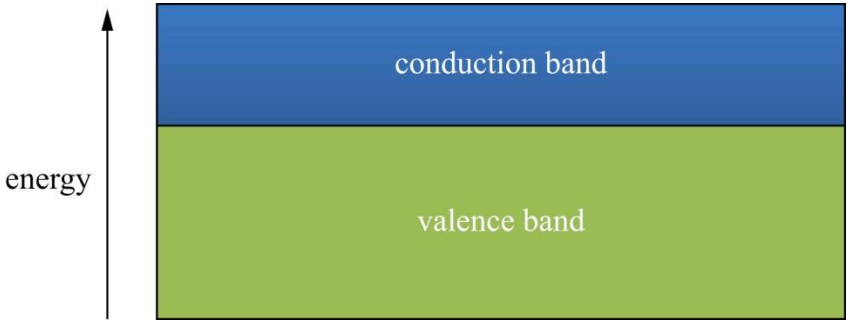


Figure 2.6: Energy bands in a conductor.

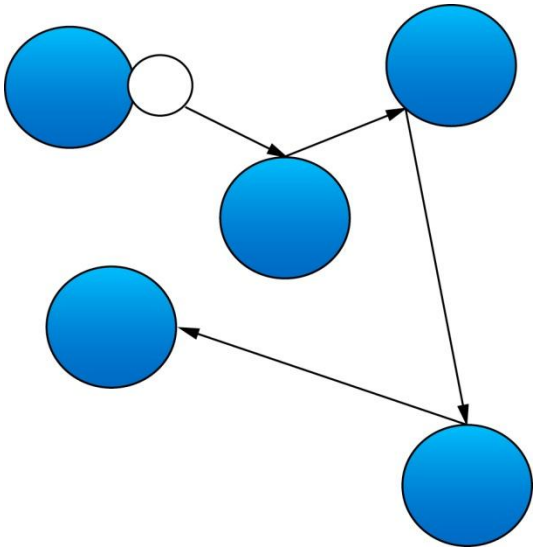


Figure 2.7: A random walk through a material.

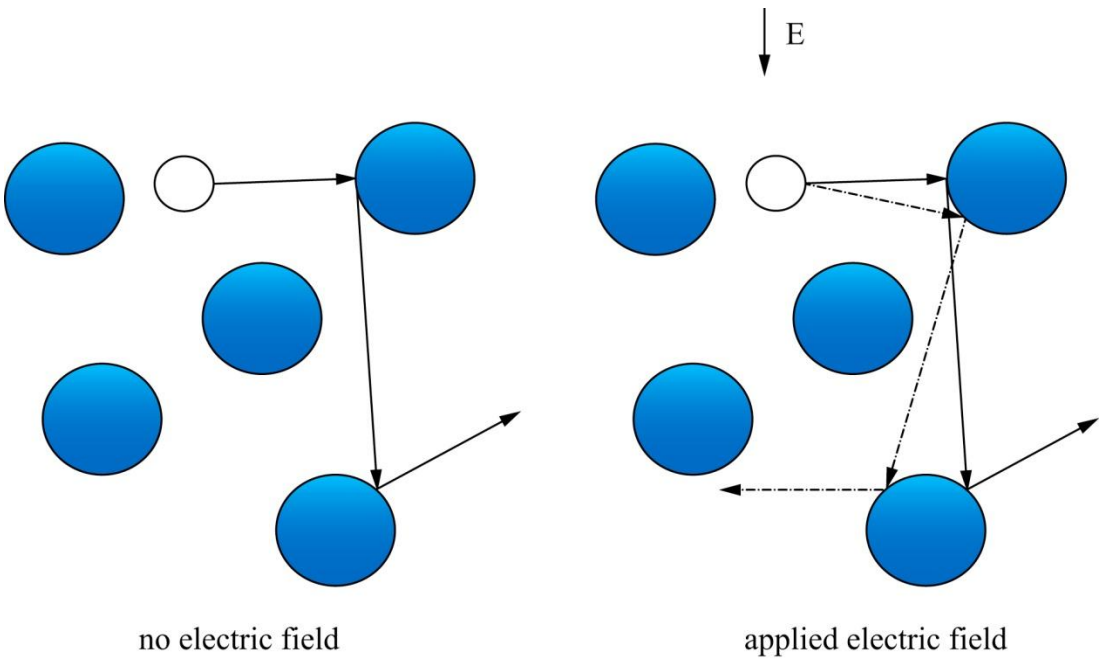


Figure 2.8: A random walk influenced by an applied field.

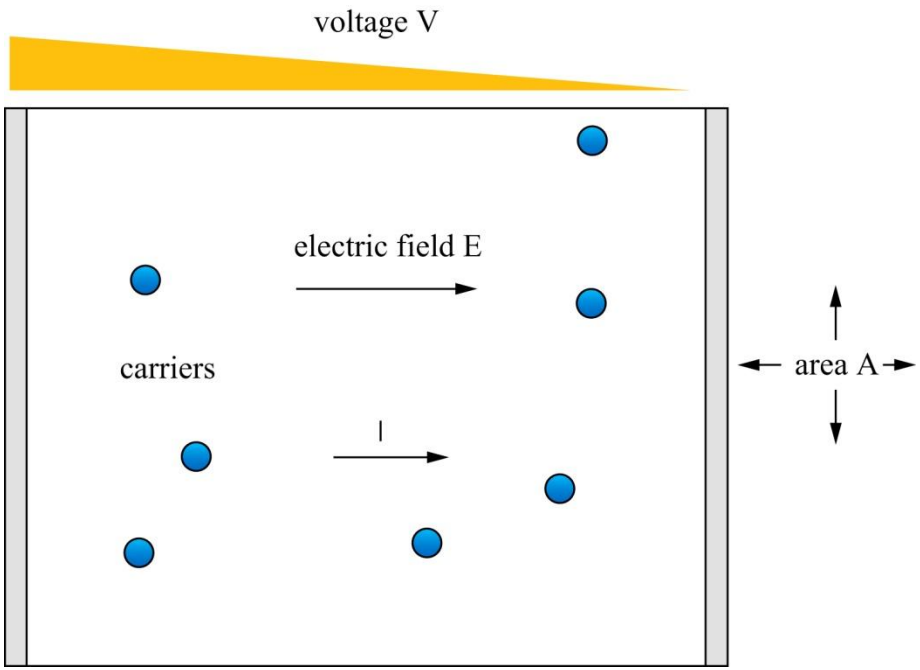


Figure 2.9: A model for drift current.

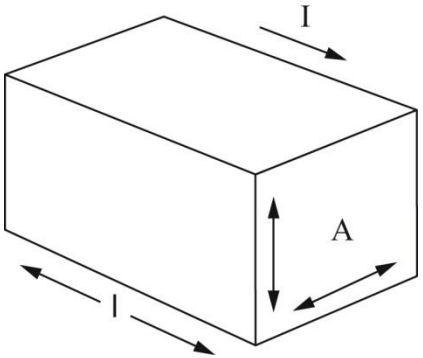


Figure 2.10: Resistance of a block of material.

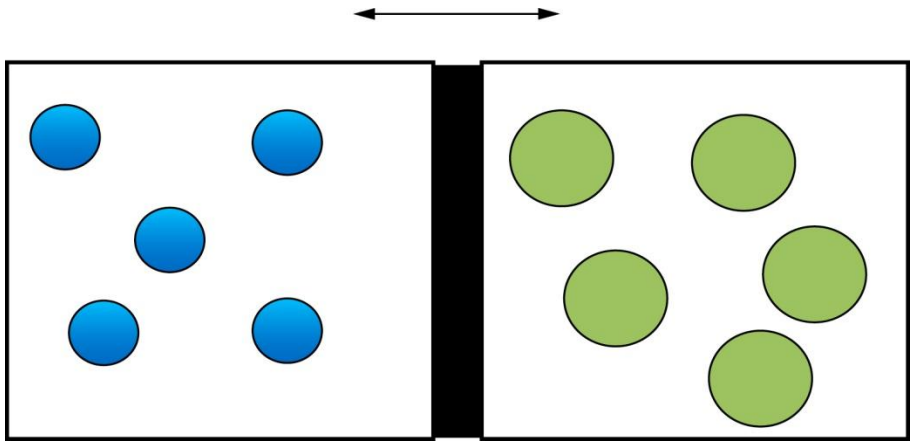


Figure 2.11: Two gasses separated by a movable piston as an example of temperature.

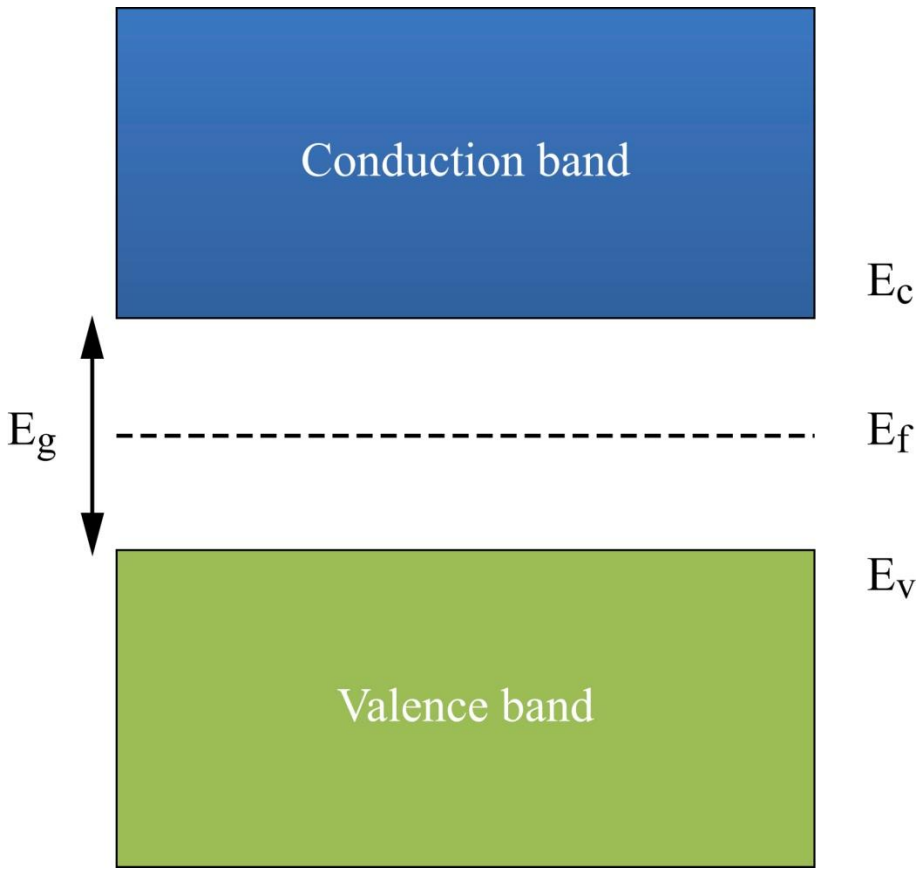


Figure 2.12: Conduction and valence bands in a semiconductor.

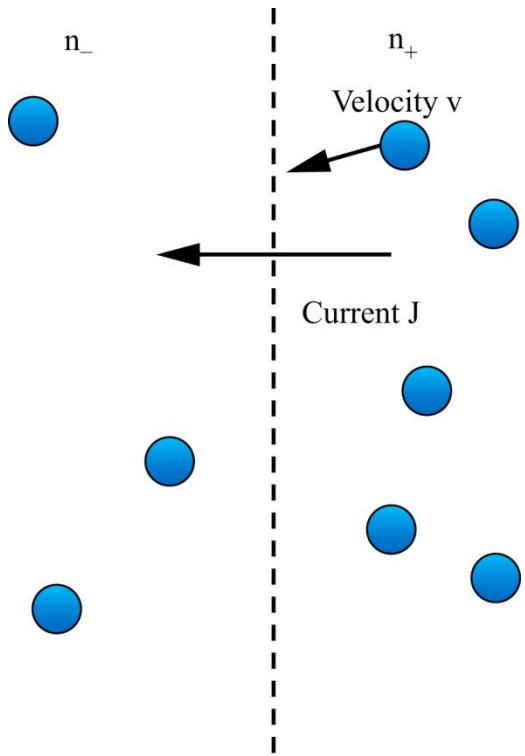


Figure 2.13: Diffusion current.

Figure 2.14: The first transistor.

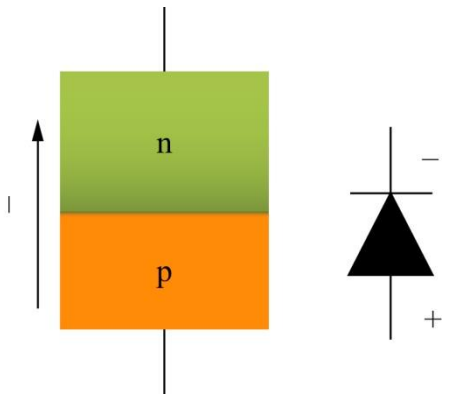


Figure 2.15: Structure and schematic symbol for a semiconductor diode.

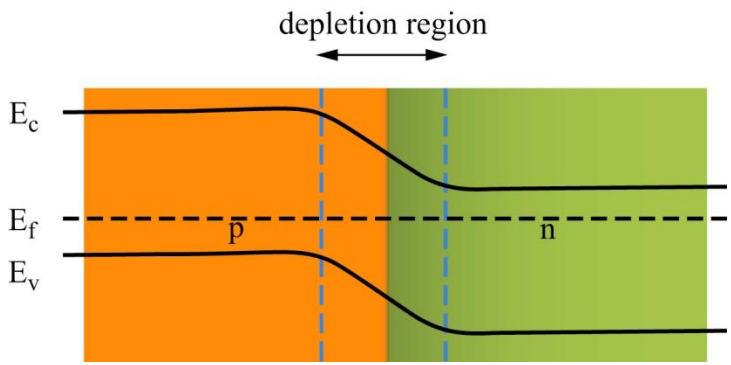


Figure 2.16: Band structures at a p-n junction.

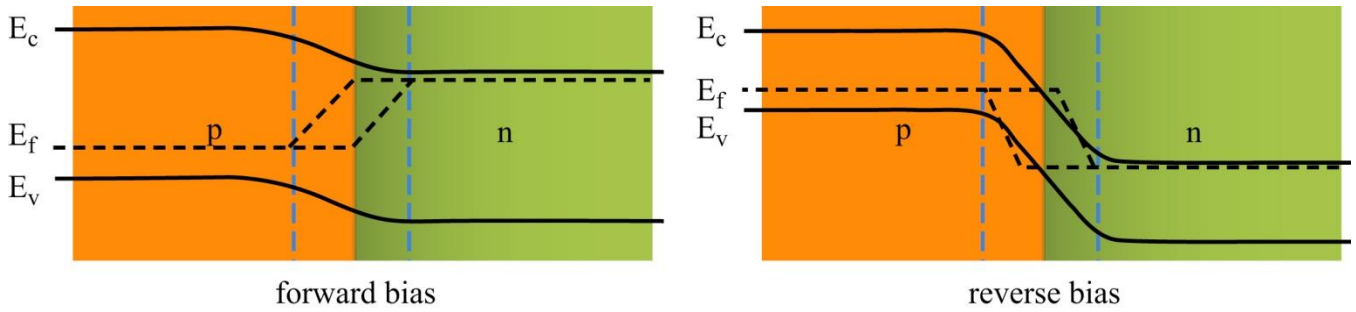


Figure 2.17: Effect of applying bias voltage to a diode.

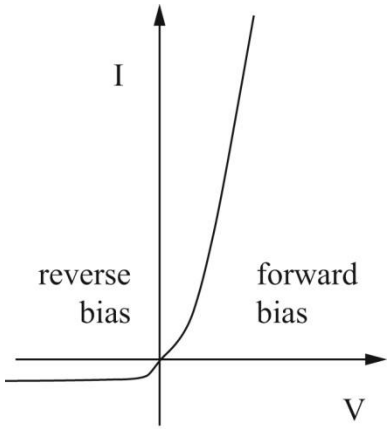


Figure 2.18: Current versus voltage characteristics of the diode.

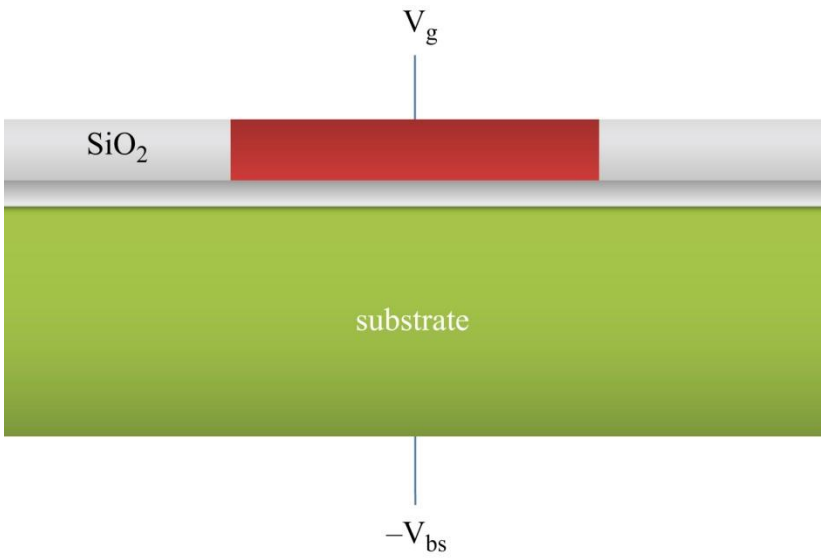


Figure 2.19: Structure of the MOS capacitor.

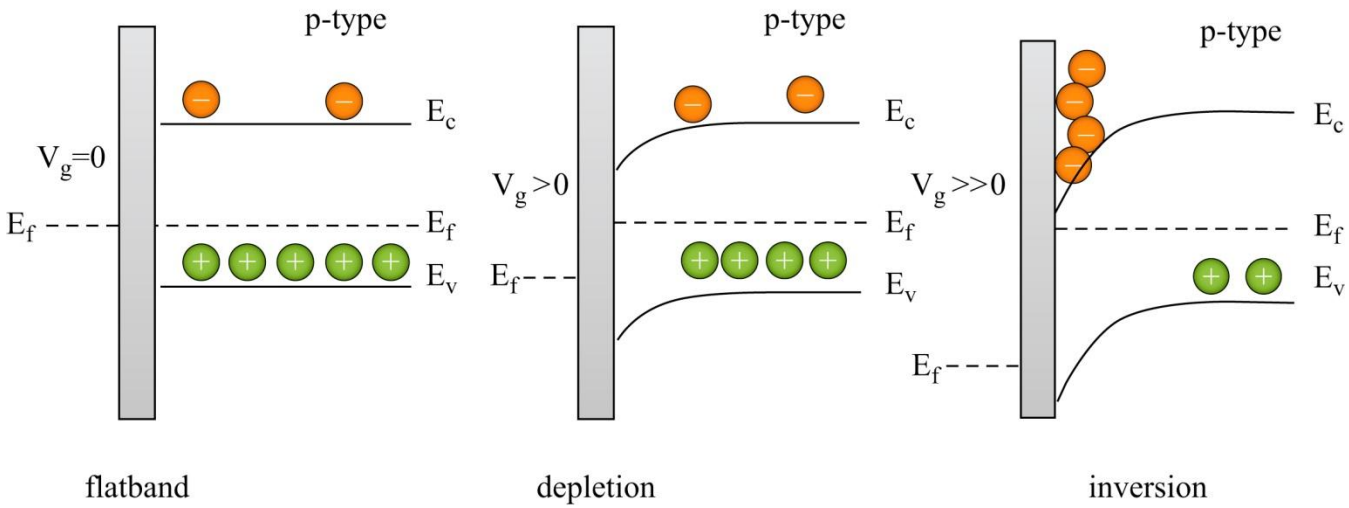


Figure 2.20: Operation of the MOS capacitor [Sze81].

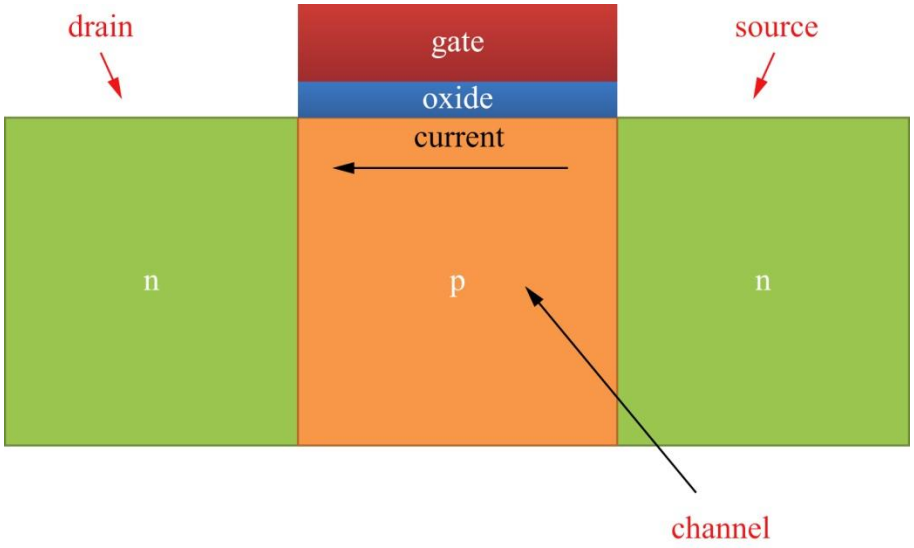


Figure 2.21: Cross section of an n-type MOS transistor.

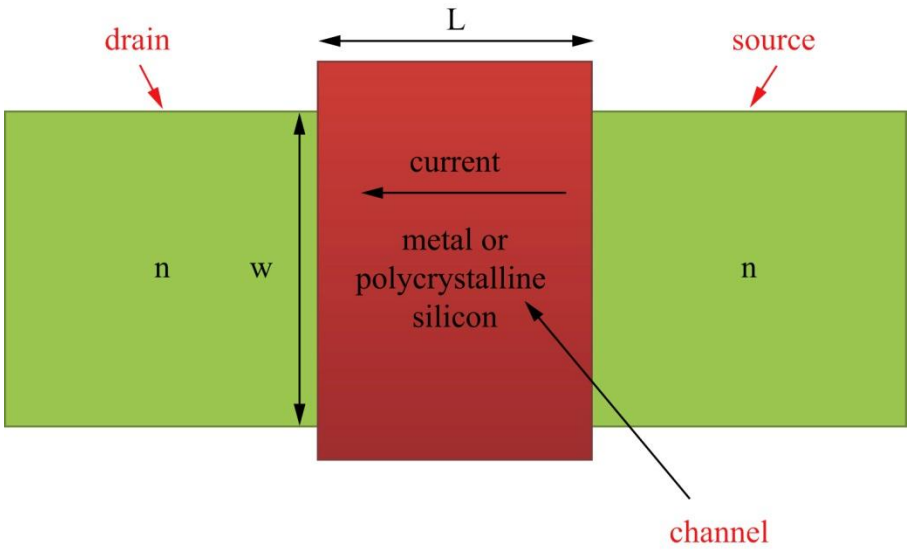


Figure 2.9: View from above of an n-type MOS transistor.

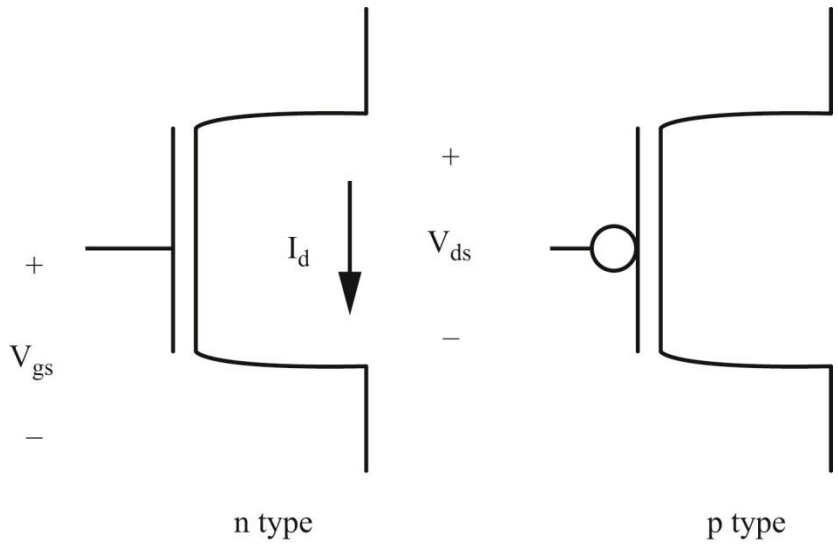


Figure 2.23: Symbol for the transistor and its associated voltages and currents.

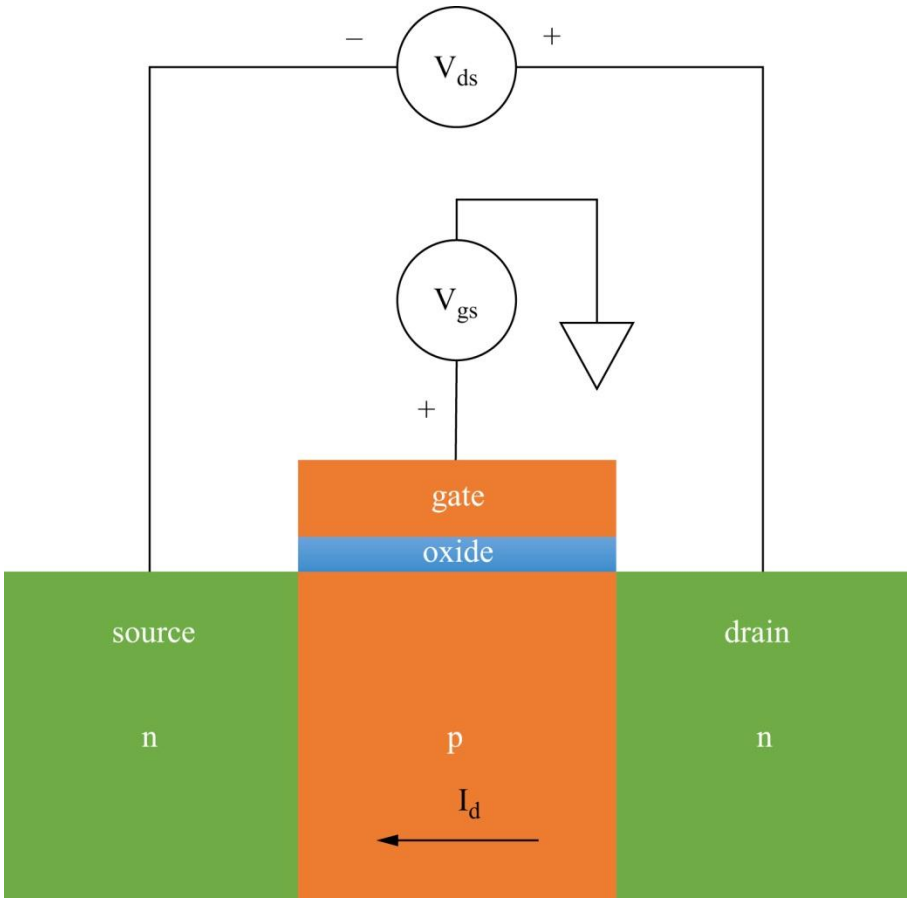


Figure 2.24: Voltages and currents in the MOSFET.

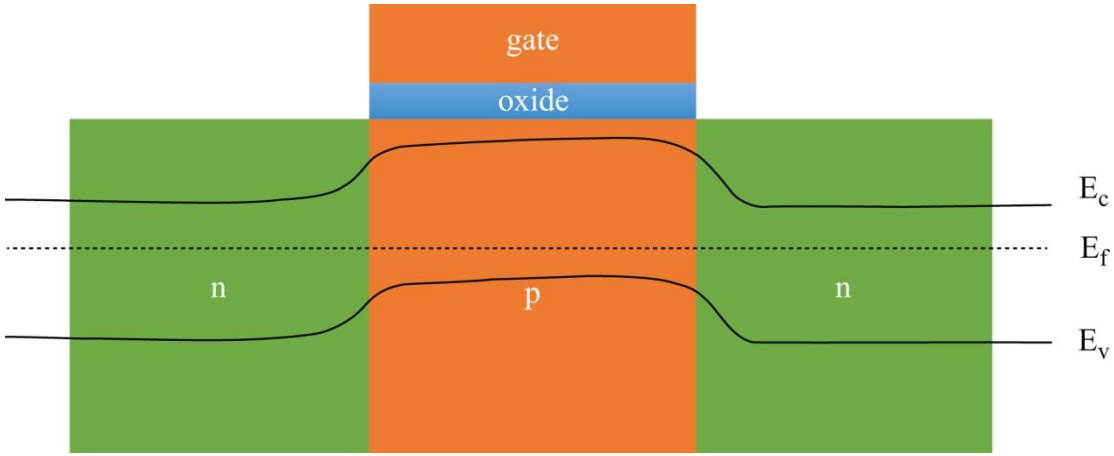


Figure 2.25: Energy bands in the n-type MOSFET.

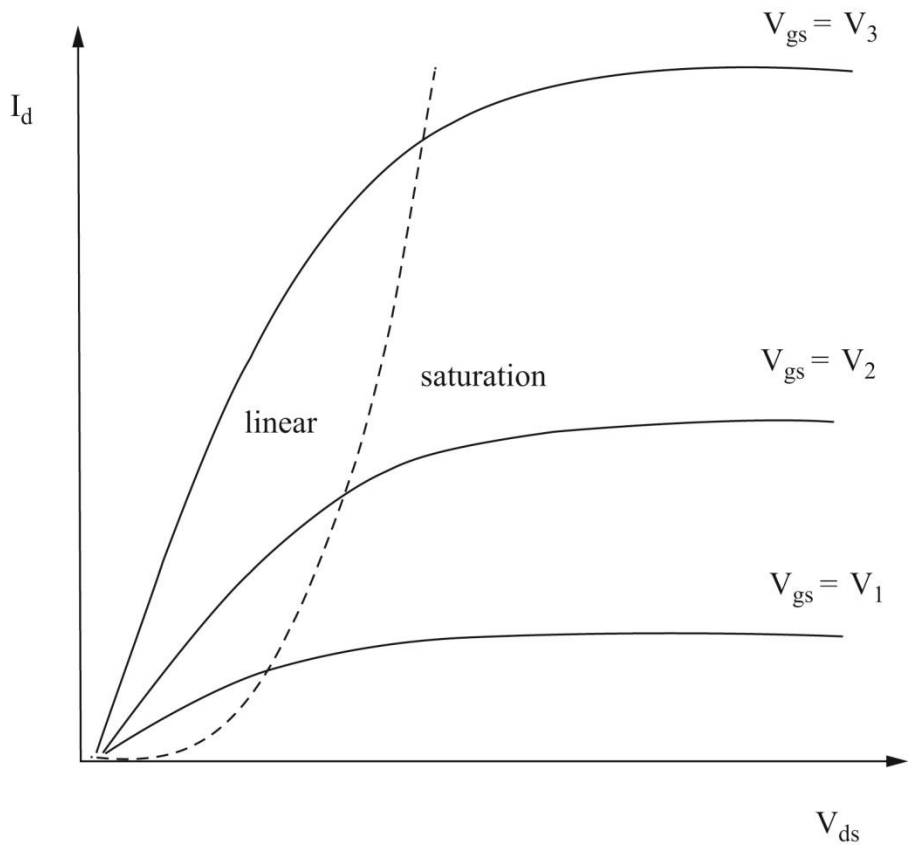


Figure 2.26: Current versus voltage curves for the MOS transistor.

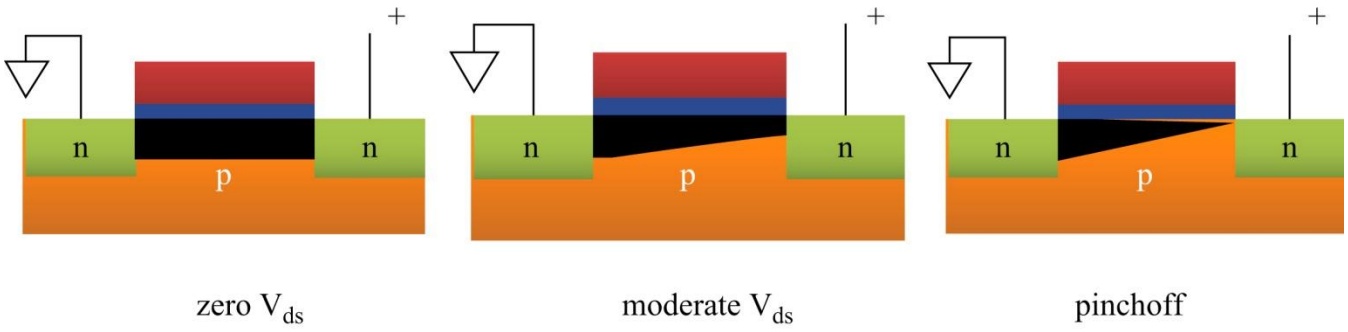


Figure 2.27: Evolution of the minority carrier populations with increasing source-to-drain voltage.

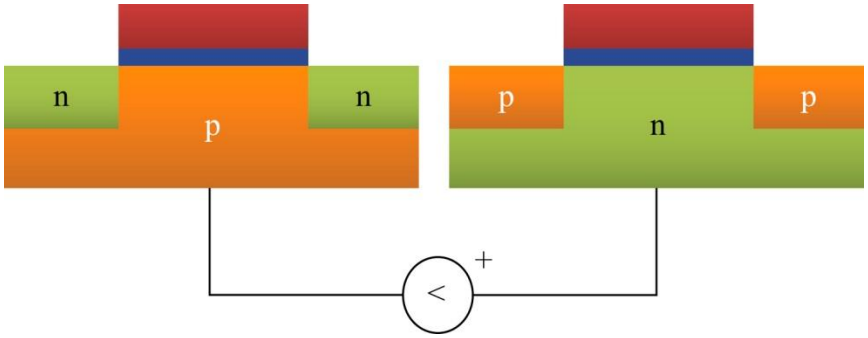


Figure 2.28: Biasing of n-type and p-type transistors.

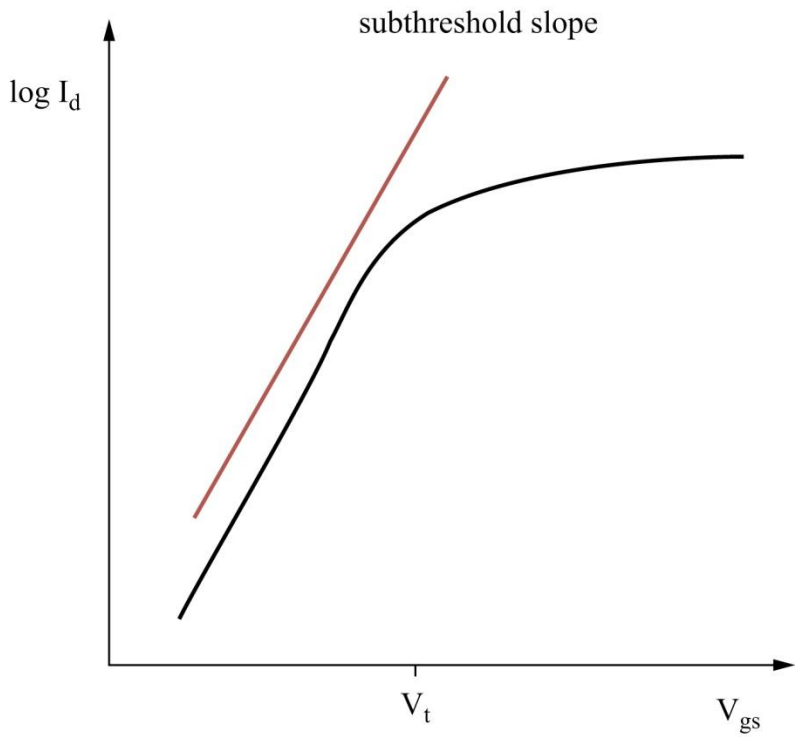


Figure 2.29: Subthreshold current characteristics.

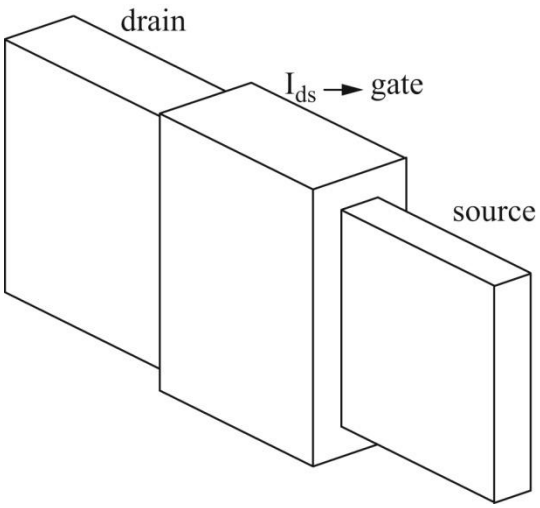


Figure 2.30: Structure of a finFET.

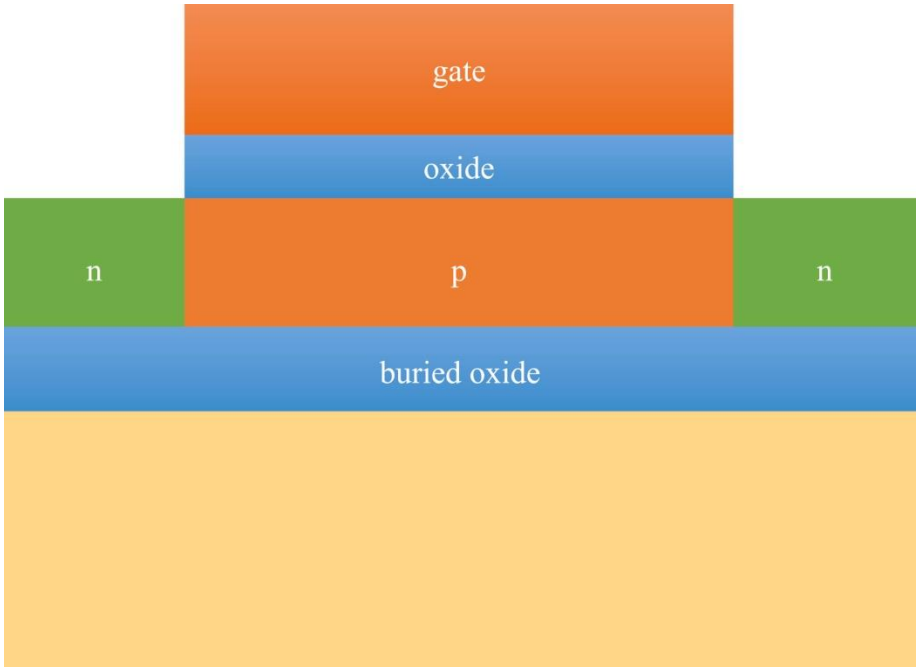


Figure 2.31: Cross section of a silicon-on-insulator (SOI) transistor.

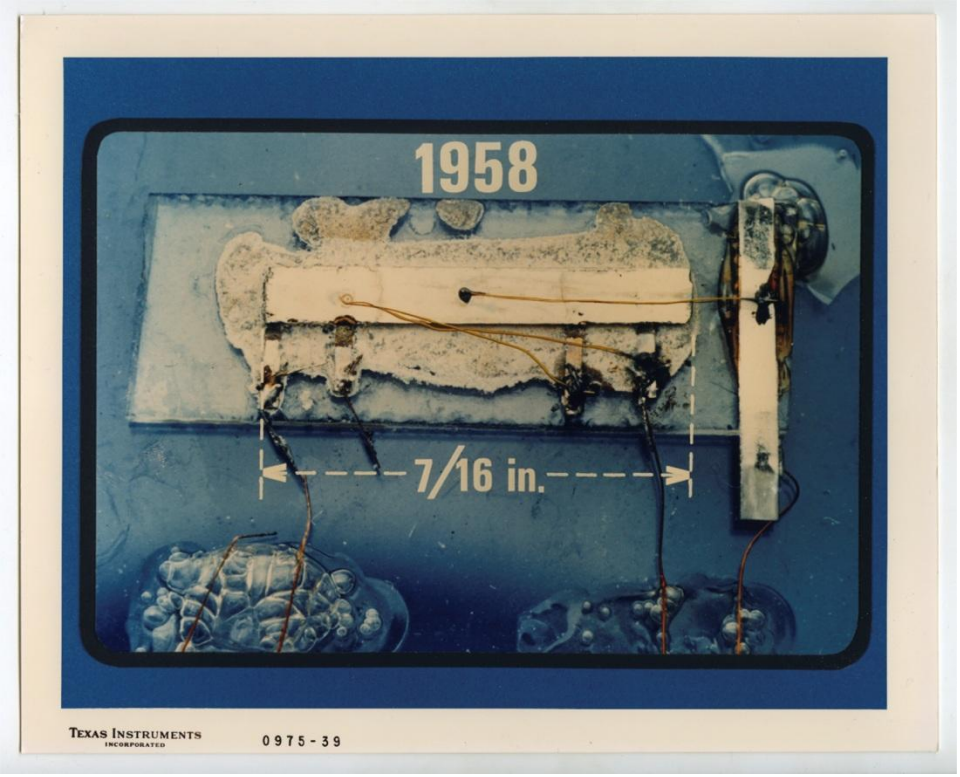


Figure 2.32: The first integrated circuit, courtesy DeGolyer Library, Southern Methodist University, Texas Instruments records.

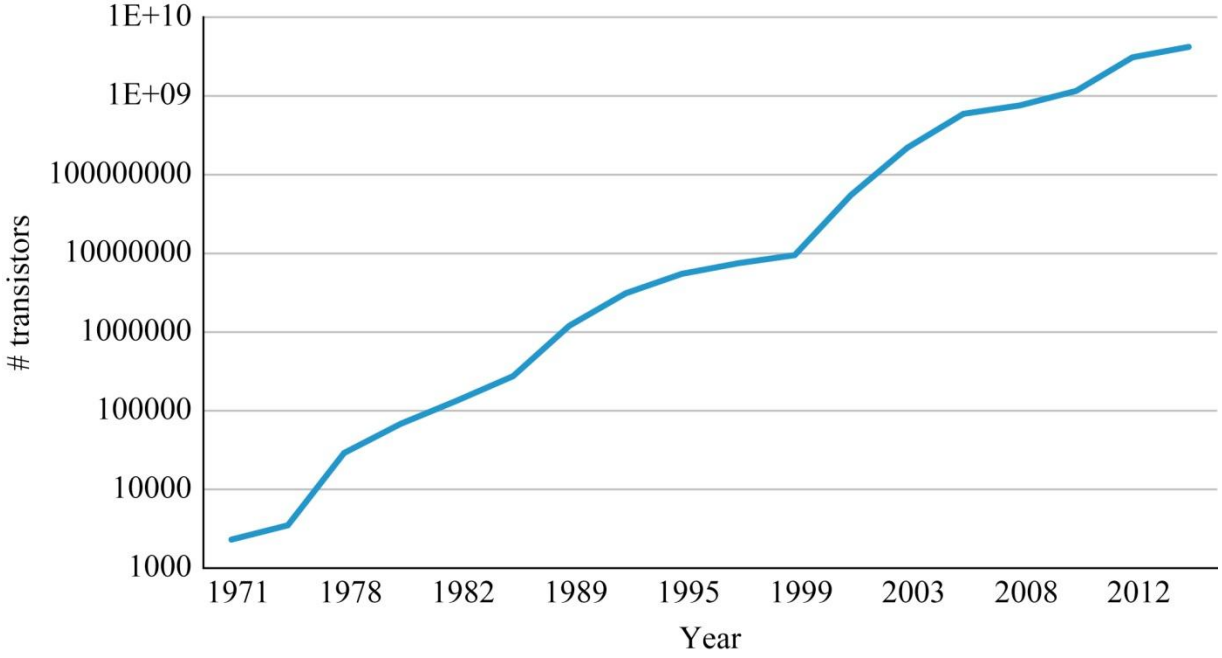


Figure 2.33: Moore's Law [Tra15].

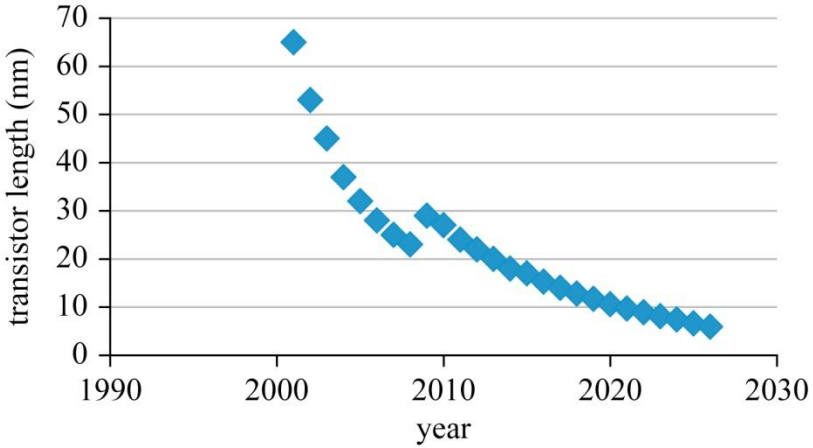


Figure 2.34: Transistor length over time [ITR01; ITR05; ITR07; ITR11; ITR13].

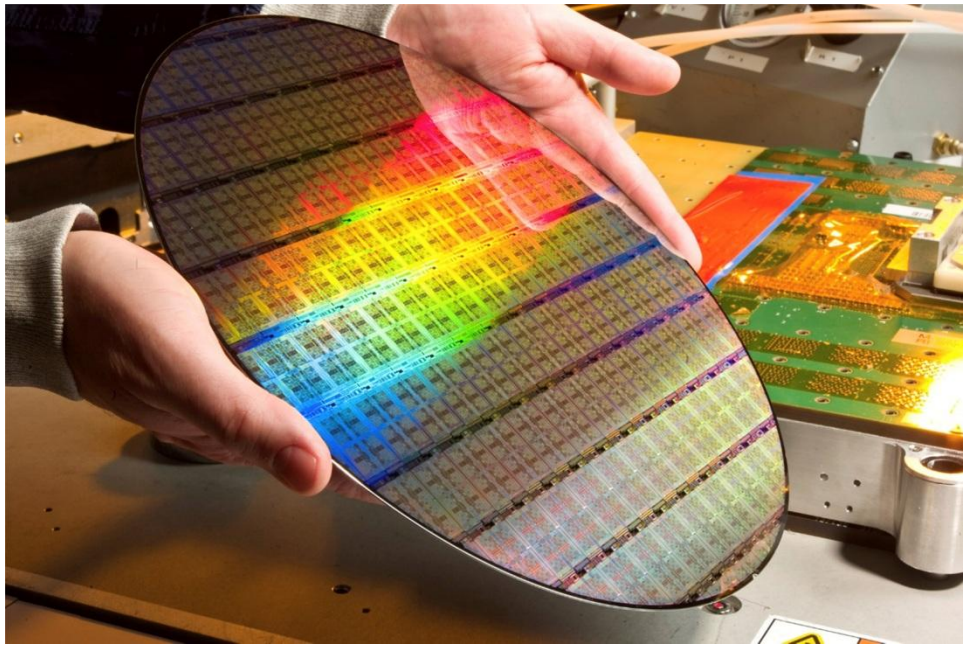


Figure 2.35: A wafer covered with integrated circuits.

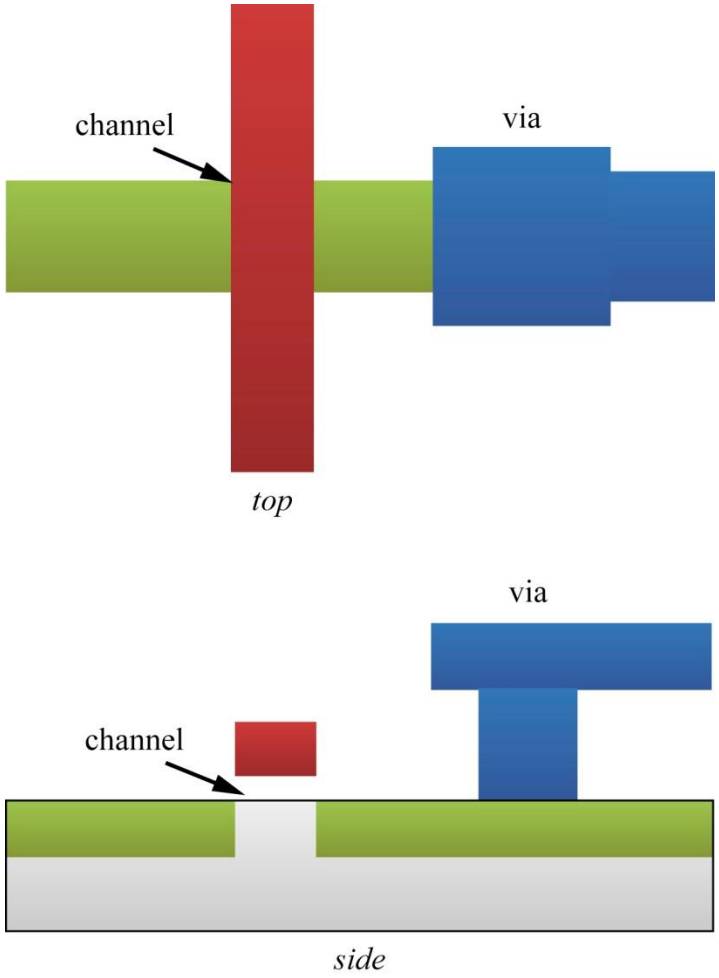


Figure 2.36: A chip layout from top and side views.

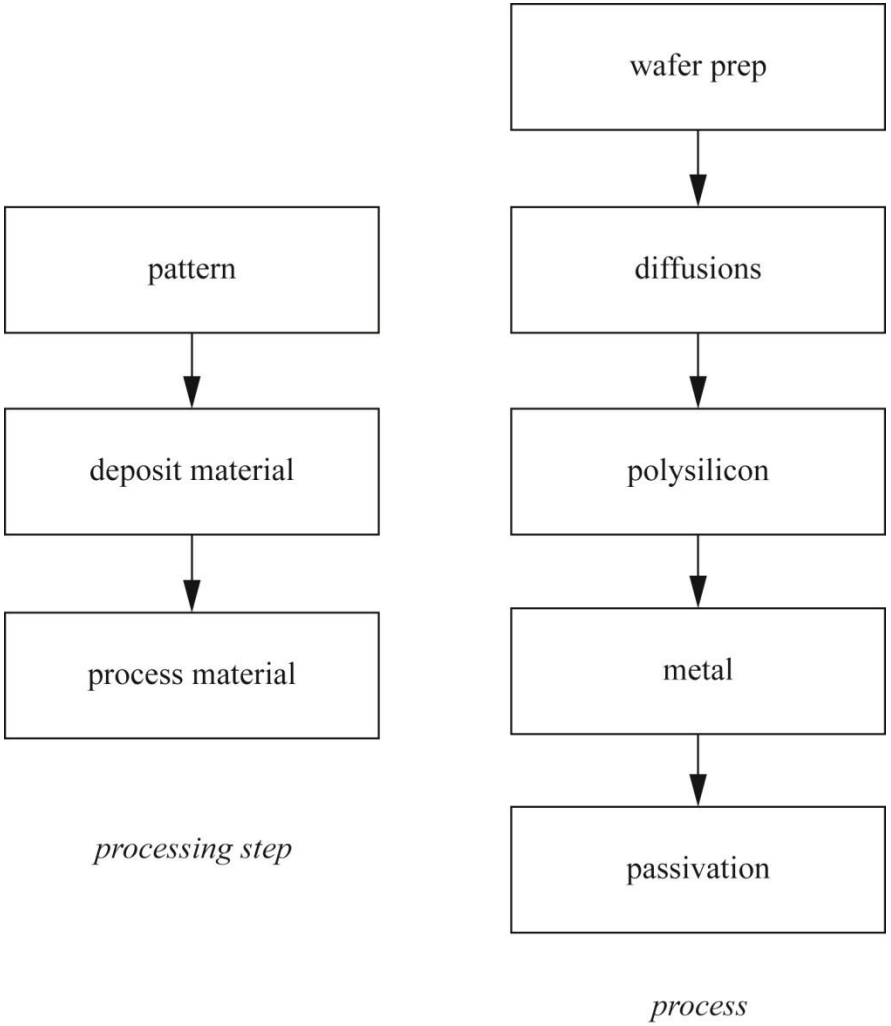


Figure 2.37: The fabrication process.

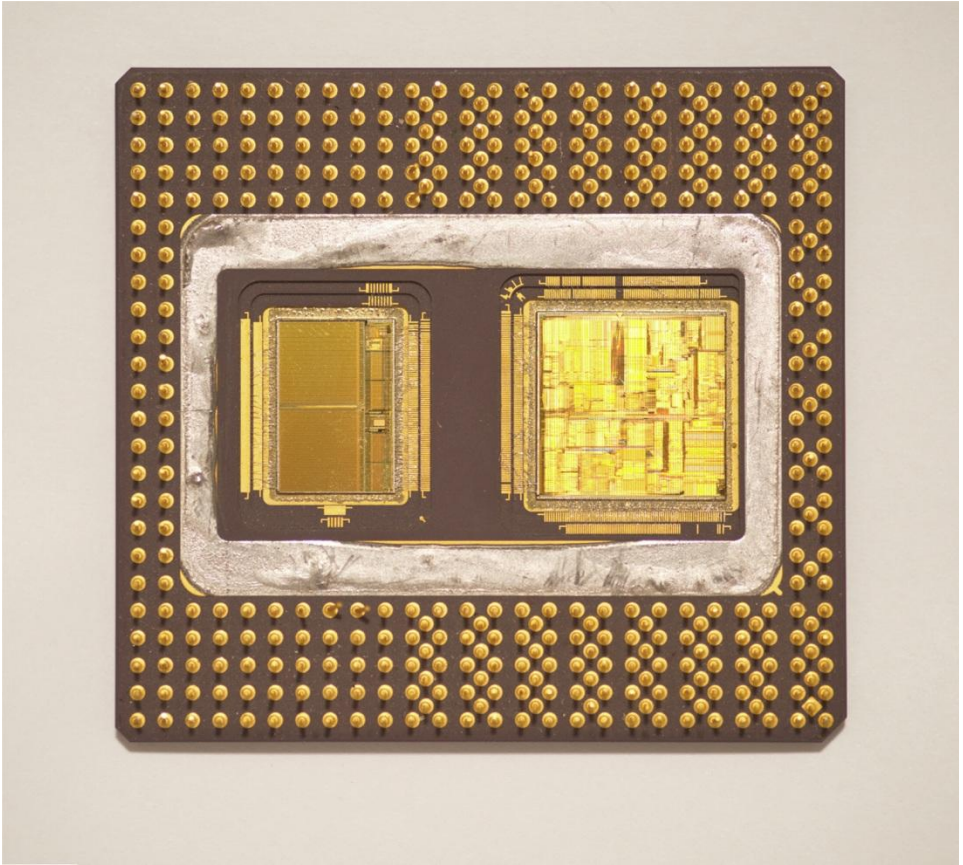


Figure 2.38: Intel Pentium Pro package c.1995.

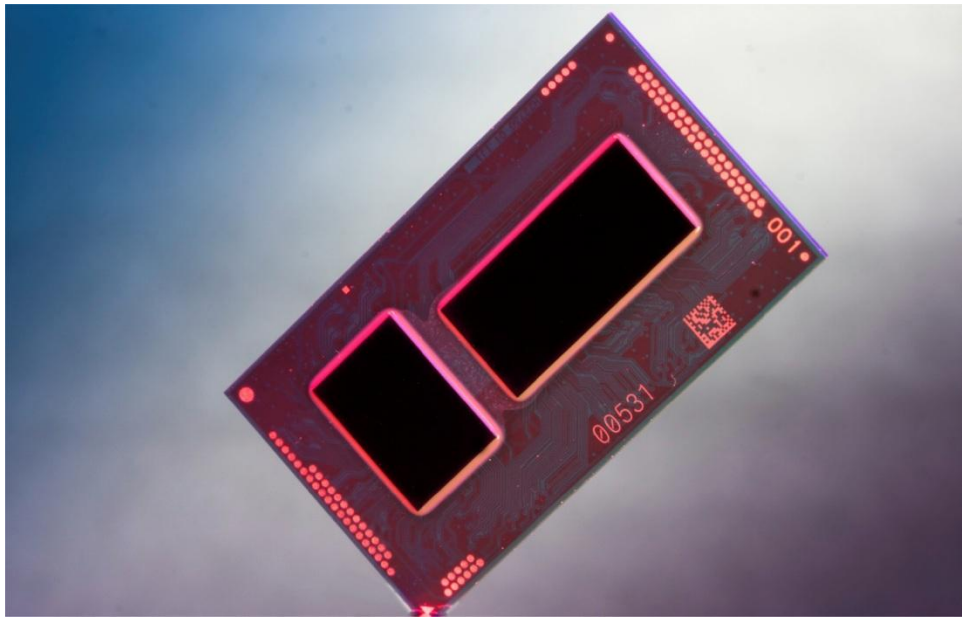


Figure 2.39: Intel Broadwell package c.2014.

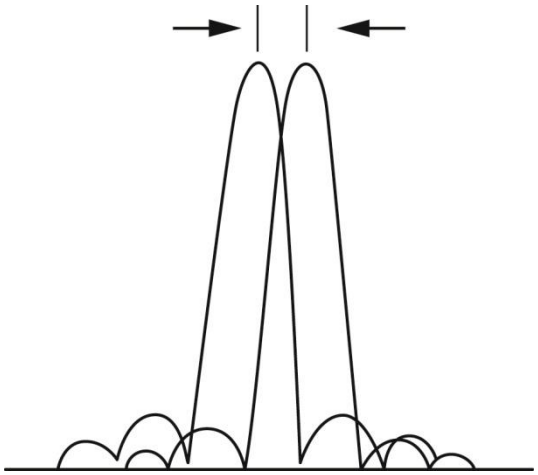


Figure 2.40: A lens projecting a mask onto a wafer.

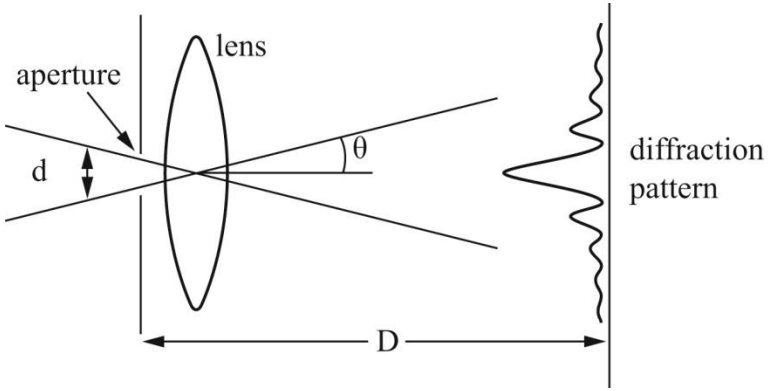
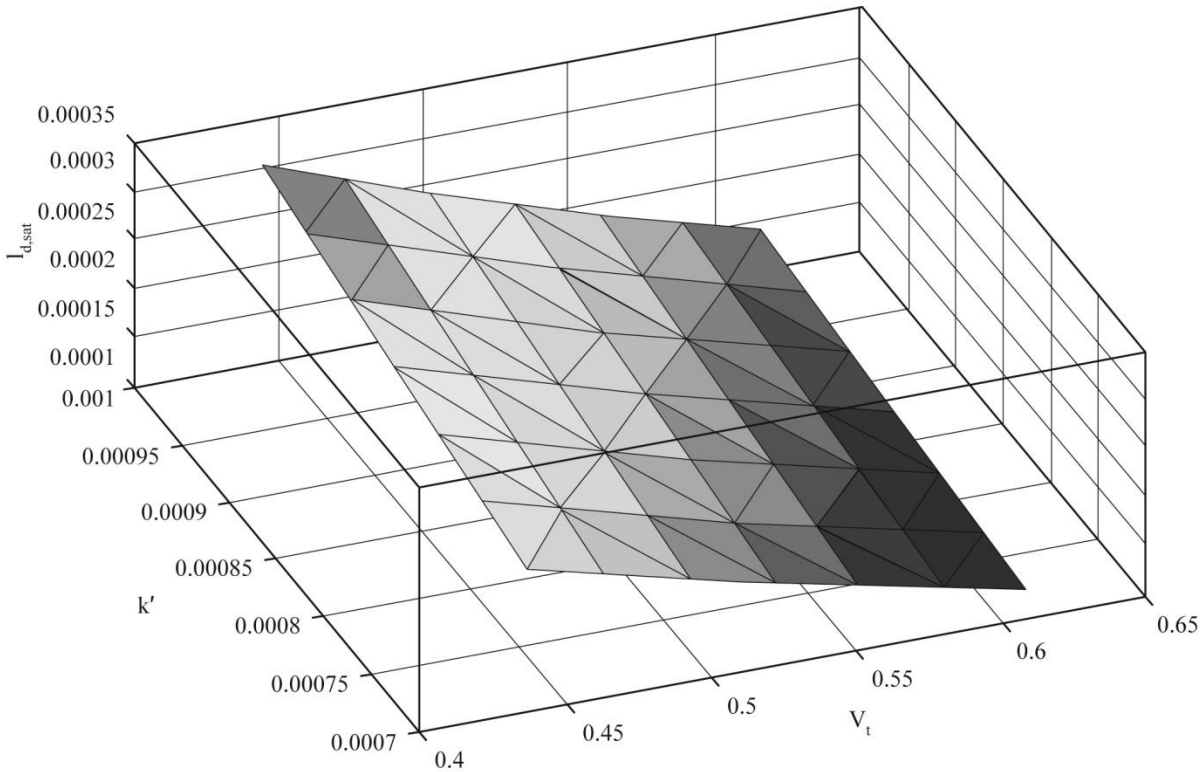
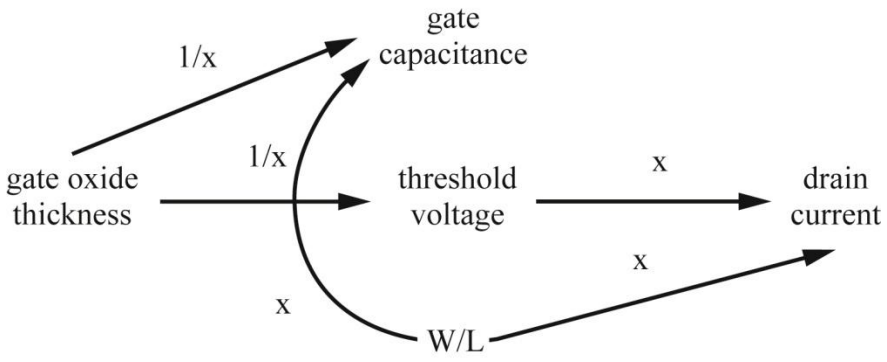


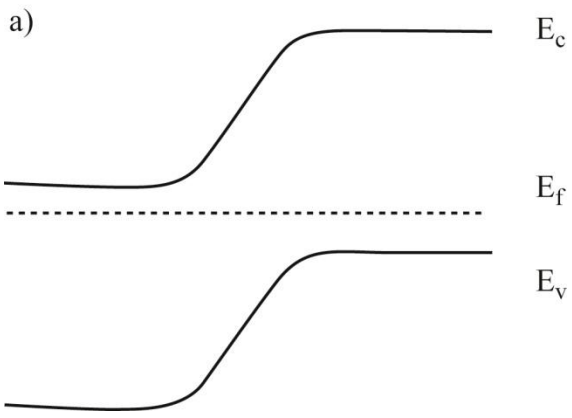
Figure 2.41: Rayleigh's criterion.



Example 2.7 Sensitivity of Id,sat



Highlight 2.7 Some of the important relationships between device parameters:



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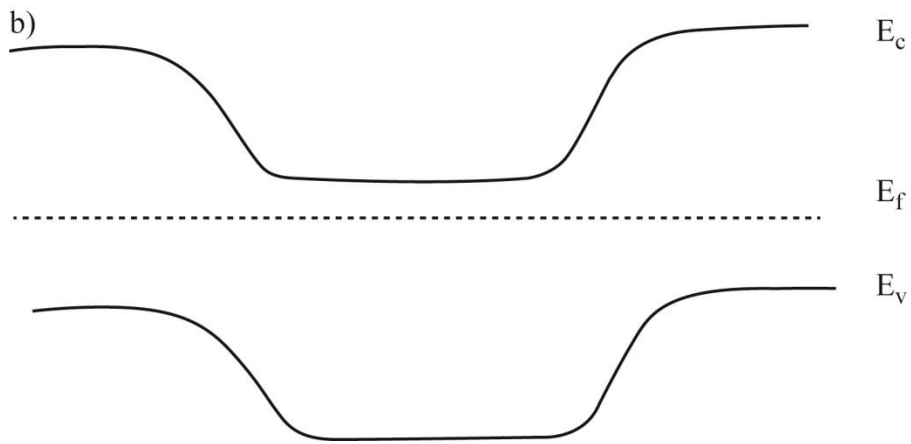

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