# Chapter 3

# Logic Gates

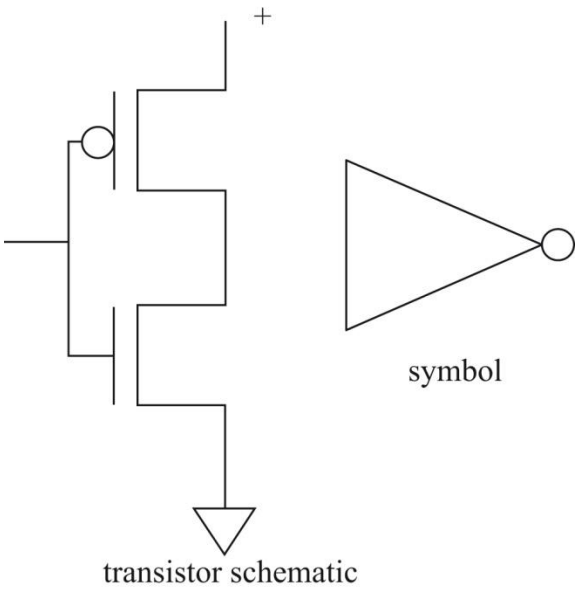



**Figure 3.1:** Schematic for a CMOS inverter.

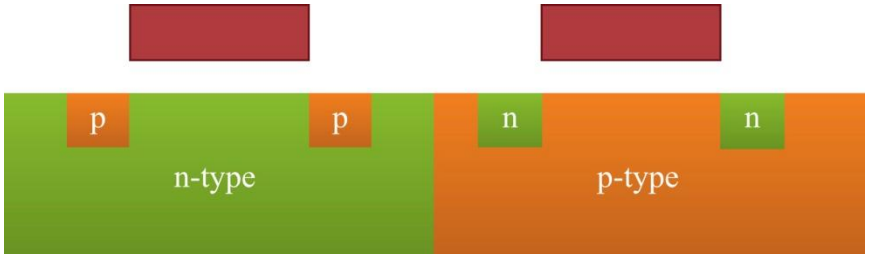



**Figure 3.2:** Cross section of twin-tub CMOS.

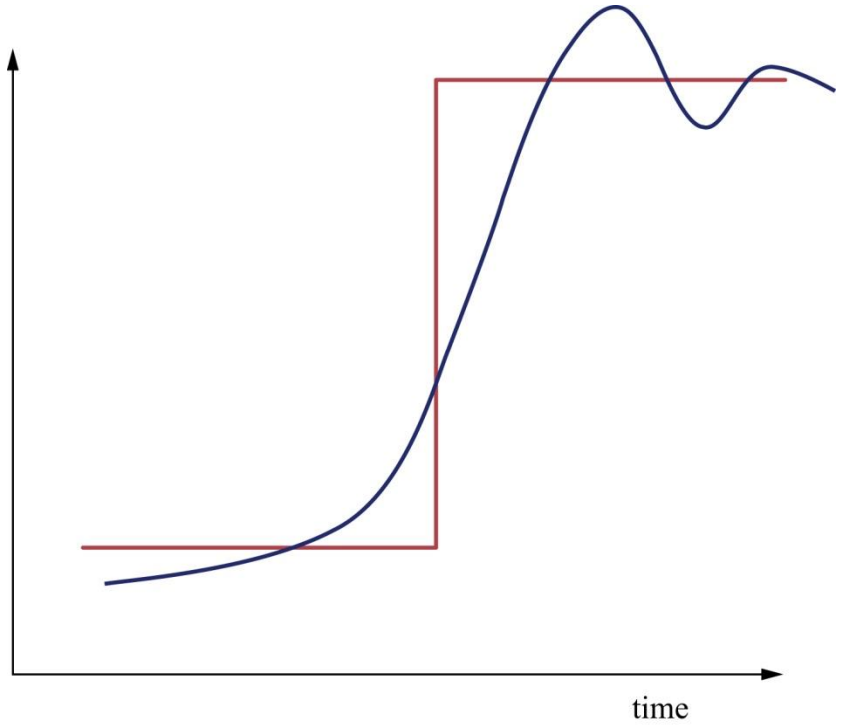



**Figure 3.3:** Waveforms and discrete values.

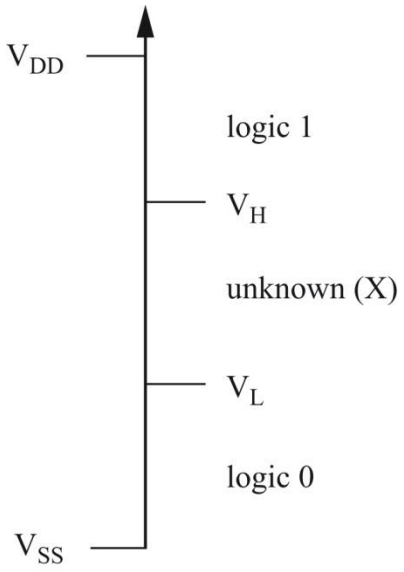



**Figure 3.4:** Voltages and logical values.

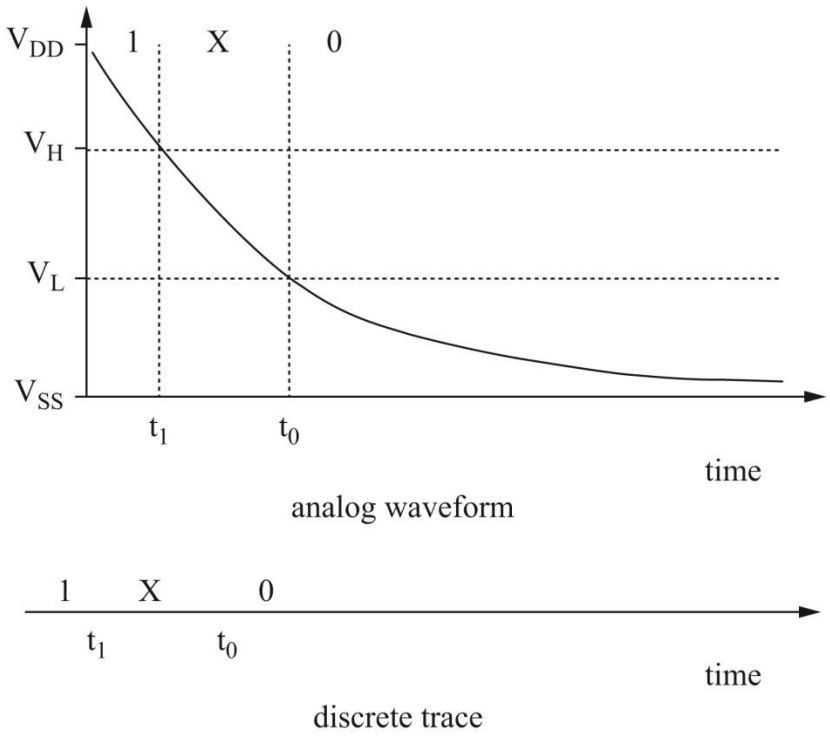



**Figure 3.5:** A waveform and its logical values.

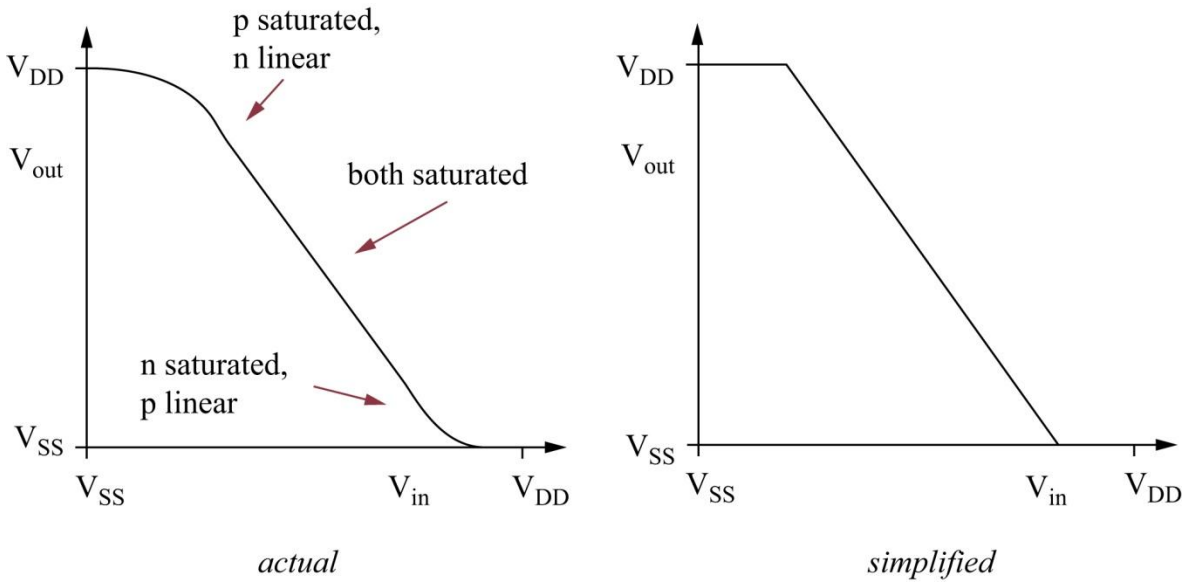



**Figure 3.6:** Voltage transfer curve for a CMOS inverter.

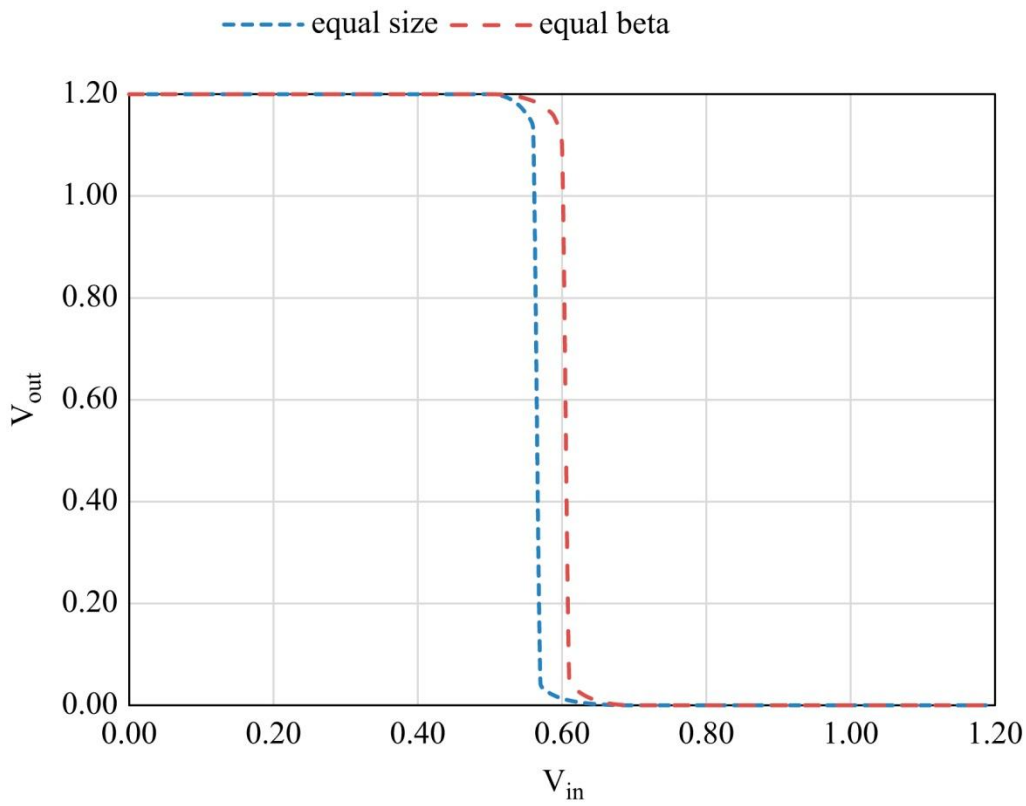



**Figure 3.7:** Transfer curves as a function of pullup size.

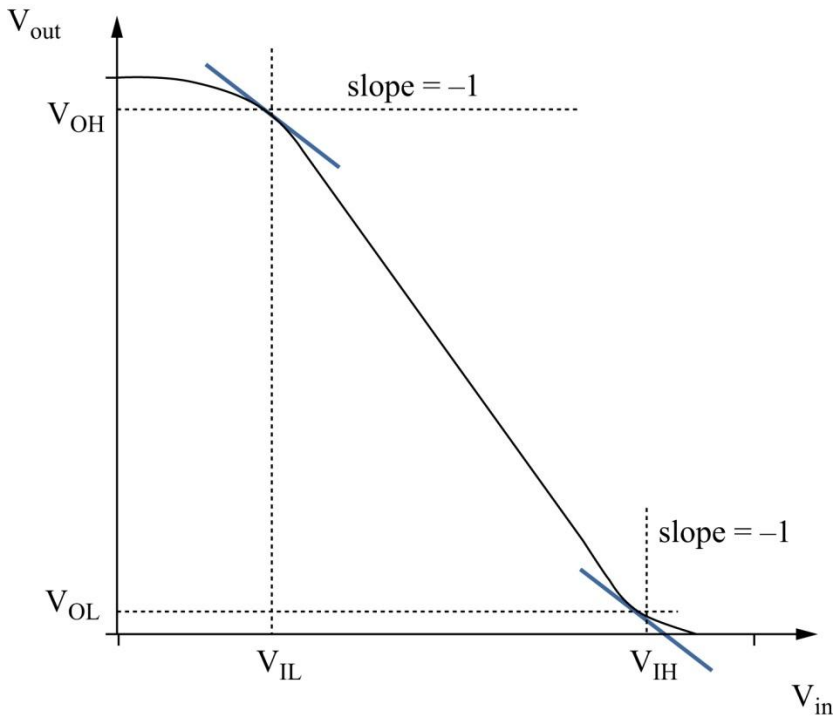



**Figure 3.8:** Choosing the voltages for logic levels.

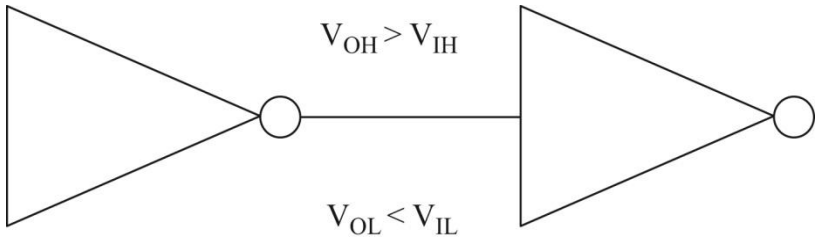



**Figure 3.9:** Compatibility of output and input voltage levels.

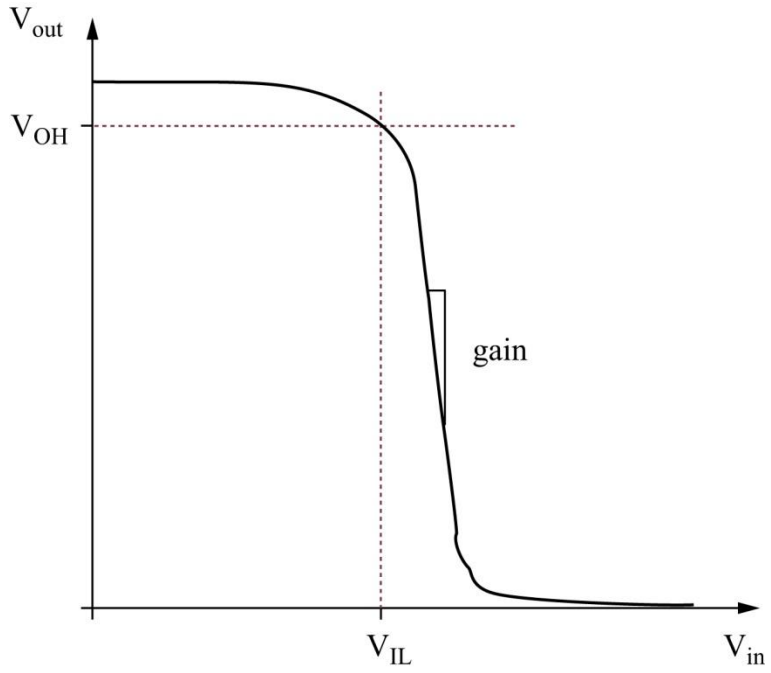



**Figure 3.10:** Gain and restoring logic values.

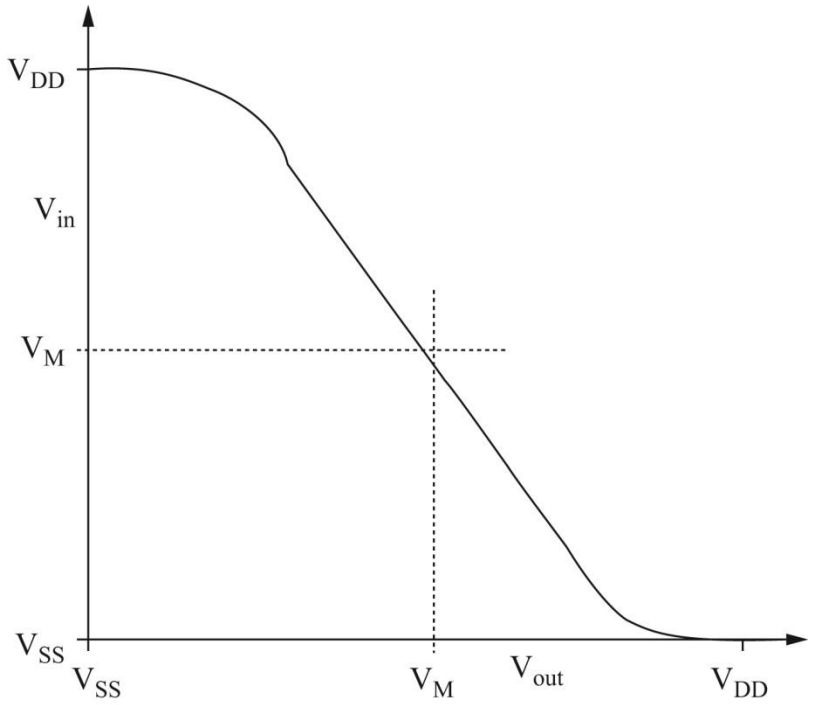



**Figure 3.9:** The middle voltage VM of the transfer characteristic.

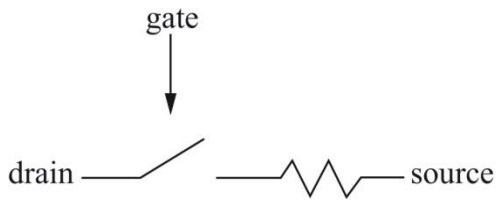



**Figure 3.12:** A simple model of a transistor.

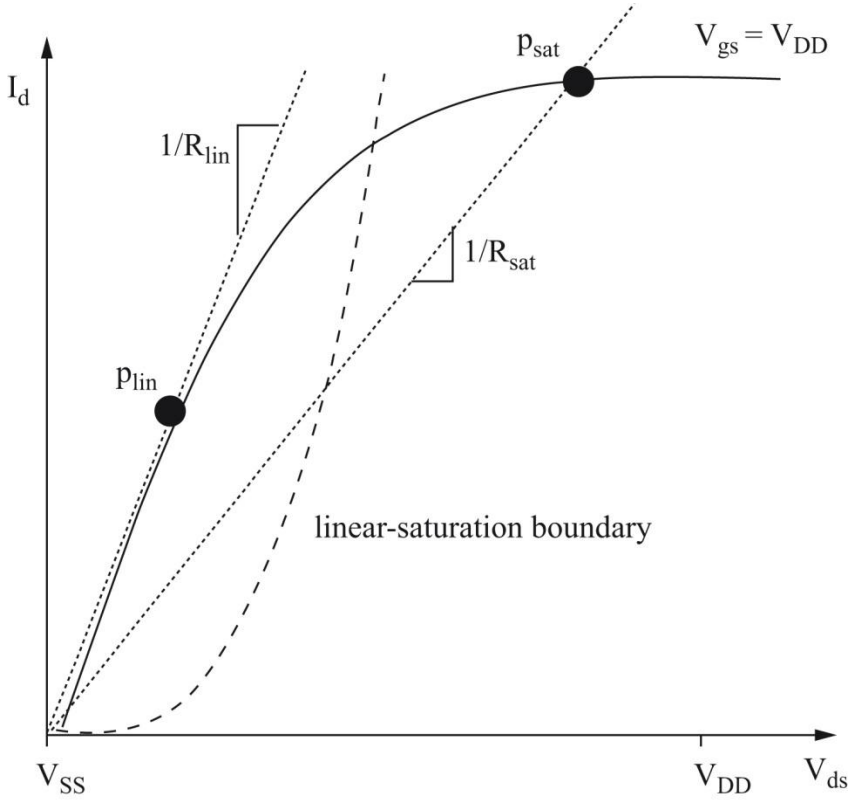



**Figure 3.13:** Resistive approximation of the transistor.

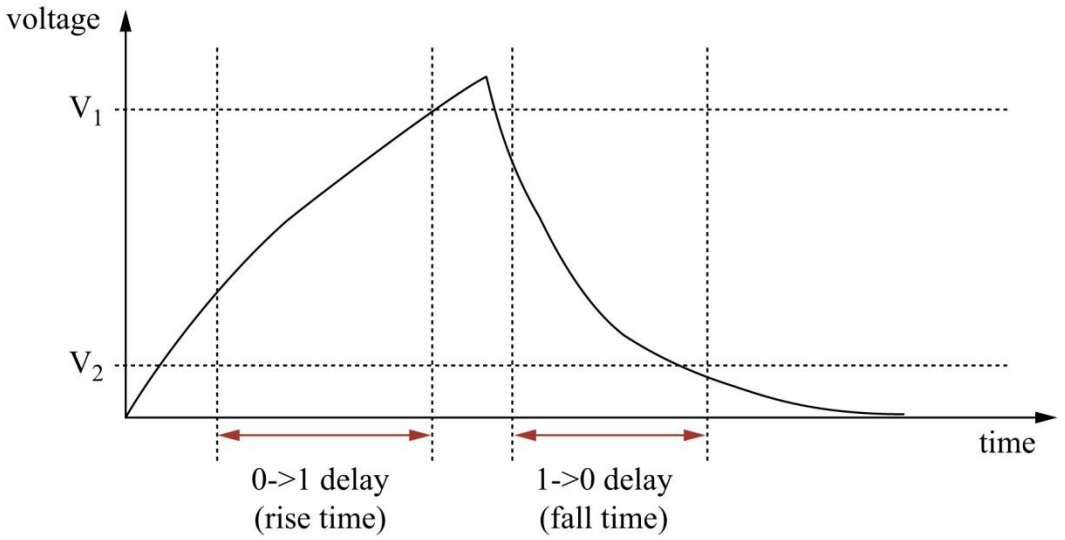



**Figure 3.14:** Measuring delay from waveforms.

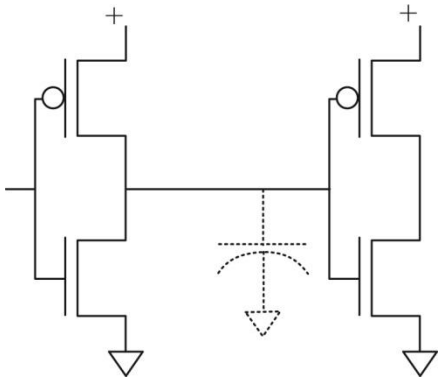


**Figure 3.15:** The capacitive load of an inverter.

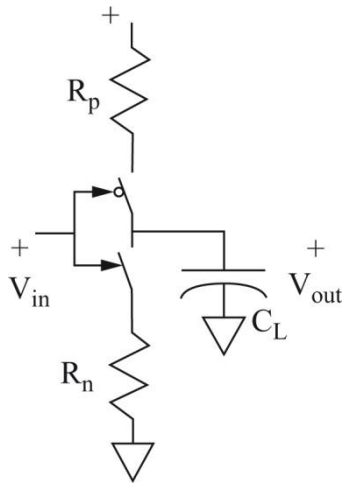



**Figure 3.16:** An inverter modeled with switched resistors.

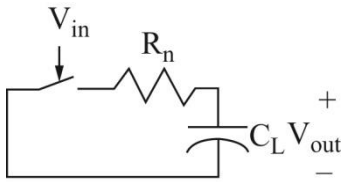



**Figure 3.17:** RC model of inverter delay.

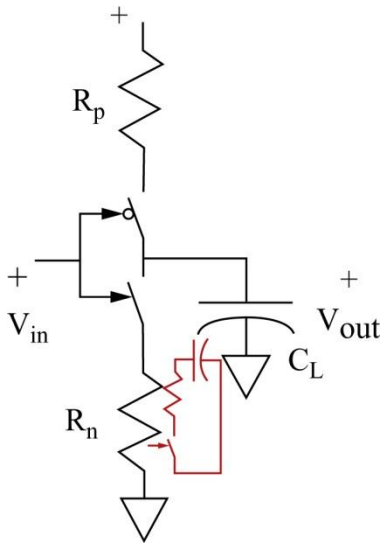



**Figure 3.18:** Relationship between the RC delay circuit and the switched resistor inverter

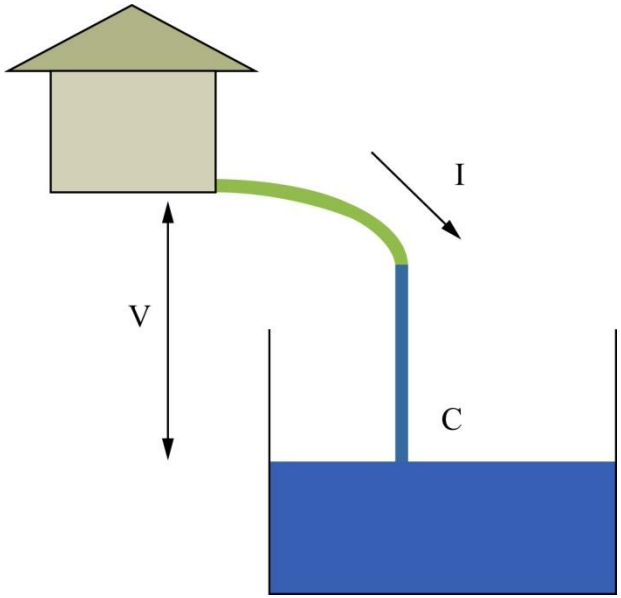



**Figure 3.19:** A water model for delay.

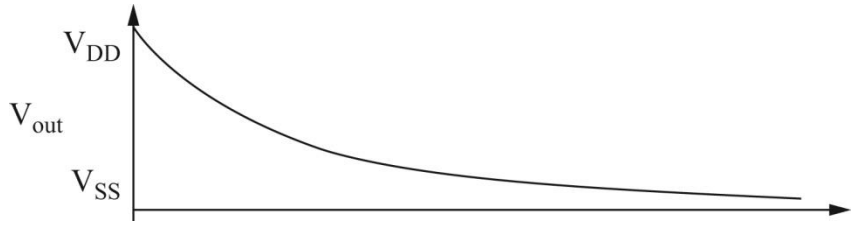



**Figure 3.20:** Output voltage waveform for fall time.

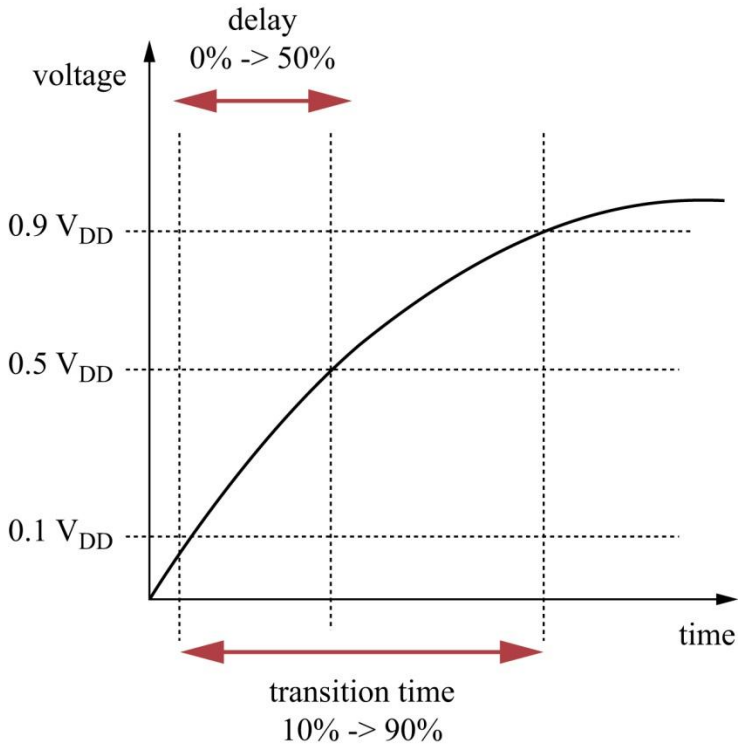



**Figure 3.21:** Definitions of delay.

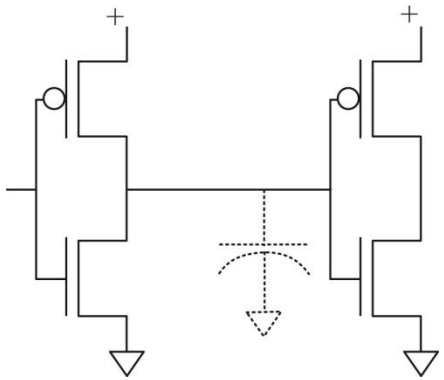


**Figure 3.22:** Drive and capacitive load.

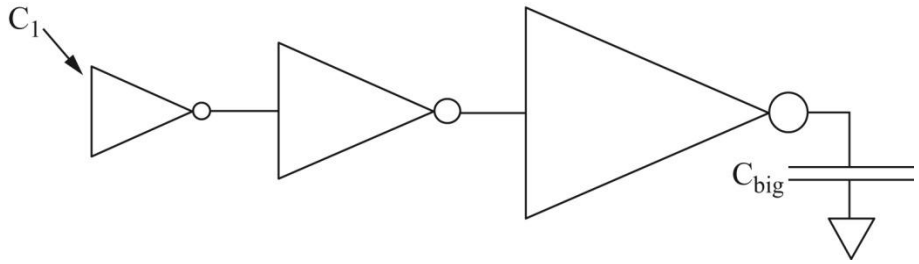



**Figure 3.23:** Driving large loads through a chain of drivers.


**Figure 3.24:** The TRS-80 Model 100 portable computer.

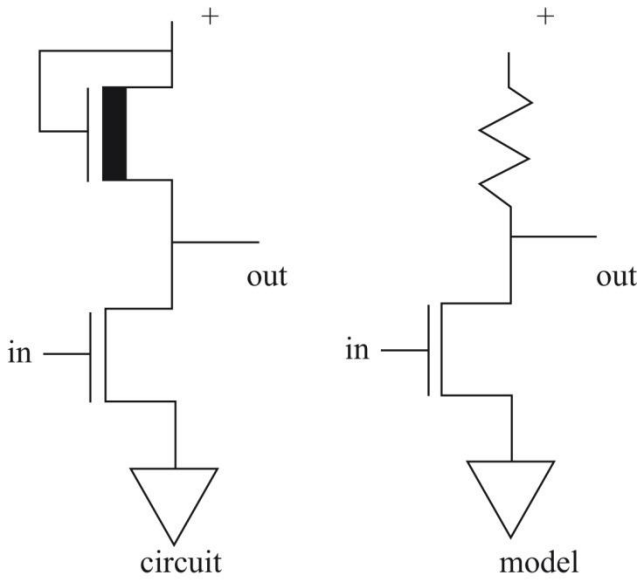



**Figure 3.25:** An nMOS inverter.

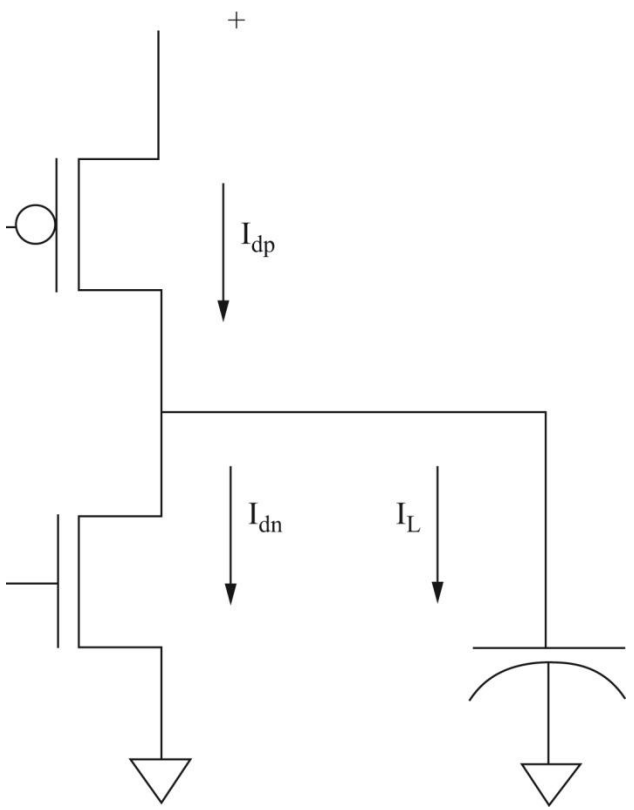



**Figure 3.26:** Short circuit current in the inverter.

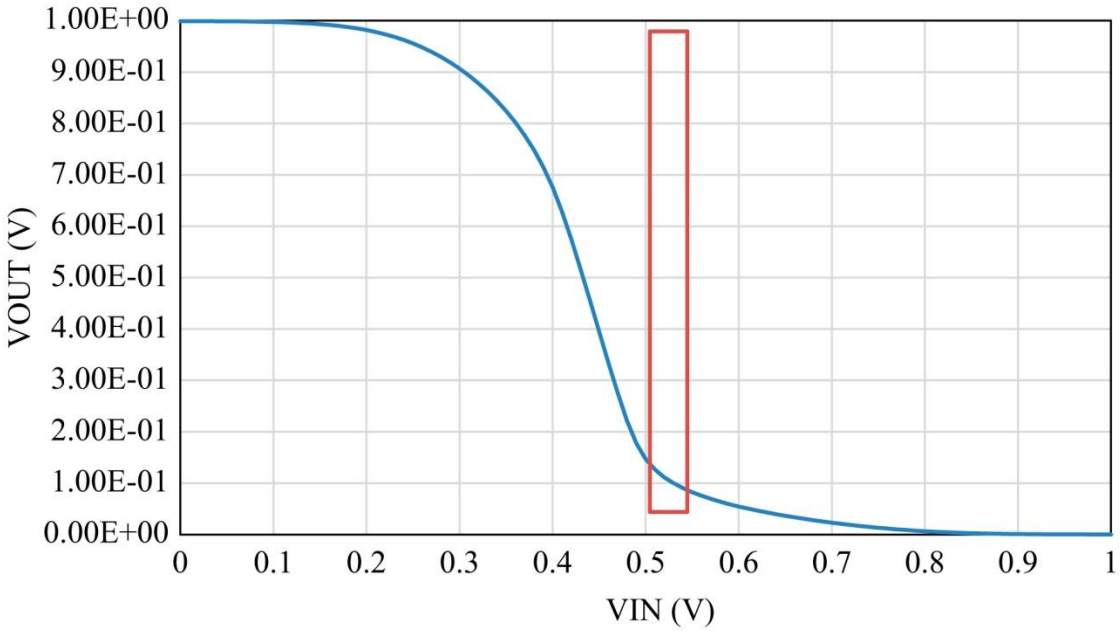



**Figure 3.27:** The short circuit region on the transfer curve.

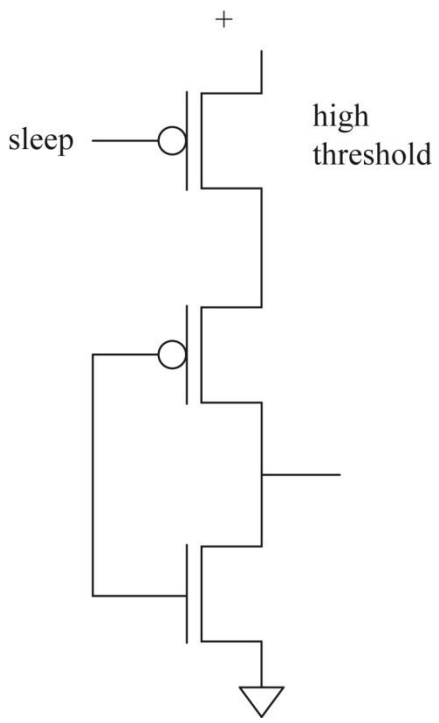



**Figure 3.28:** Power management for logic gates.

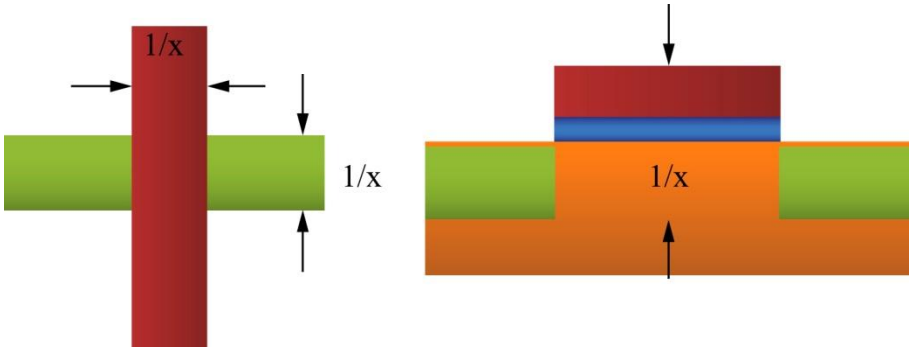



**Figure 3.29:** Dennard et al.'s model for transistor scaling.

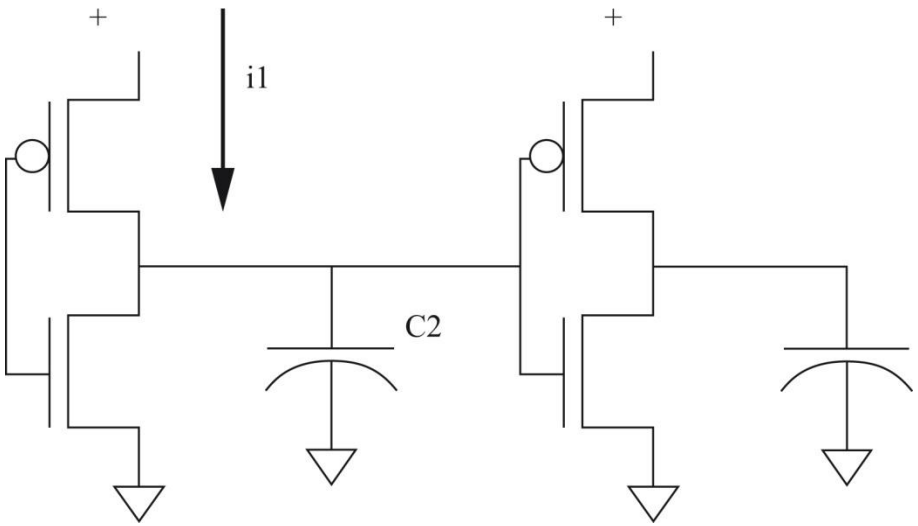



**Figure 3.30:** Loads and drive currents.

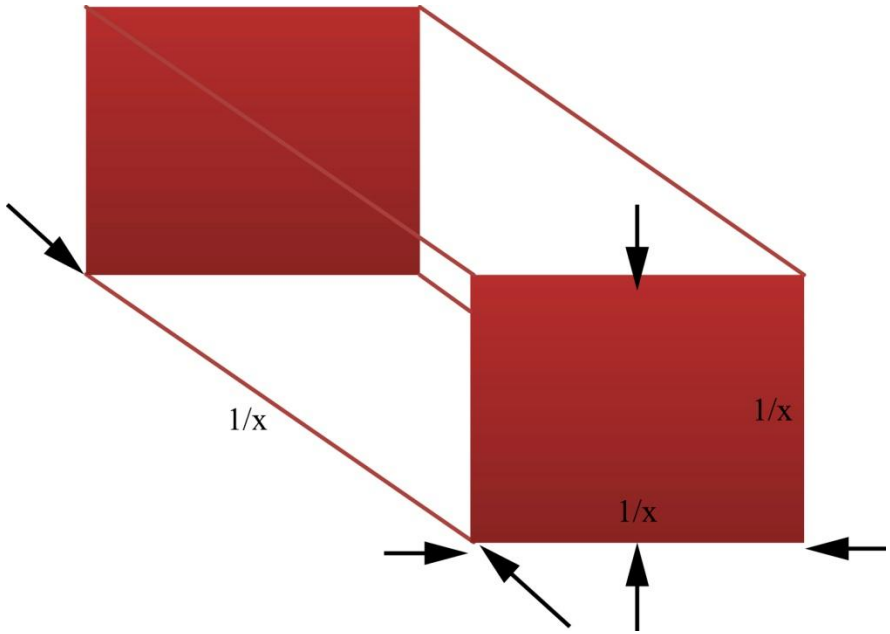



**Figure 3.31:** Dennard's model for wire scaling.

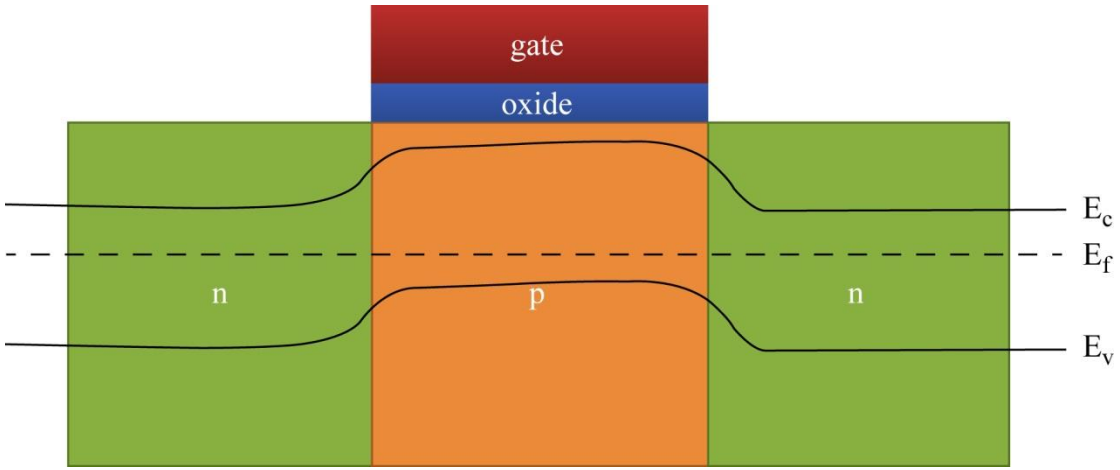
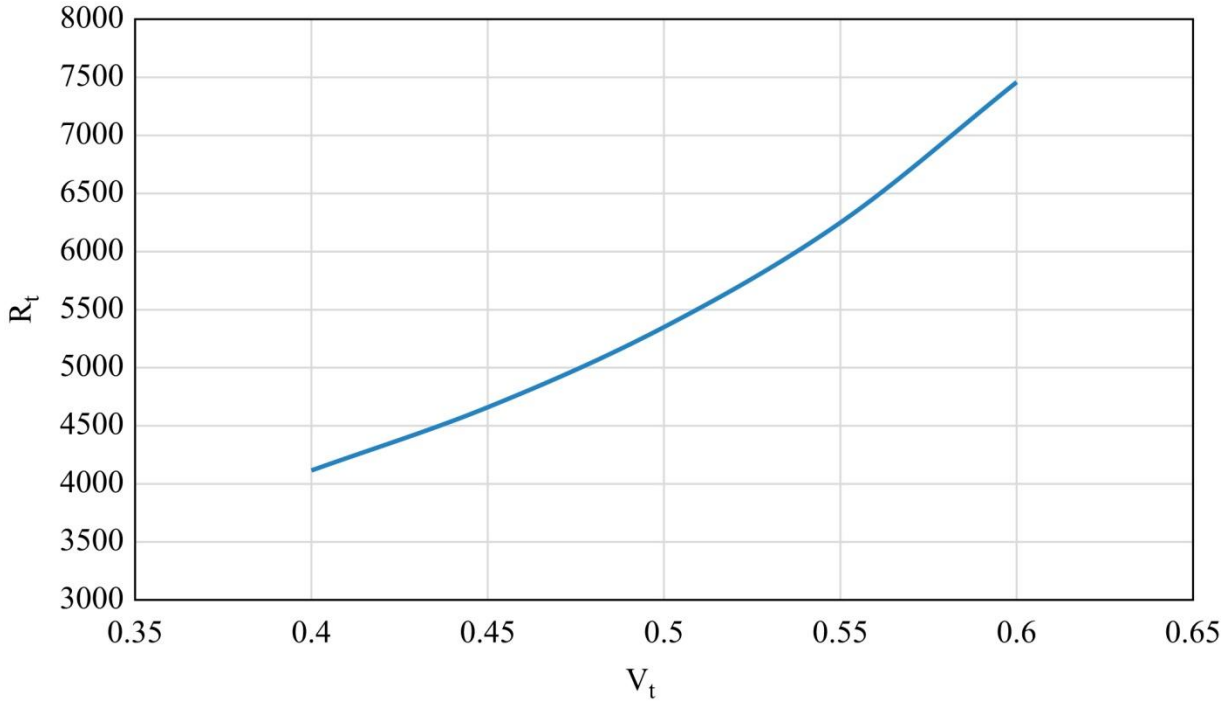
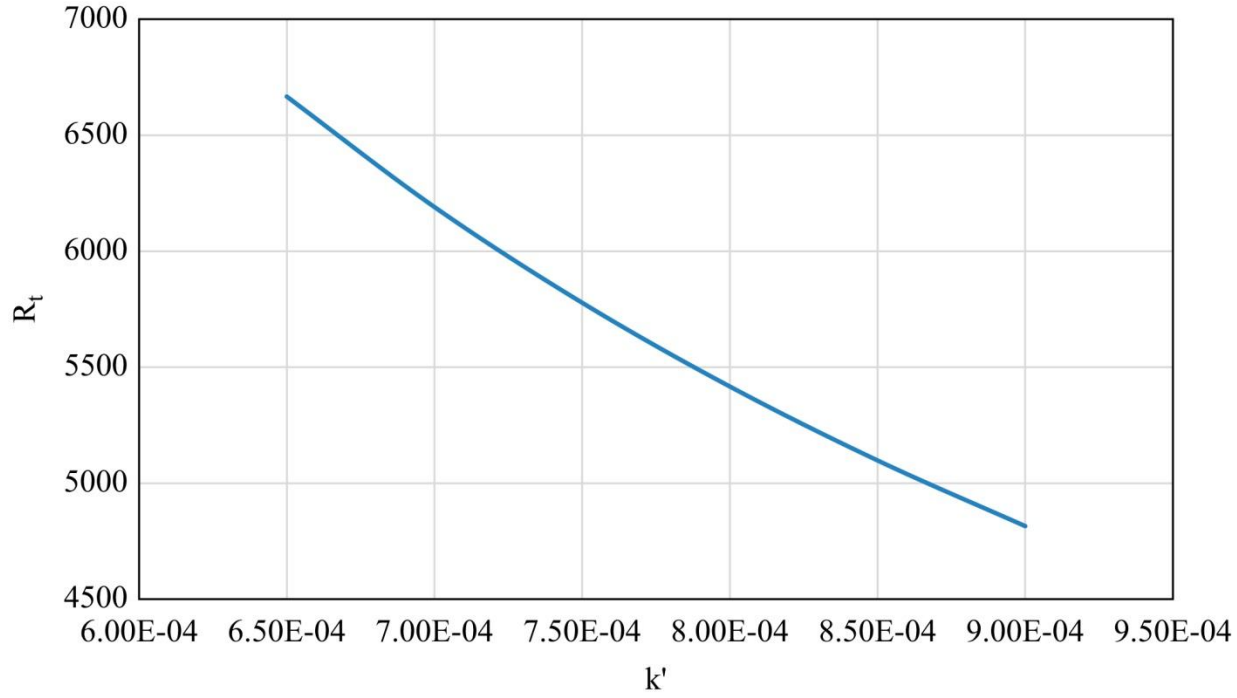


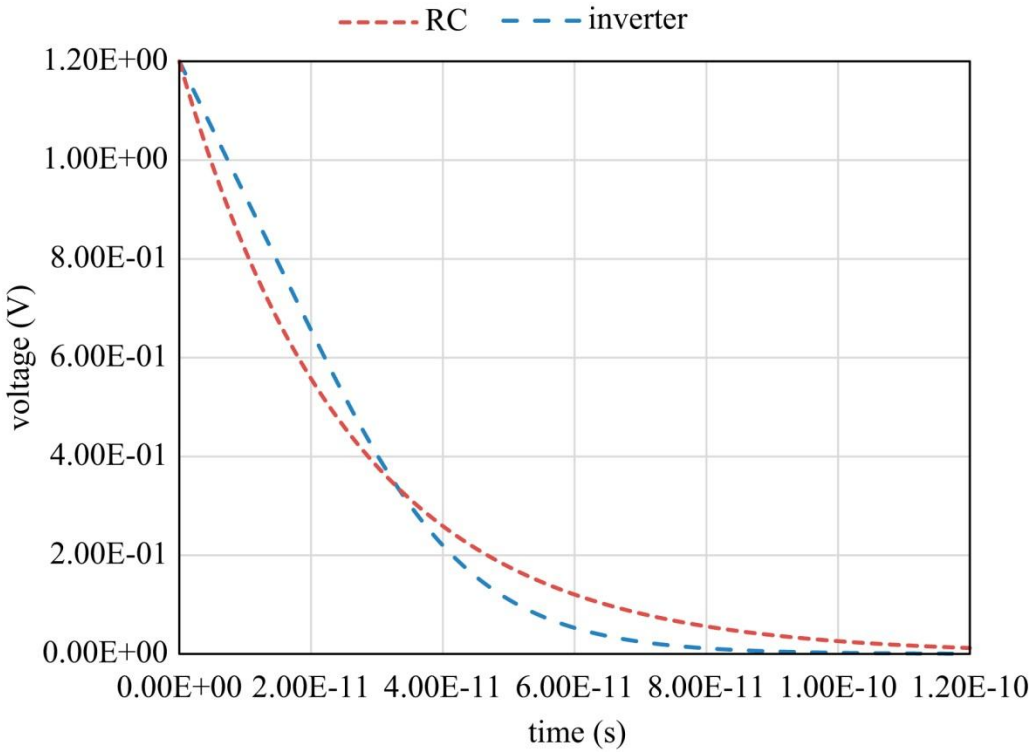

**Figure 3.32:** Energy bands in the transistor as barriers.



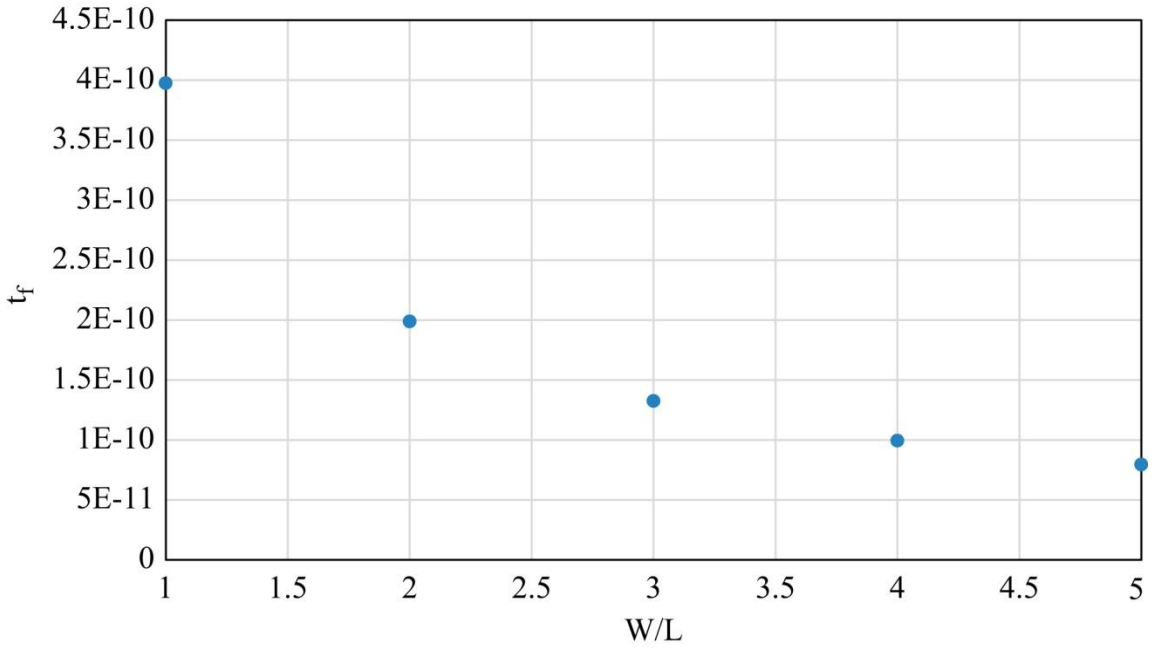

**Example 3.2** Sensitivity of Rt



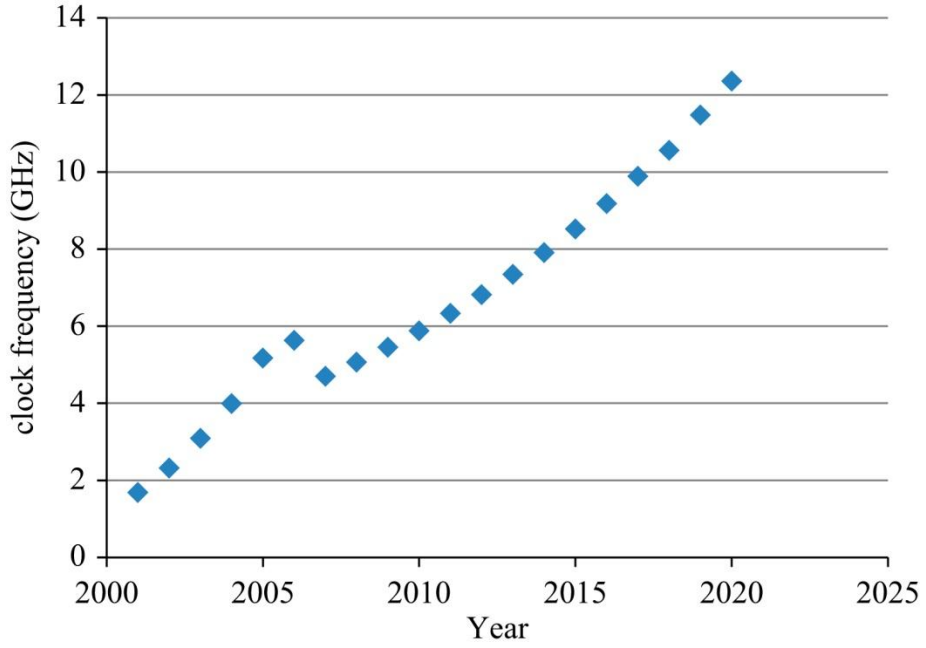

**Example 3.2** Sensitivity of Rt



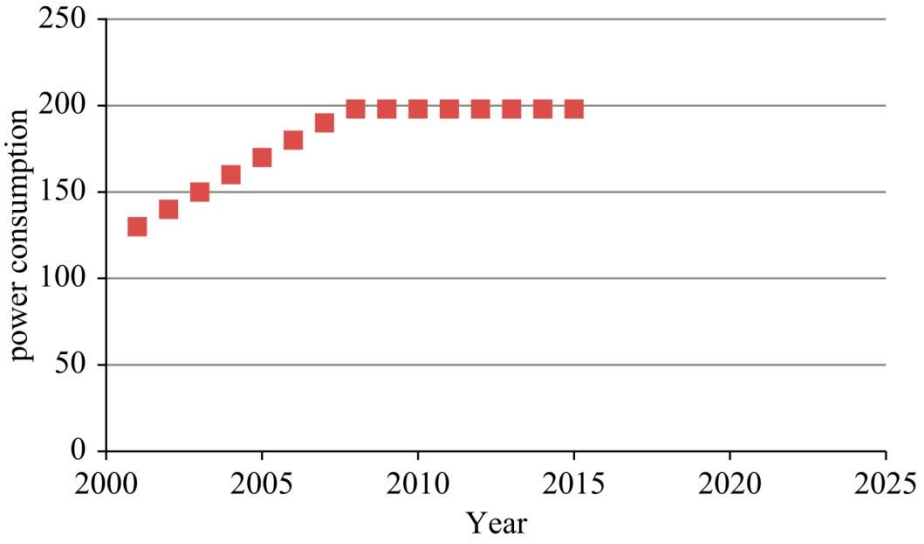

**Example 3.3** Inverter Delay.



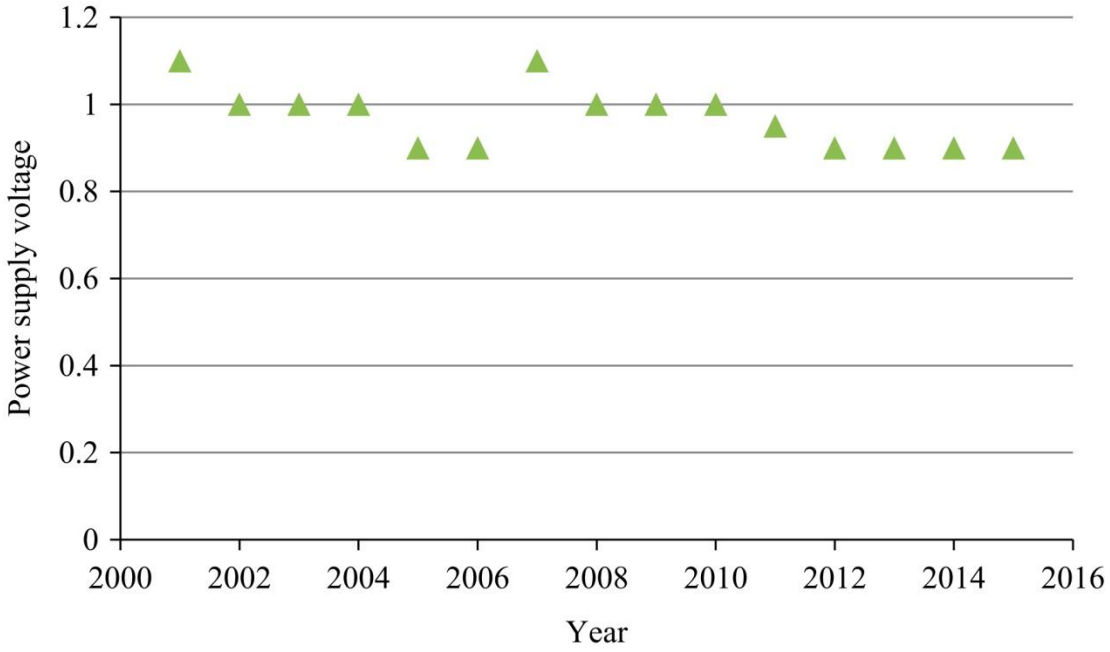

**Example 3.4** Transistor Sizing.




**Example 3.5** Scaling in Practice




**Example 3.5** Scaling in Practice




**Example 3.5** Scaling in Practice