Chapter 4

Sequential Machines

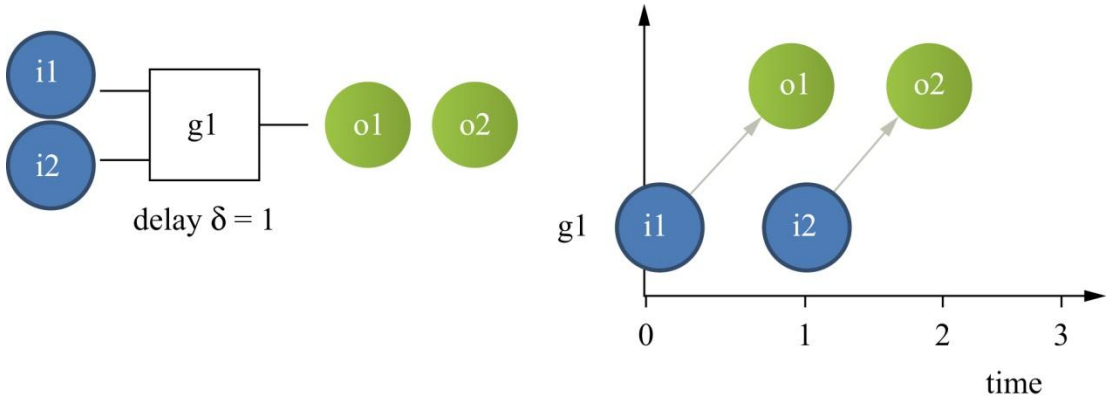


Figure 4..1: Events on a gate.

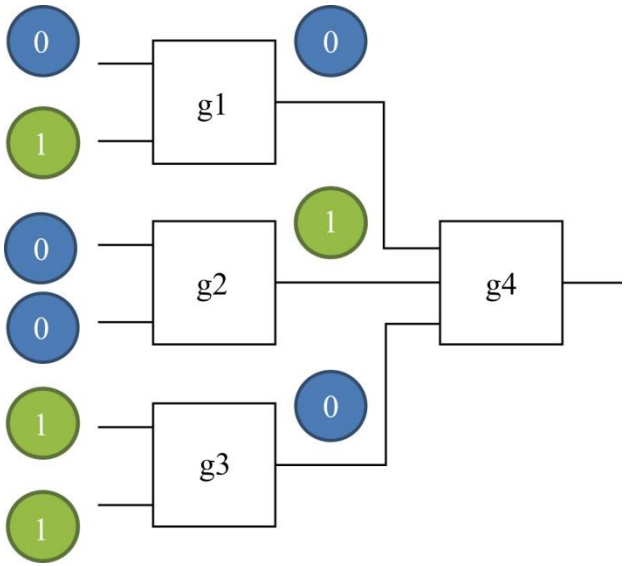


Figure 4..2: Discrete values in combinational logic.

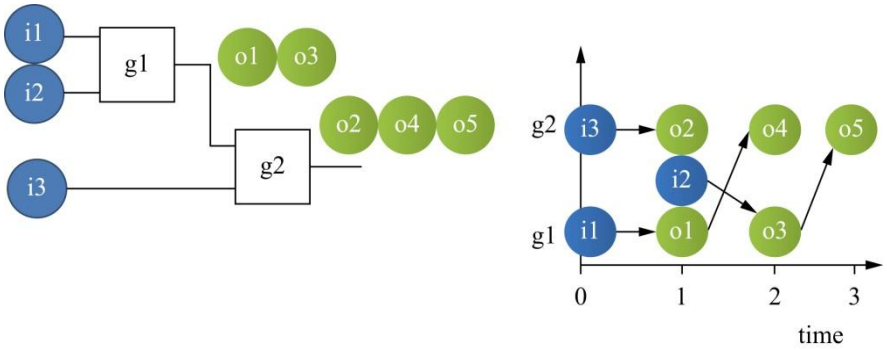


Figure 4..3: Events in a combinational network.

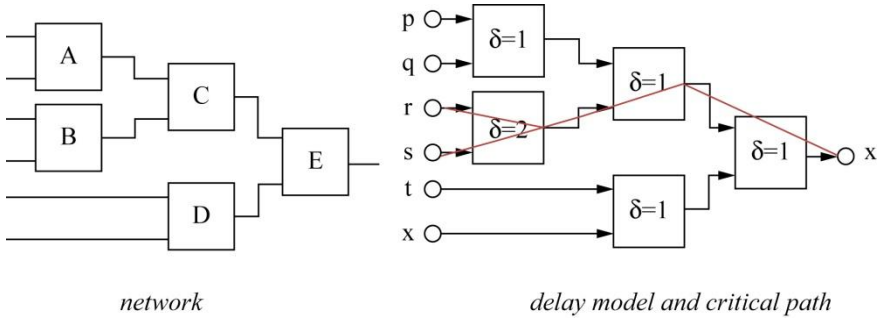


Figure 4..4: Critical delay paths.

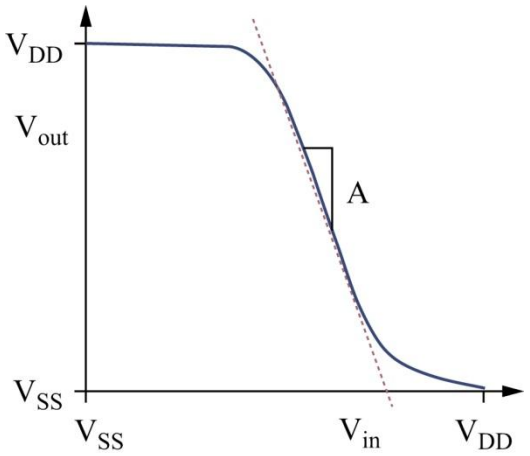


Figure 4..5: Inverter gain from the transfer curve.

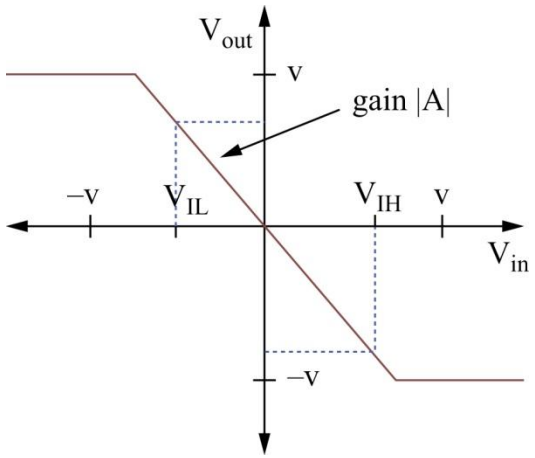


Figure 4..6: Gain and logic levels.

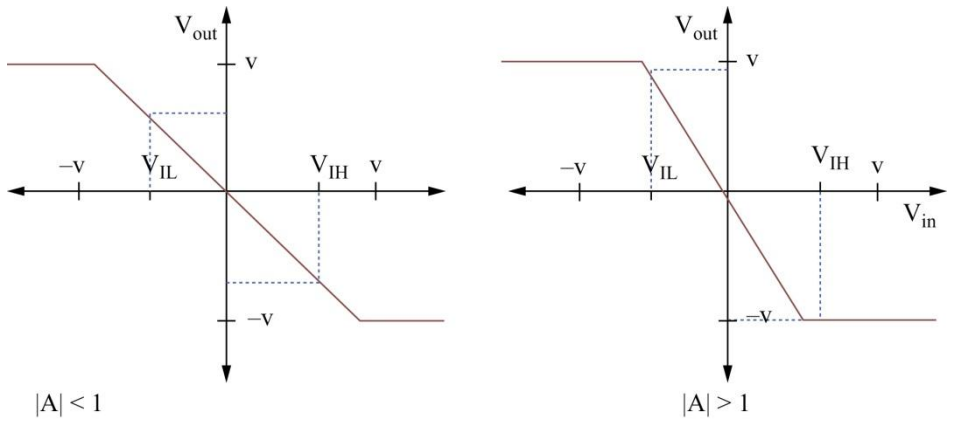


Figure 4..7: Effects of high and low gain on signal levels

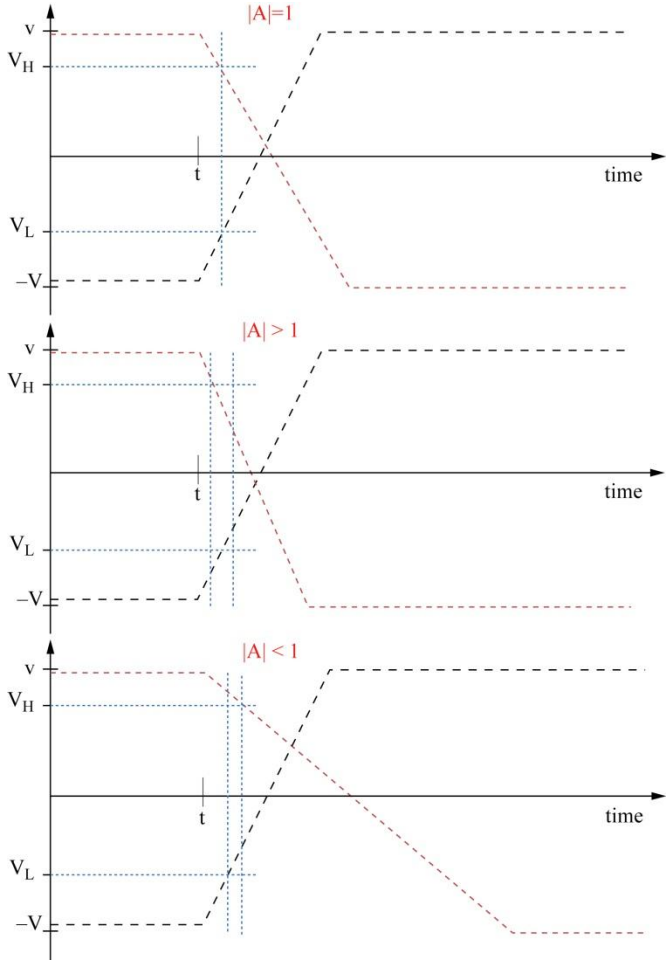


Figure 4..8: Ramp response of an inverter.

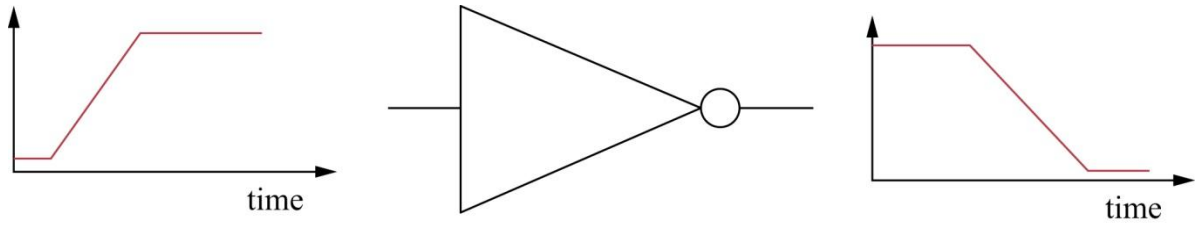


Figure 4..9: Nonideal waveforms.

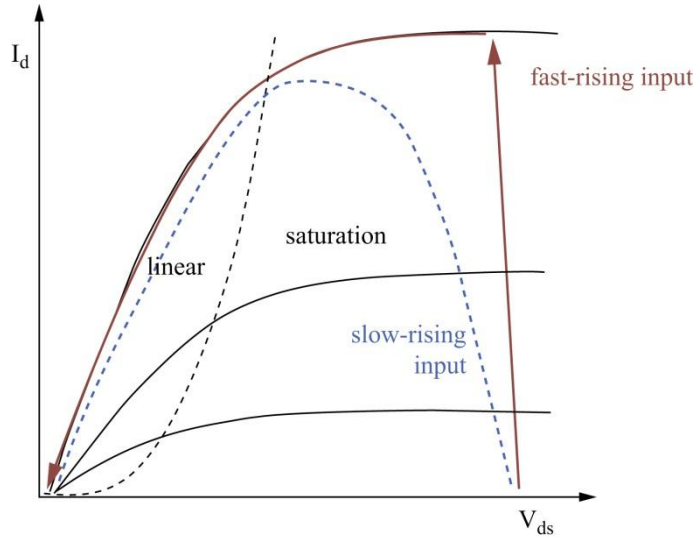


Figure 4.10: Trajectory of transistor current during fast- and slow-rising inputs.

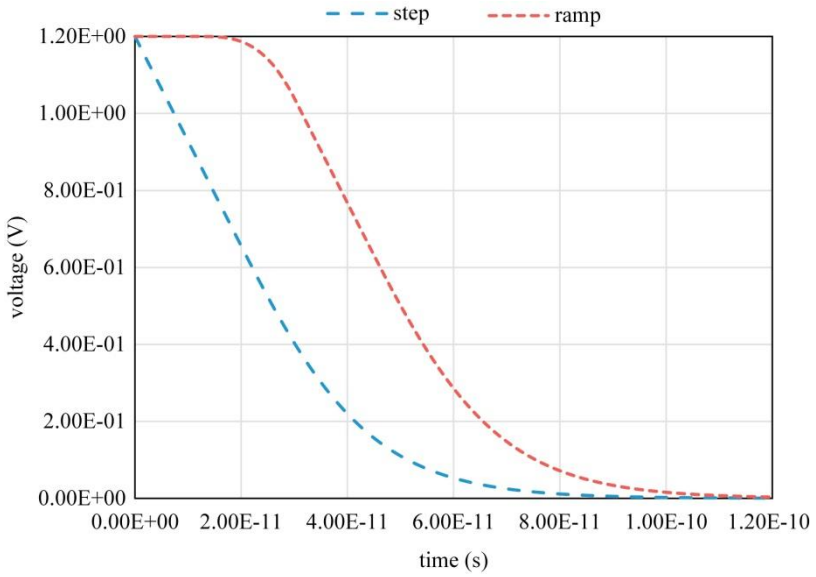


Figure 4.11: Voltage waveform for step and ramp inputs.

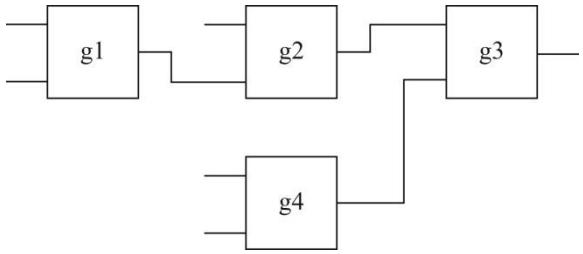


Figure 4.12: Effects of slowing down gates on the critical path.

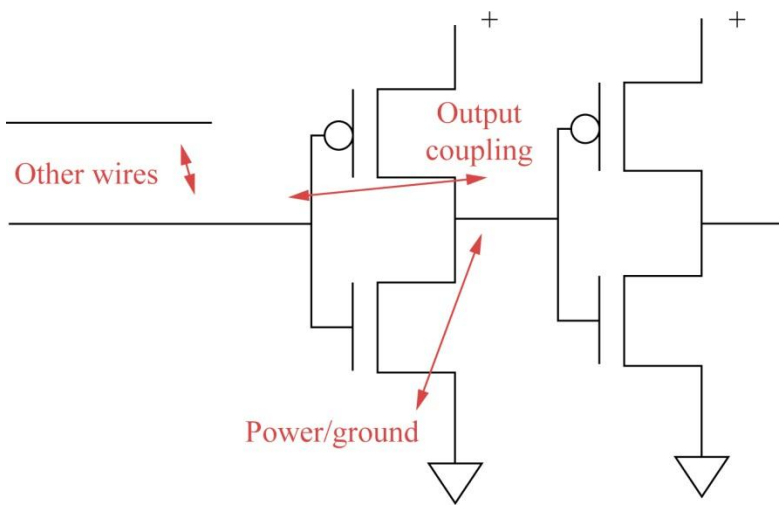


Figure 4.13: A mechanical governor.

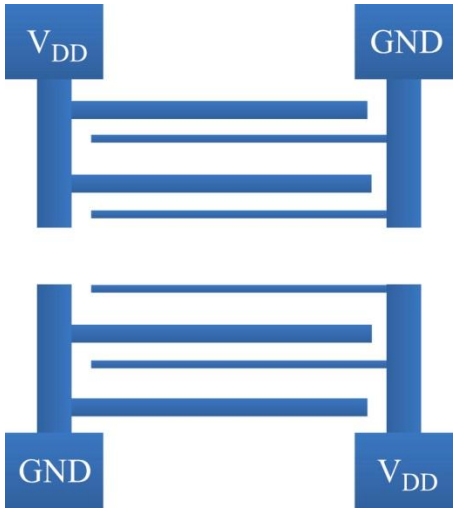


Figure 4.14: A mechanical governor.

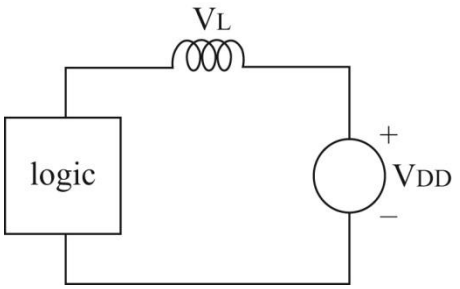


Figure 4.15: A mechanical governor.

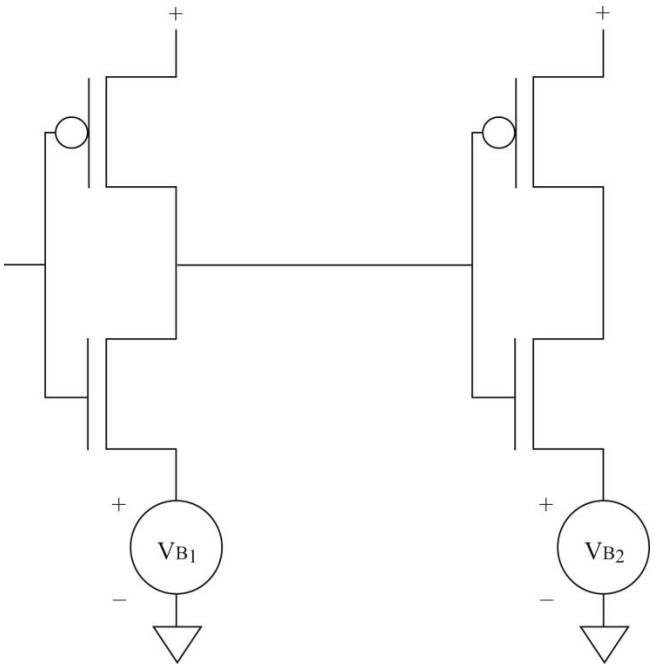


Figure 4.16: Circuit model for ground bounce and logic gates.

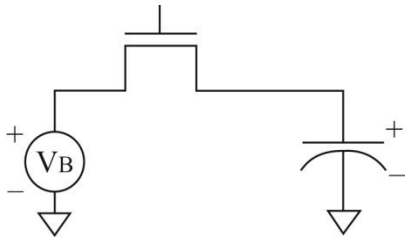


Figure 4.17: Circuit model for ground bounce and current.

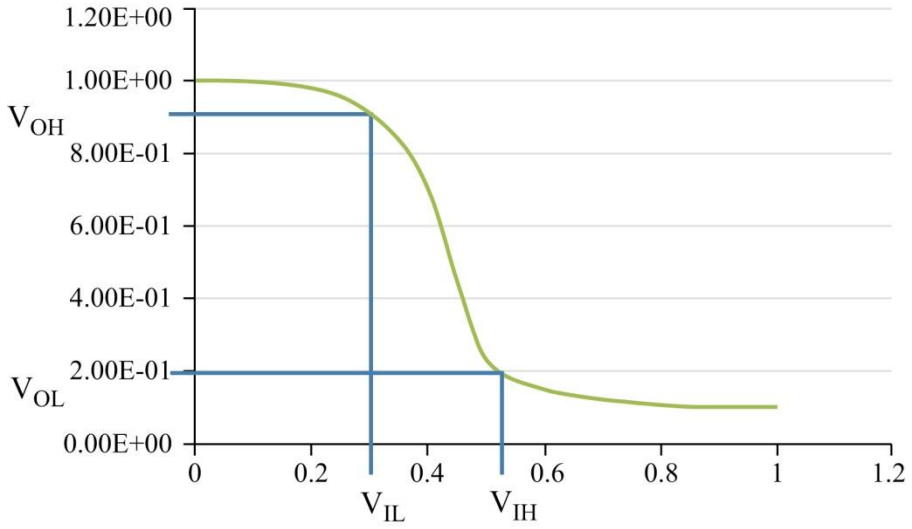


Figure 4.18: The effect of ground bounce on the gate transfer characteristic.

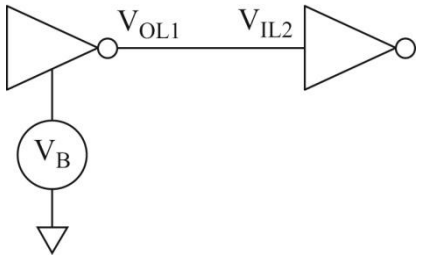


Figure 4.19: Effect of ground bounce on gate-to-gate communication.

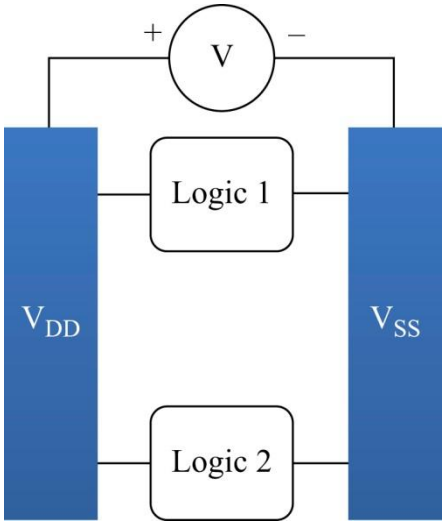


Figure 4.20: Logic blocks and current demands.

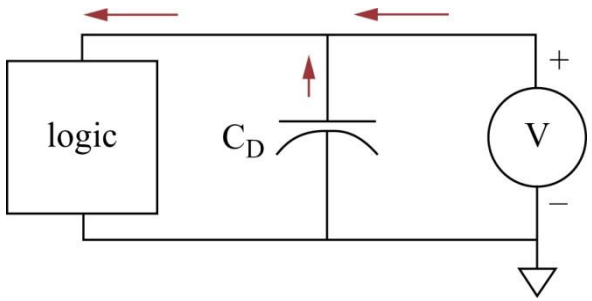


Figure 4.21: A decoupling capacitor for the power supply wiring.

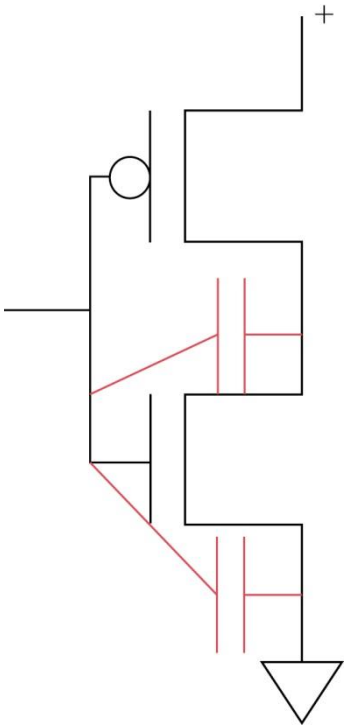


Figure 4.22: Coupling between the input and output of an inverter.

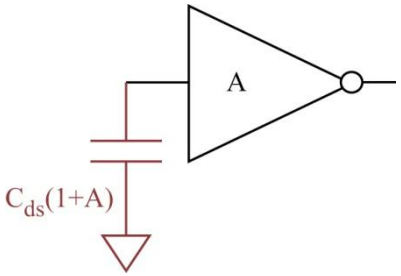


Figure 4.23: Miller capacitance.

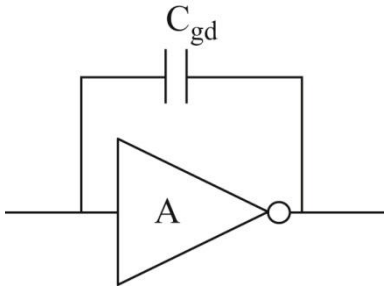


Figure 4.24: Gate/substrate and Miller capacitances.

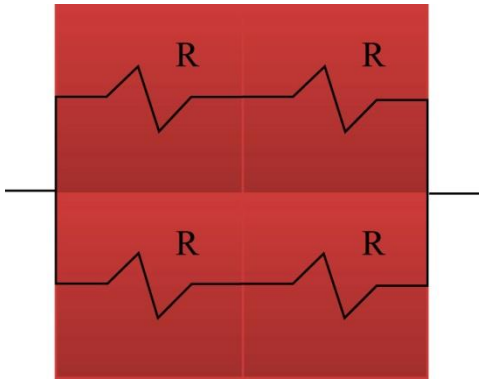


Figure 4.25: Resistance of squares is independent of square dimensions.

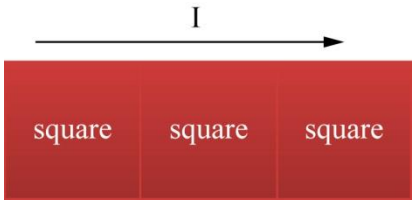


Figure 4.26: Wire resistance is measured along the direction of current flow.

Figure 4.27: A transmission line.

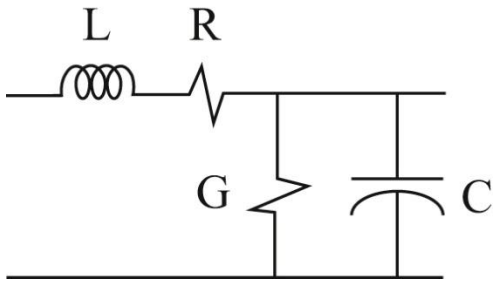


Figure 4.28: A section of an RLC transmission line.

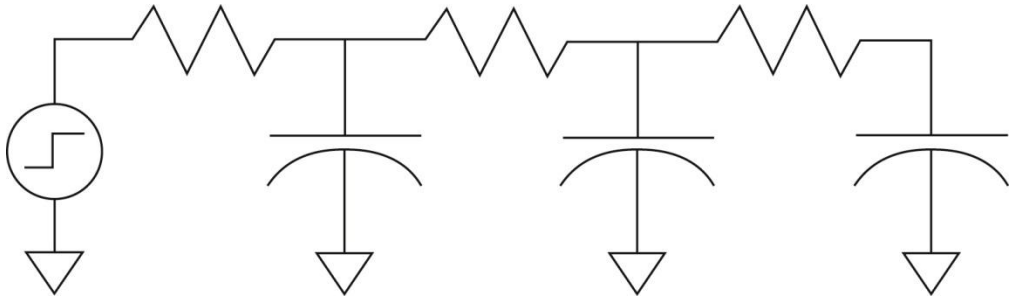


Figure 4.29: An RC transmission line.

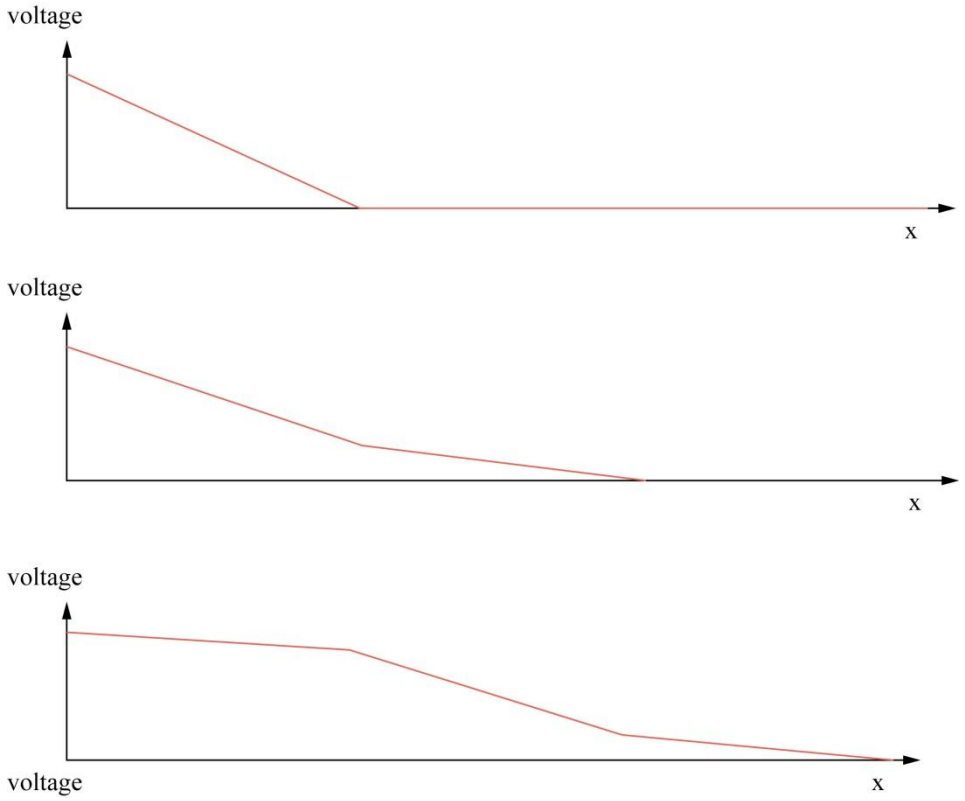


Figure 4.30: Propagation of a step input along an RC transmission line.

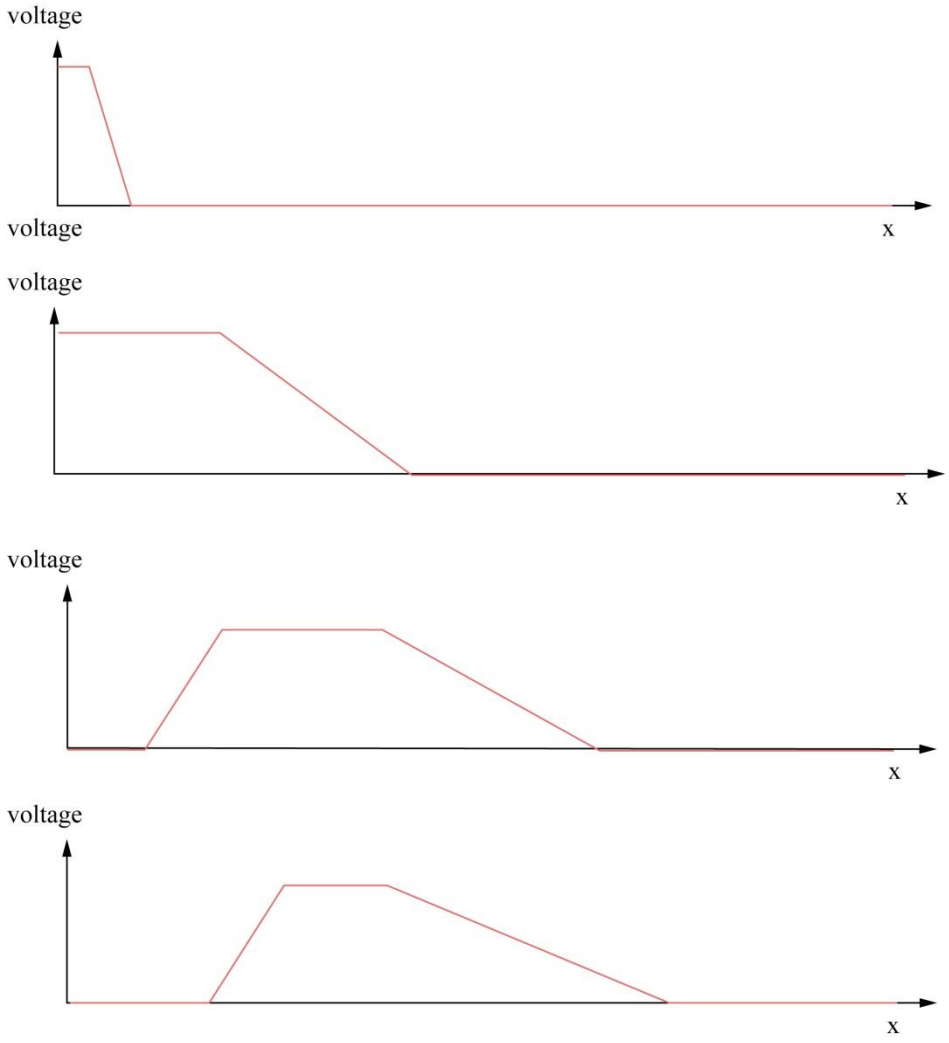


Figure 4.31: Distortion of a pulse traveling along a transmission line.

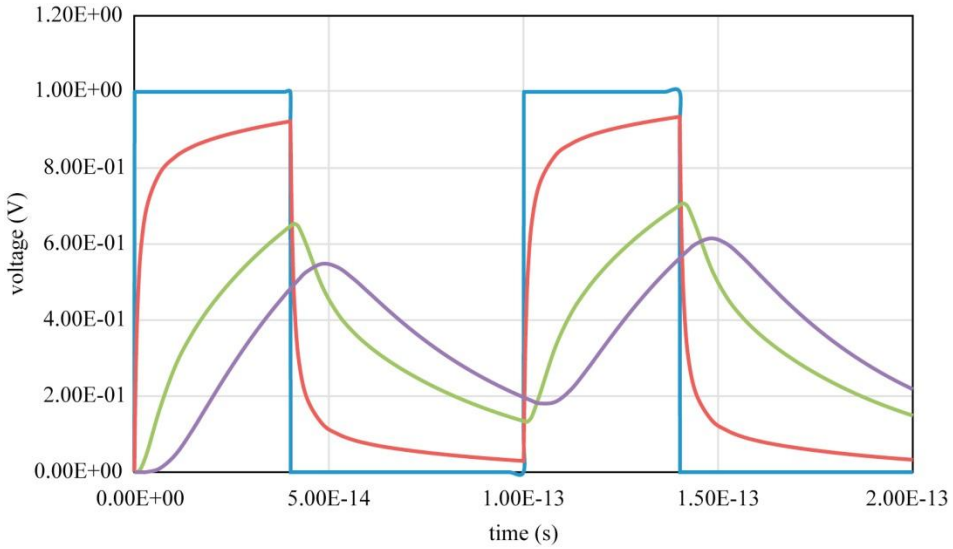


Figure 4.32: Performance of a series of RC sections.

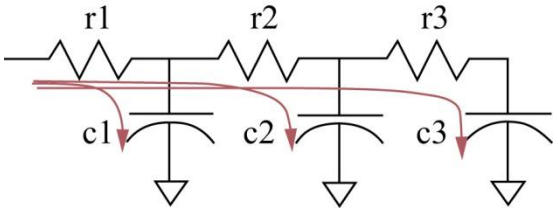


Figure 4.33: Currents in the Elmore model.

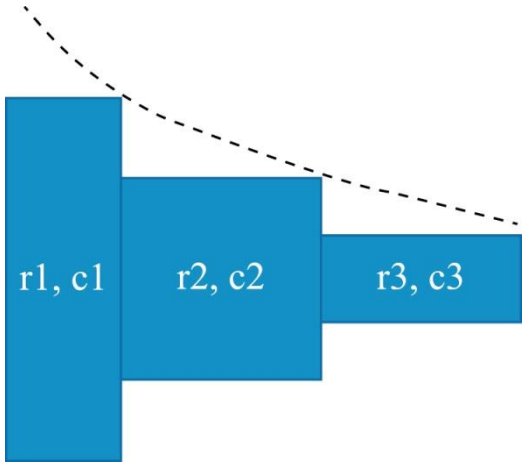


Figure 4.34: Resistance and capacitance along a nonuniform wire.

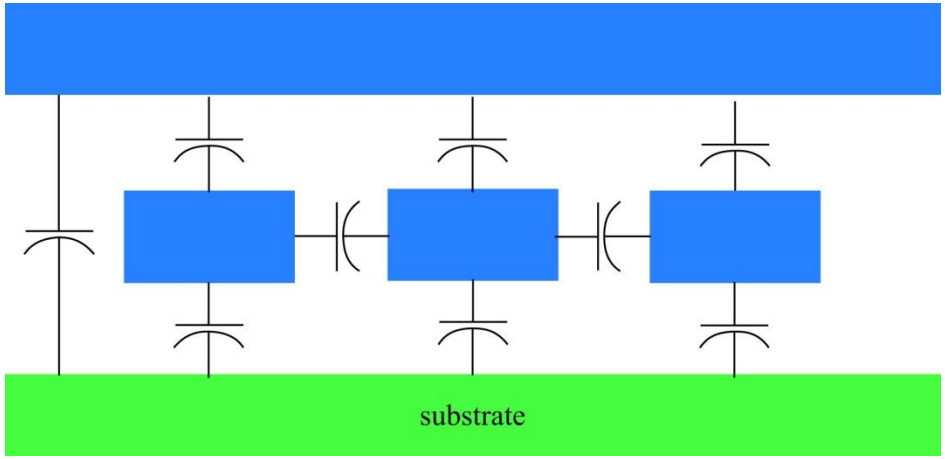


Figure 4.35: Capacitive couplings of wires.

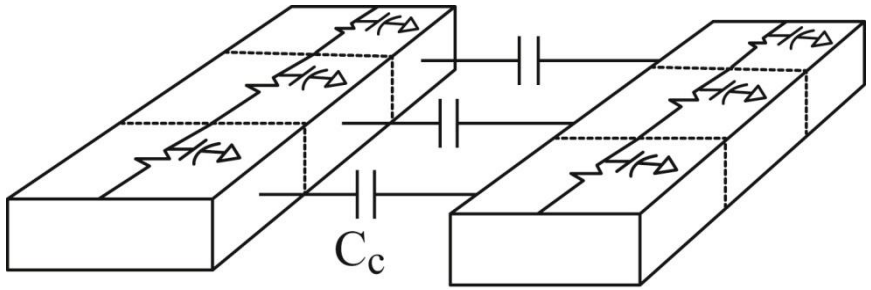


Figure 4.36: Capacitive coupling between wires..

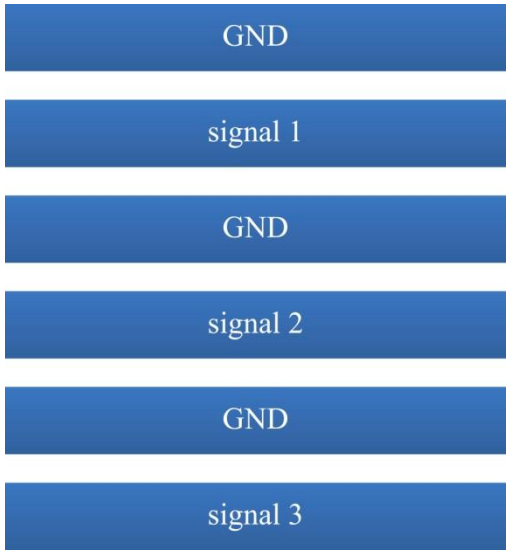


Figure 4.37: Shielded wires.

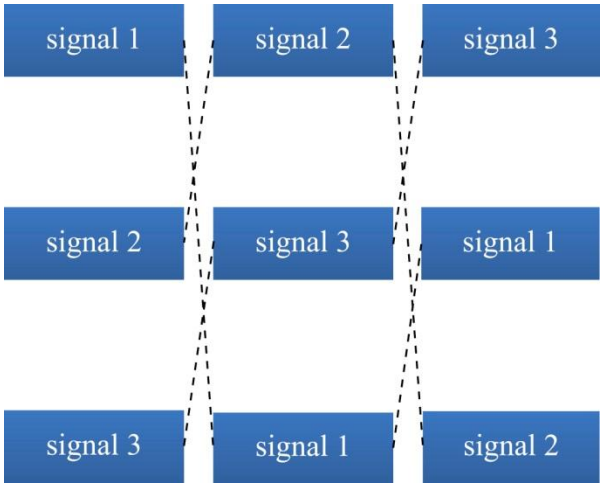


Figure 4.38: Twizzled wires.

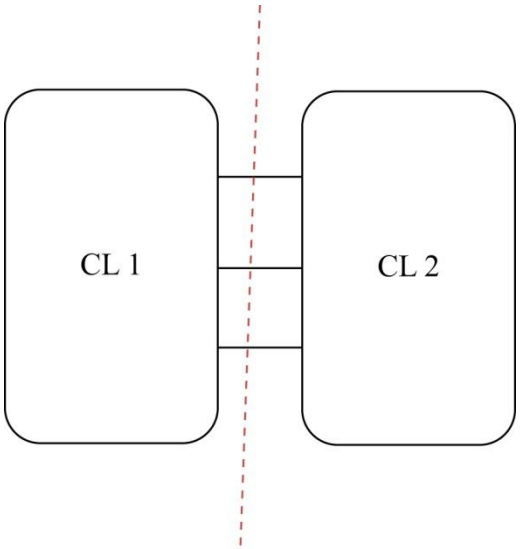


Figure 4.39: Partitioning as a measure of wiring complexity.

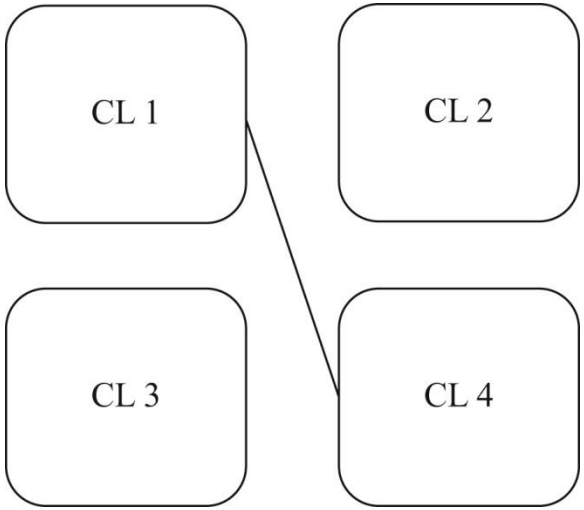


Figure 4.40: Recursive partitioning for wiring estimation.

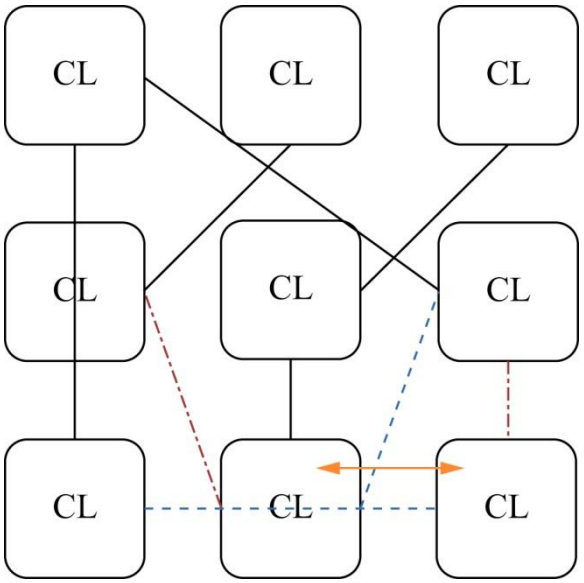


Figure 4.41: Wire length estimation by Euclidean distance.

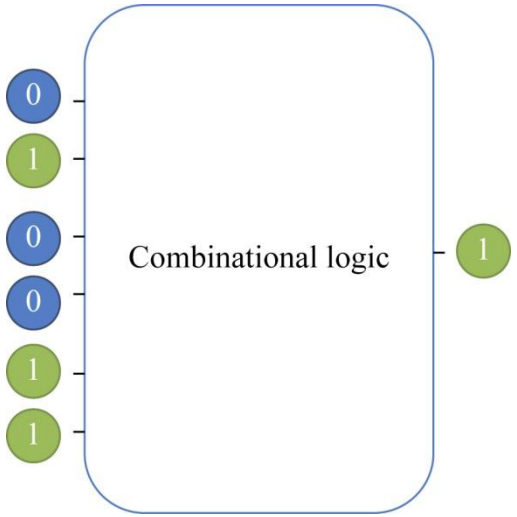


Figure 4.42: The combinational abstraction for logic.

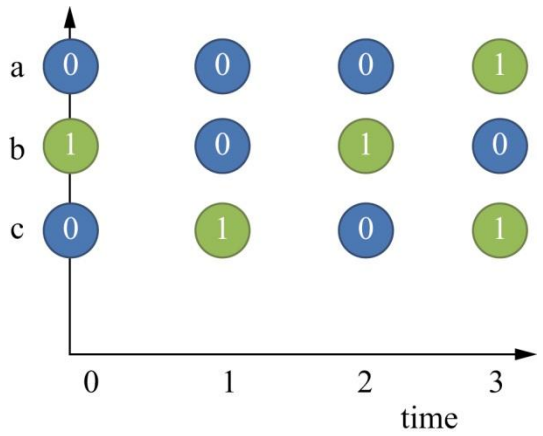


Figure 4.43: Signals in discrete time.

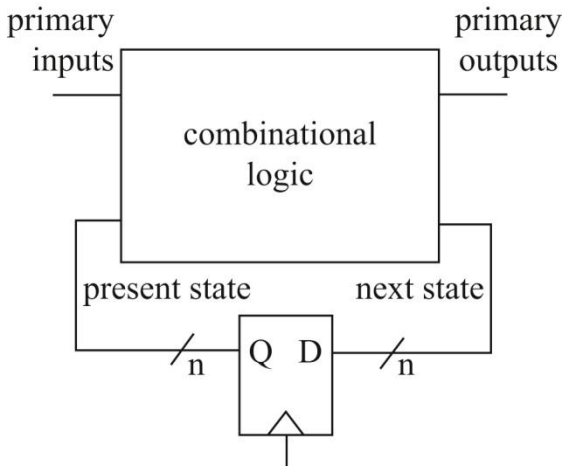


Figure 4.44: A sequential machine.

input	present state	next state	output
0	00	00	0
1	00	01	0
0	01	01	0
1	01	10	0
0	10	10	0
1	10	00	1

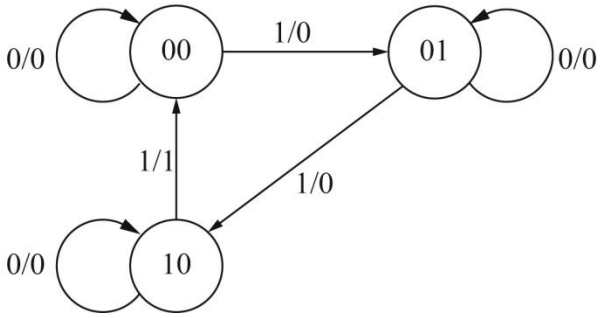


Figure 4.45: State transition tables and graphs.

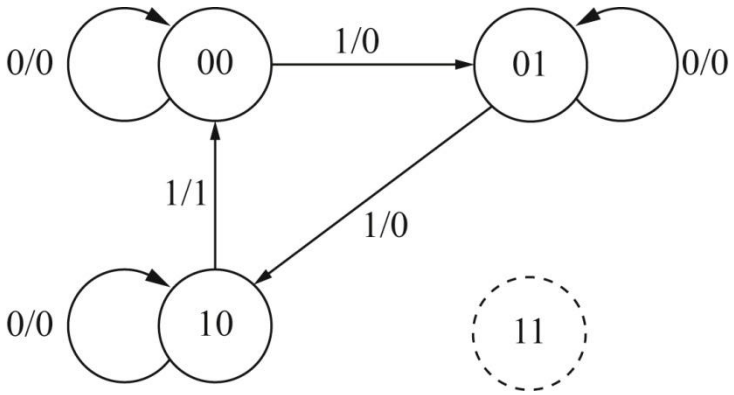


Figure 4.46: An FSM with an unspecified state.

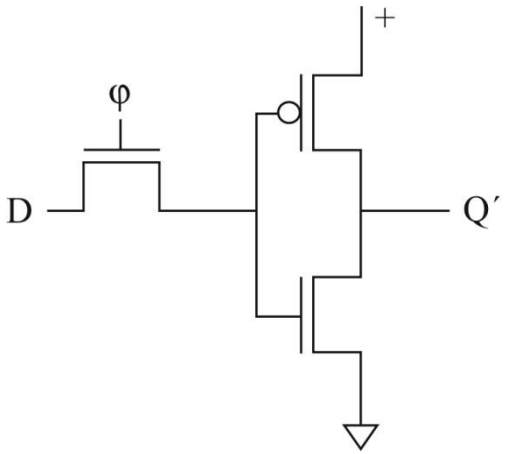


Figure 4.47: Circuit schematic for a dynamic latch.

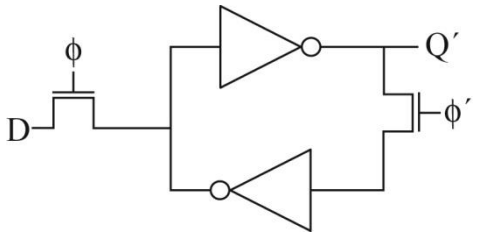


Figure 4.48: A static latch circuit.

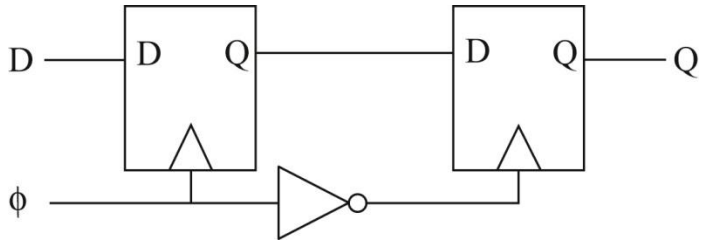


Figure 4.49: A master-slave flip-flop.

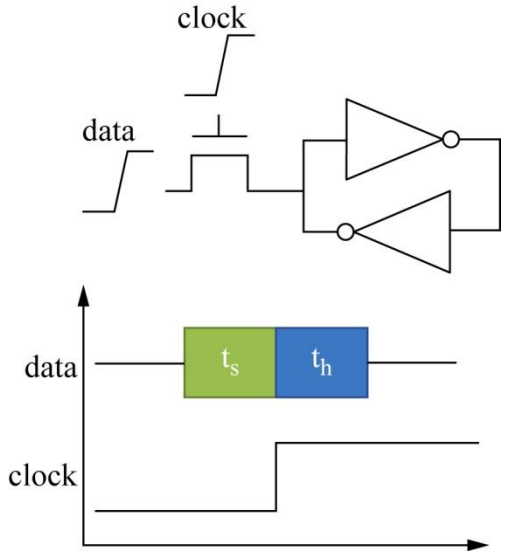


Figure 4.50: Setup and hold times.

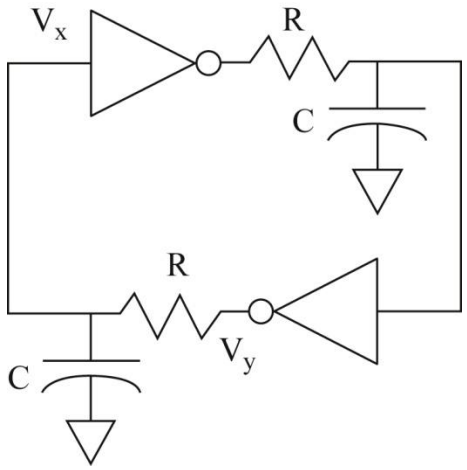


Figure 4.51: A simple analytical model for a register.

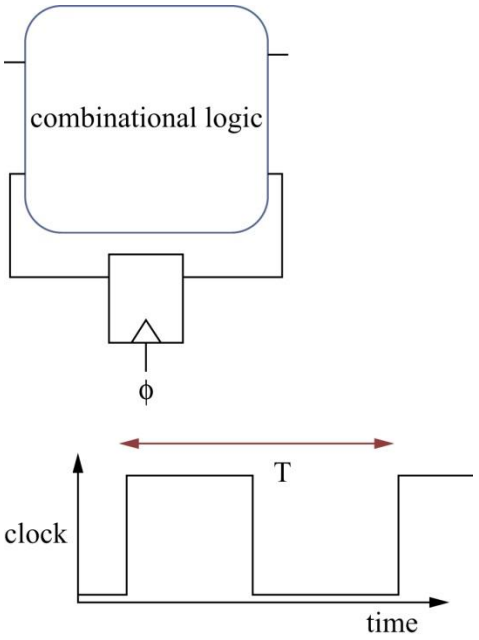


Figure 4.52: Sequential machines and clock period.

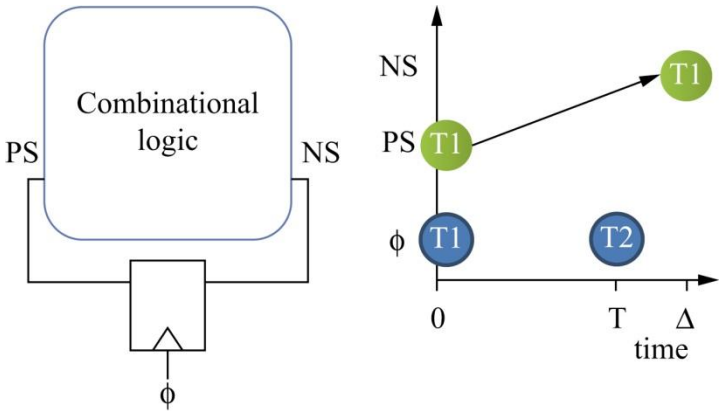


Figure 4.53: Errors caused by too-fast clocking.

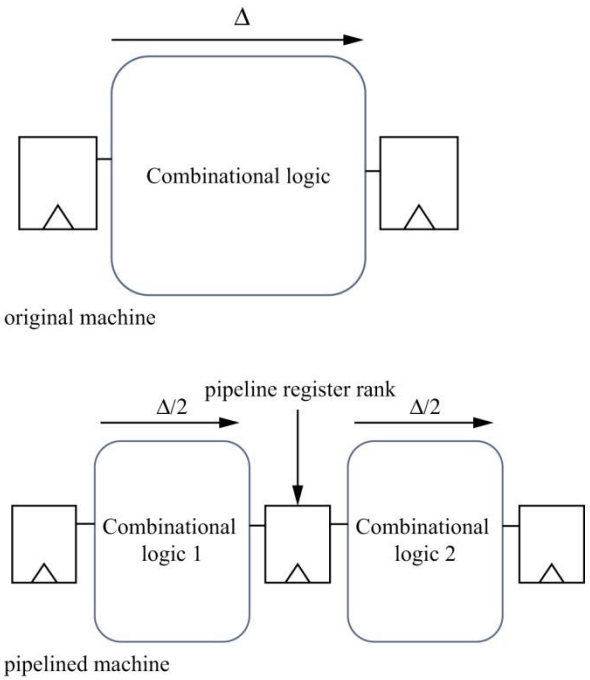


Figure 4.54: Pipelining.

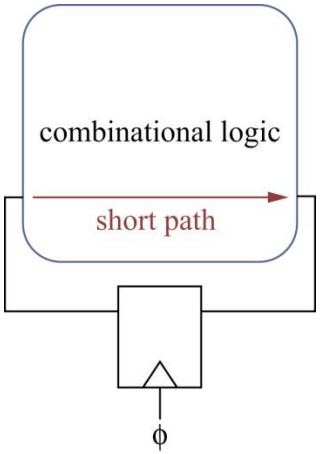


Figure 4.55: Problems with a single rank of latches.

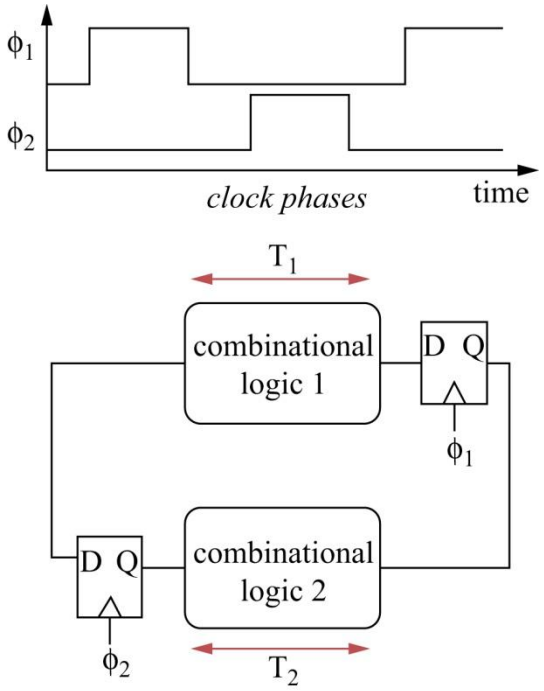


Figure 4.56: Two-phase, nonoverlapping clocks for latches.

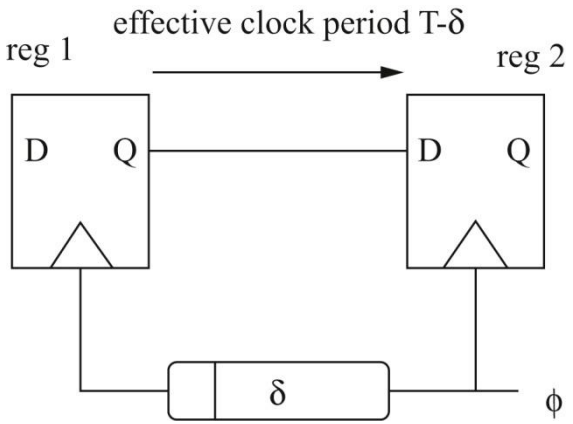


Figure 4.57: Clock delay and skew.

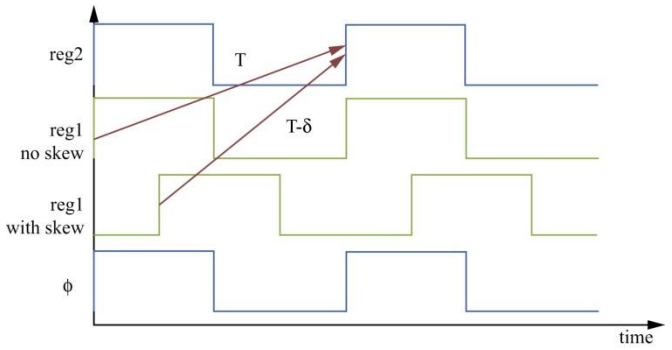


Figure 4.58: The effect of clock skew on system timing.

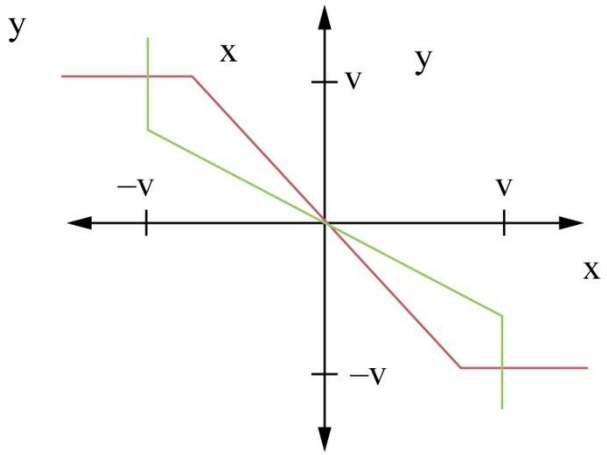


Figure 4.59: Metastability in cross-coupled inverters.

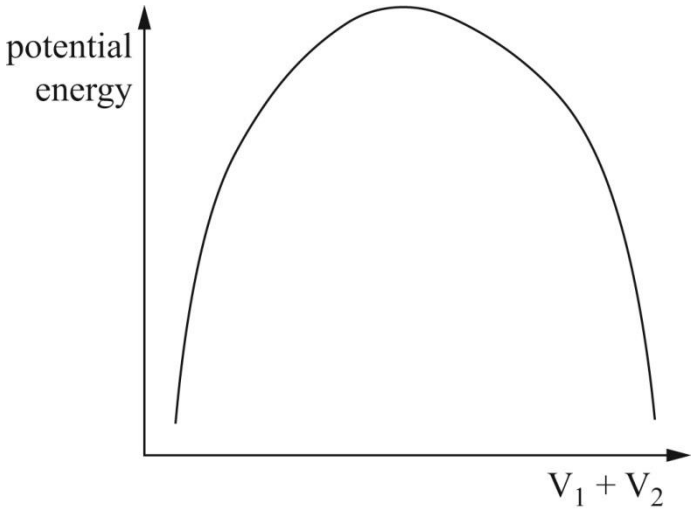


Figure 4.60: Energy versus system state for a register.

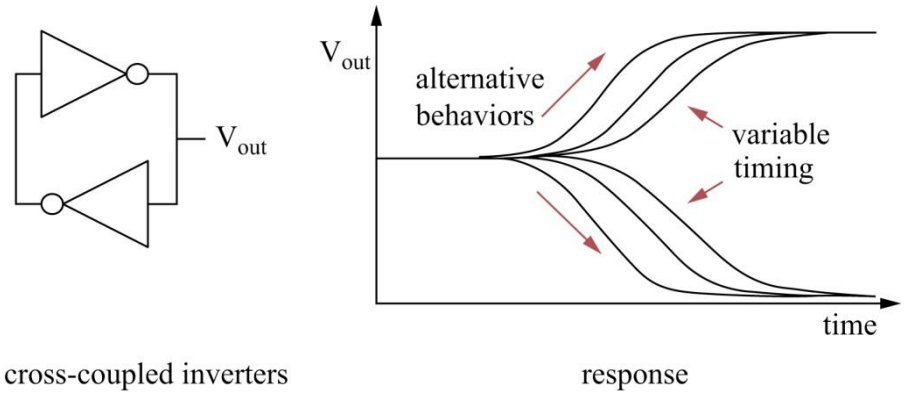


Figure 4.61: Metastable exponential divergence.

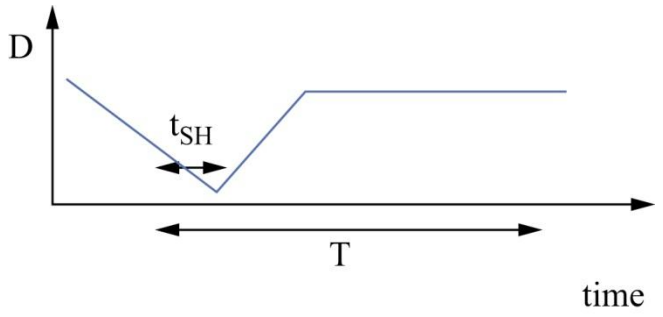


Figure 4.62: The vulnerable interval for metastability.

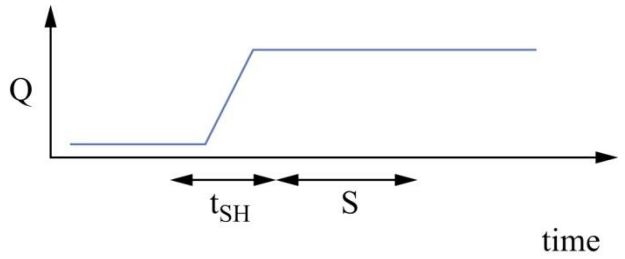


Figure 4.63: The stabilization window.

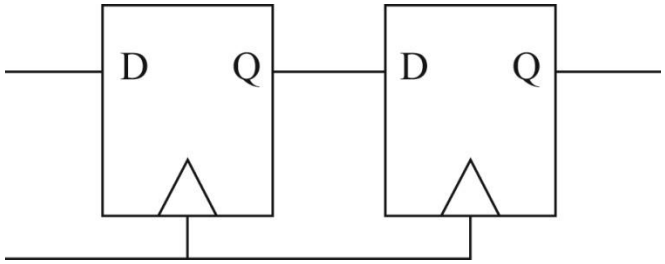
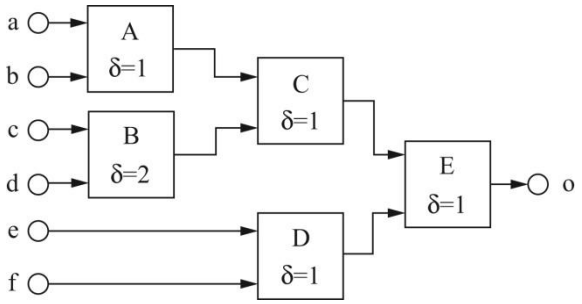
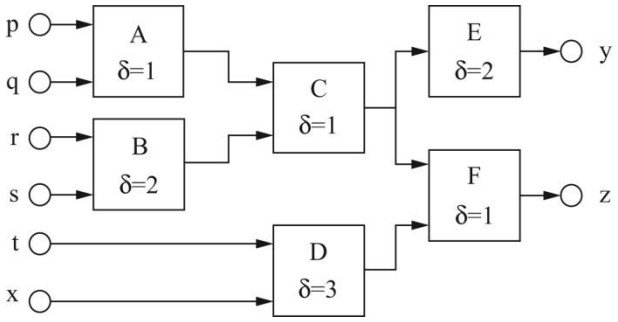


Figure 4.64: A dual-register synchronizer.

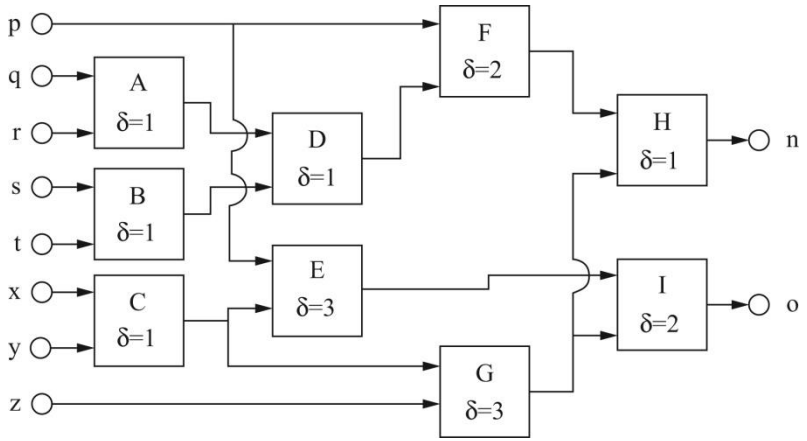
Example 4.4 Resistance and Capacitance Measurements.



Q4-1



Q4-2



Q4-3.