Chapter 5

Processors and Systems

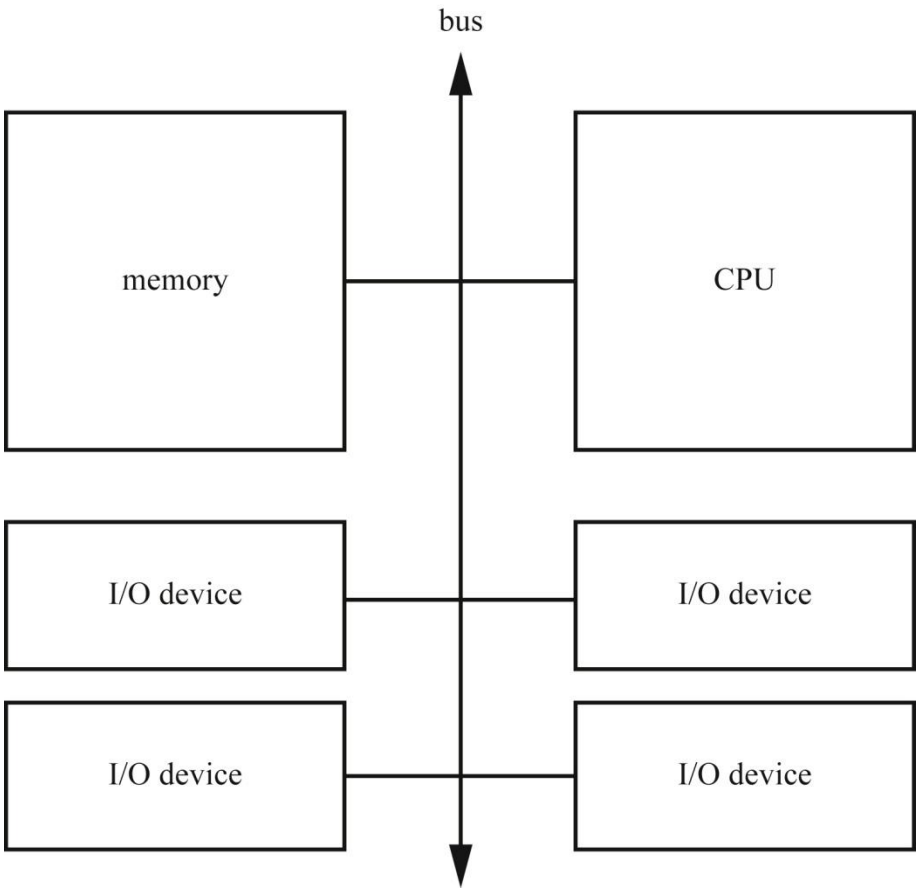


Figure 5.1: Block diagram of a computer system..

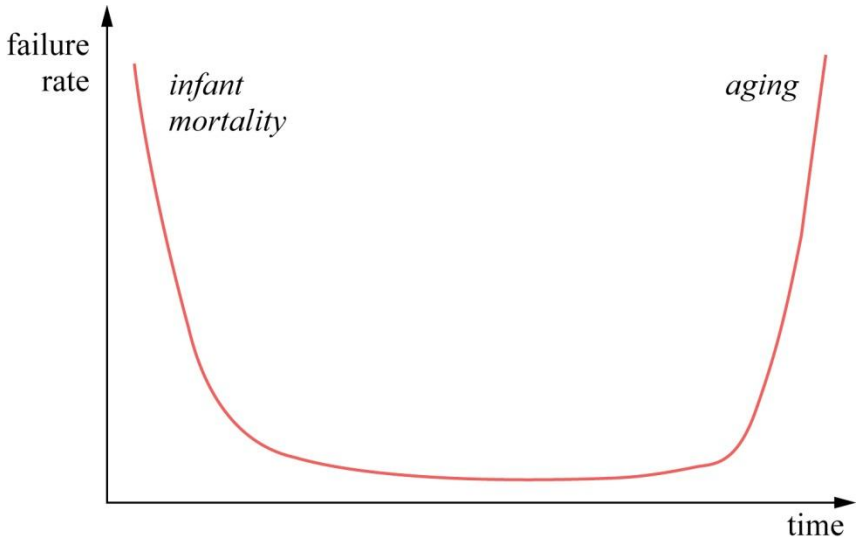


Figure 5.2: The bathtub curve for failure rates..

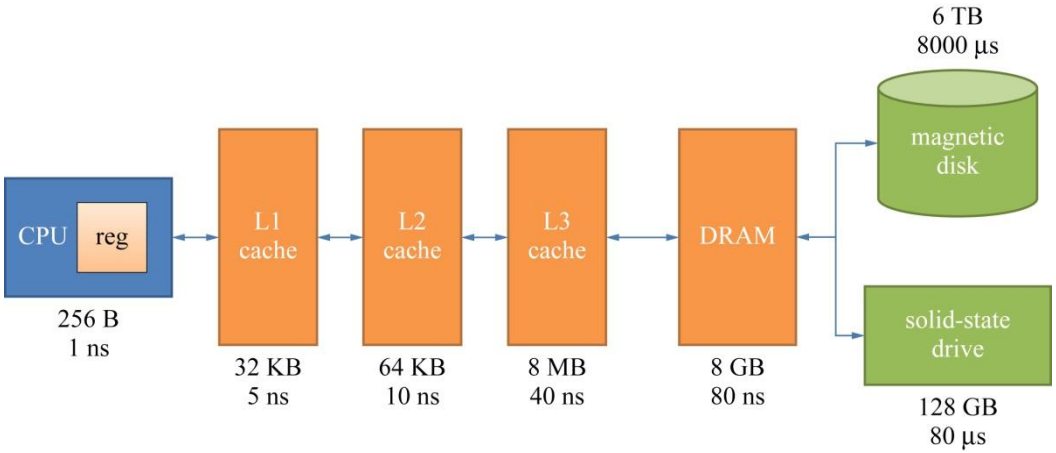


Figure 5.3: Relative access times across the memory hierarchy

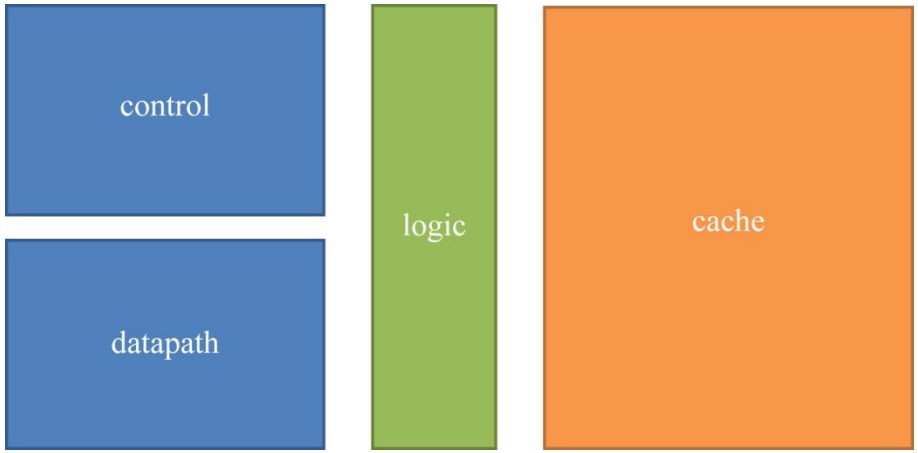


Figure 5.4: A chip floorplan.

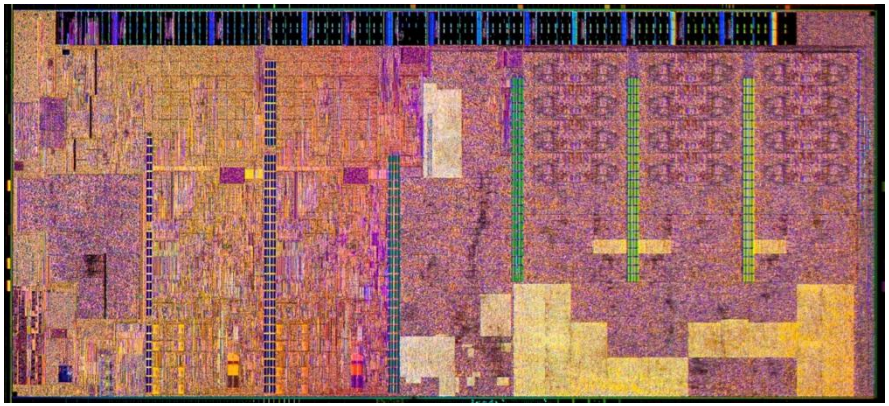


Figure 5.5: Die photo of a Broadwell processor.

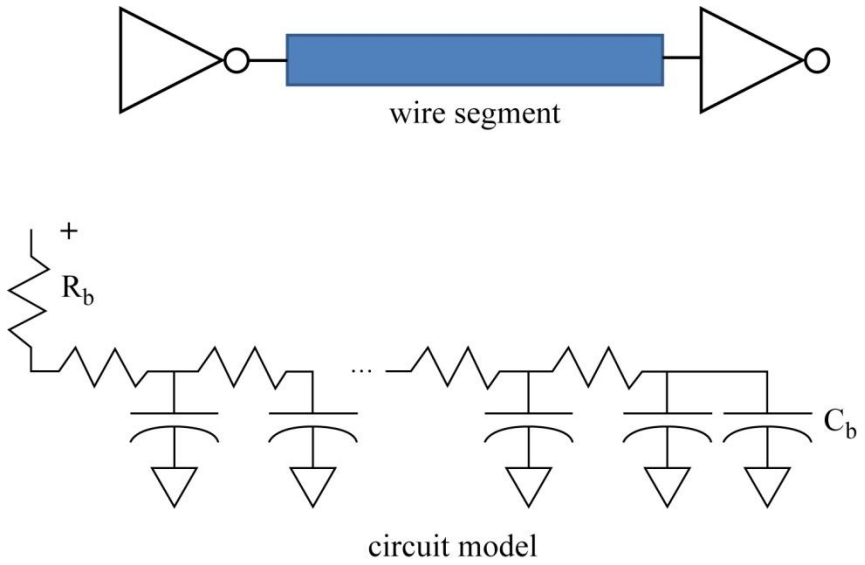


Figure 5.6: A model for buffers on long wires.

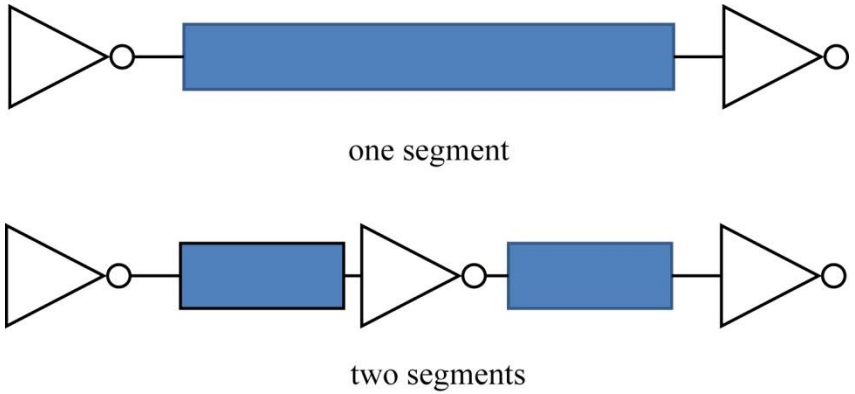


Figure 5.7: A long wire divided into one versus two segments.

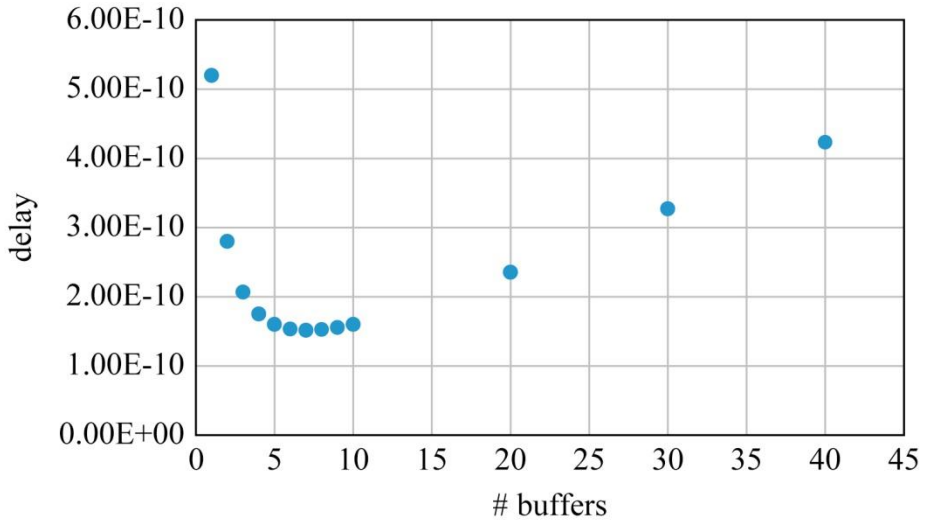


Figure 5.8: Delay versus number of buffers.

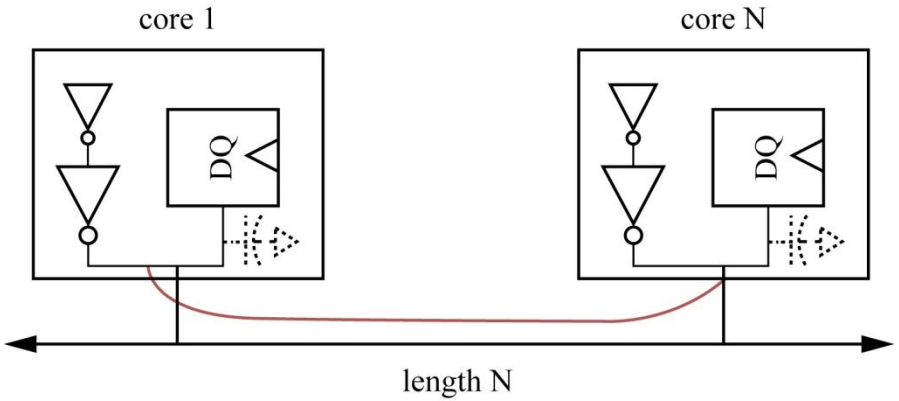


Figure 5.9: Model for delay on a bus.

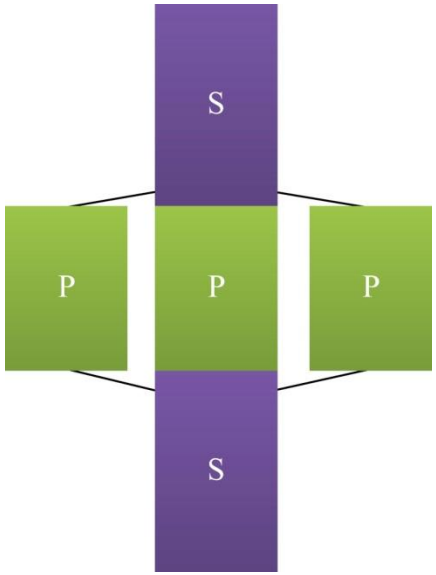


Figure 5.10: Series and parallel components of a job for Amdahl's law.

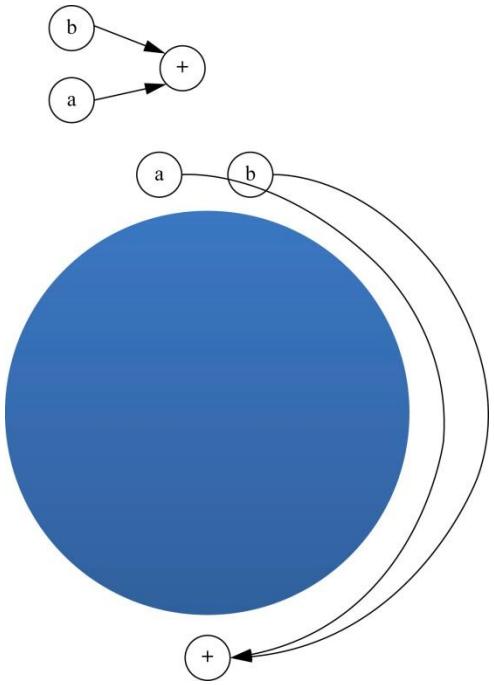


Figure 5.11: Communication delay between jobs.

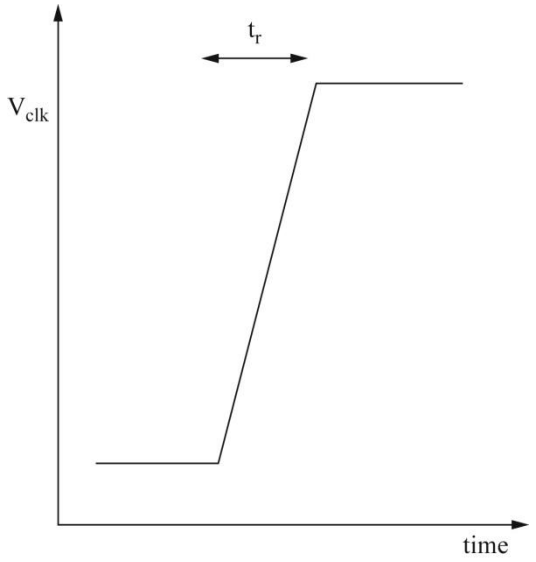


Figure 5.12: Rise time in a clock signal.

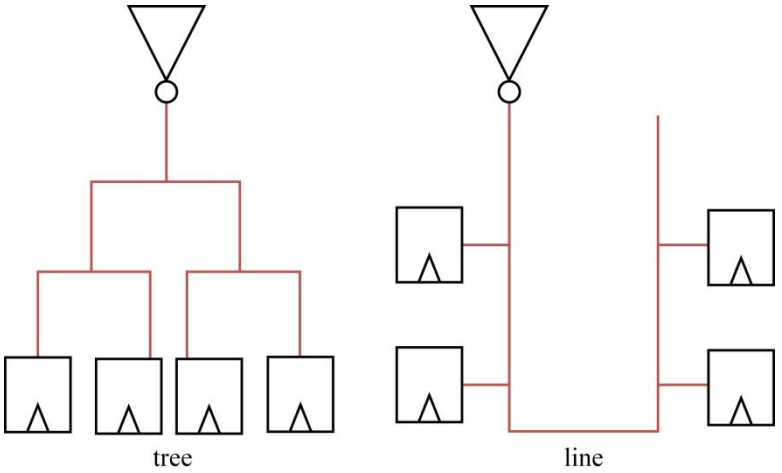


Figure 5.13: Trees versus lines for clock distribution.

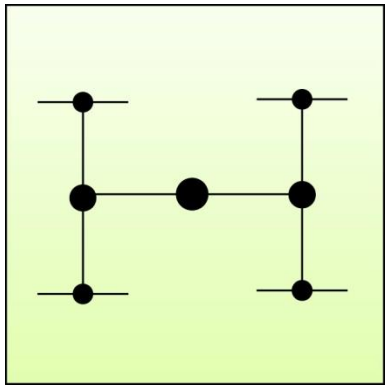


Figure 5.14: An H-tree for clock distribution..

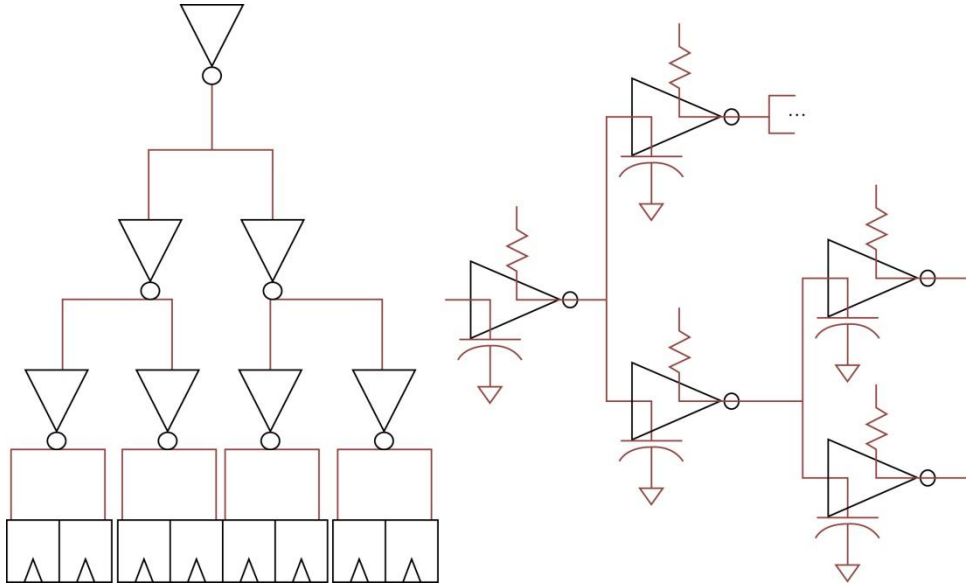


Figure 5.15: A buffered clock tree.

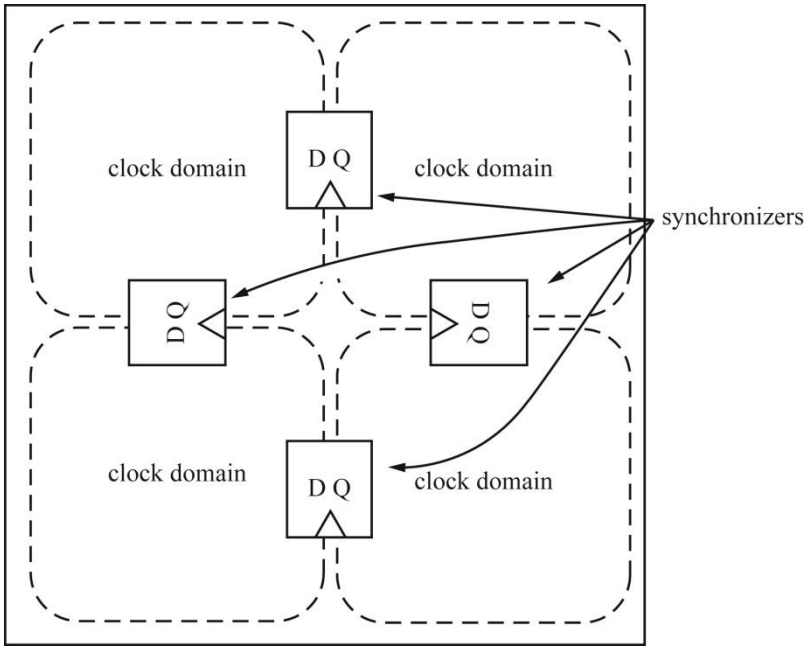


Figure 5.16: Clock domains on a large chip.

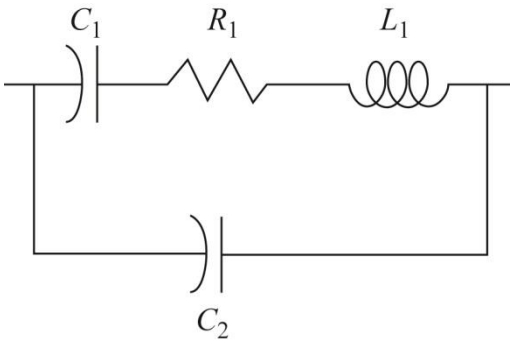


Figure 5.17: Equivalent circuit of a piezoelectric crystal [Pec97].

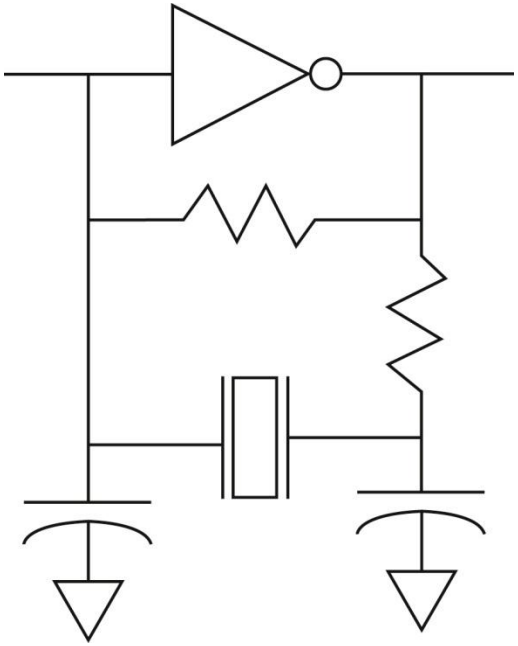


Figure 5.18: A Pierce oscillator..

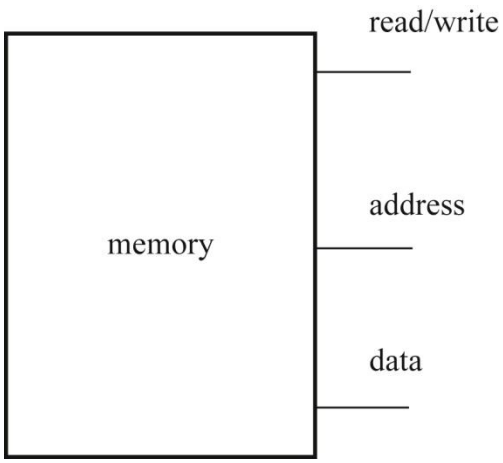


Figure 5.19: Interface to memory.

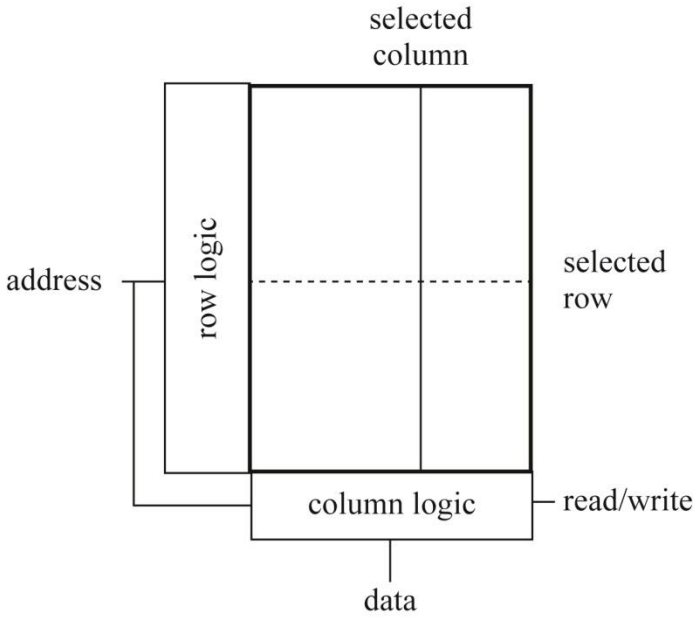


Figure 5.20: Organization of a memory array.

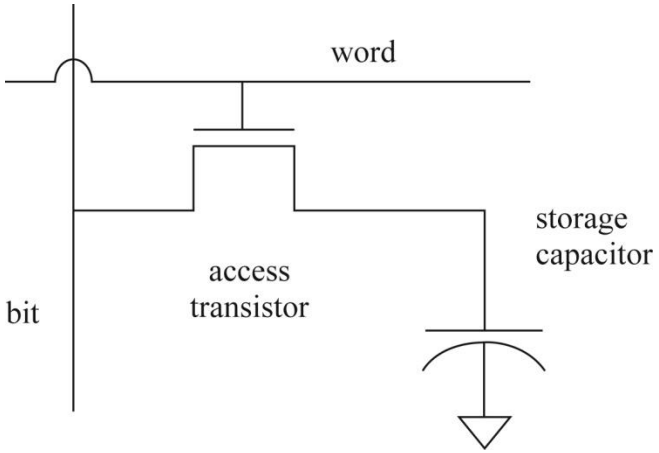


Figure 5.21: Circuit diagram for a DRAM cell.

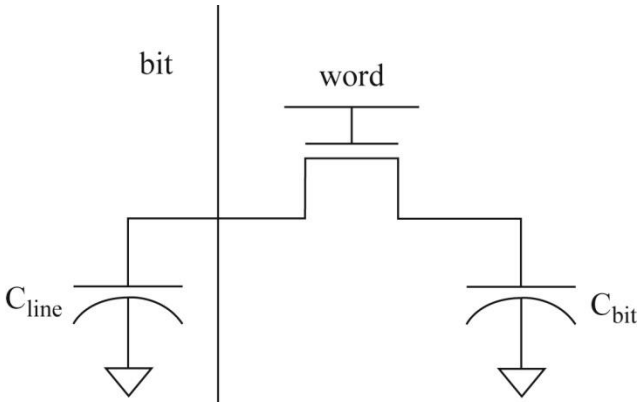


Figure 5.22: Model for DRAM sensing.

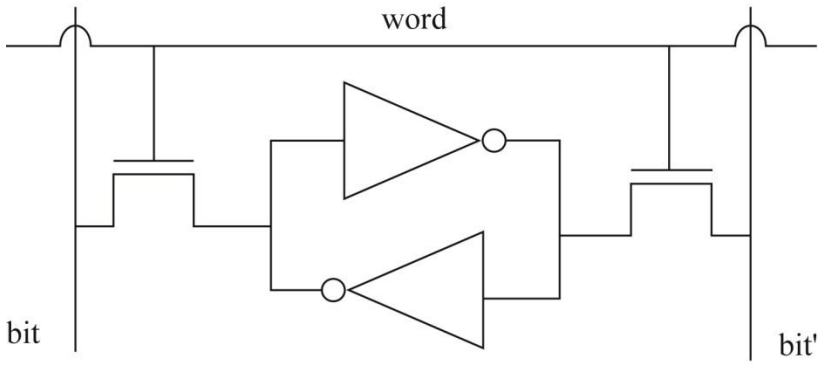


Figure 5.23: Circuit diagram for an SRAM cell.

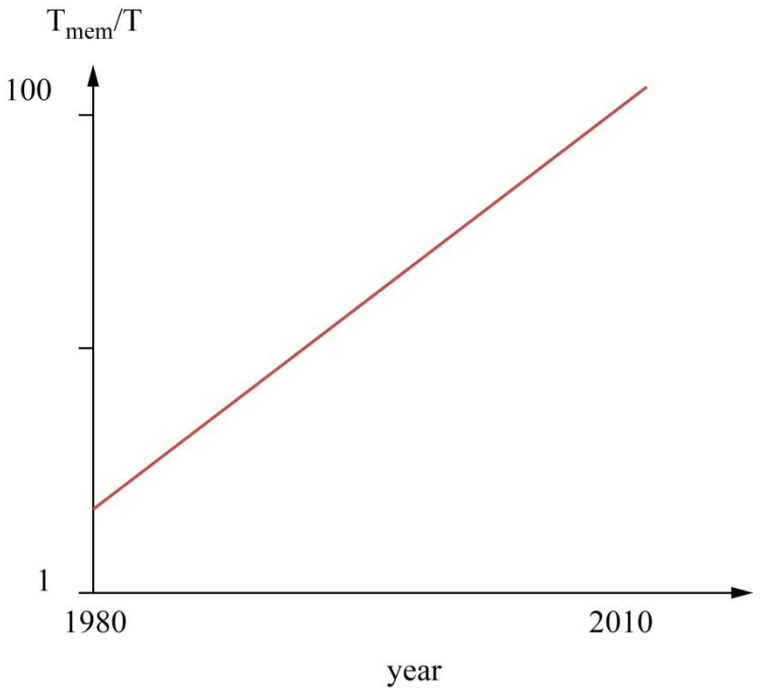


Figure 5.24: Growth of the memory wall over time.

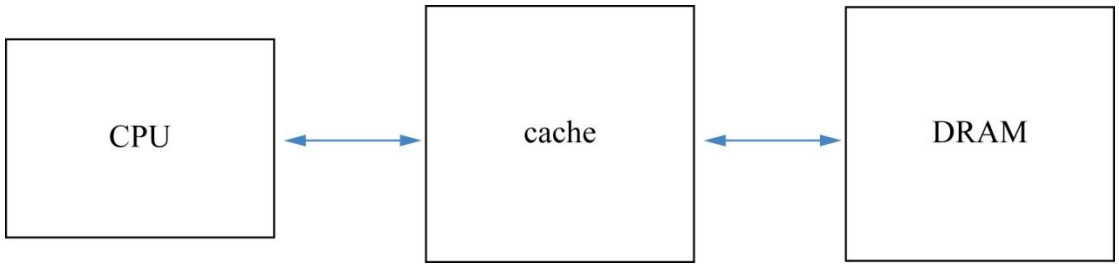


Figure 5.25: A memory system using both SRAM cache and DRAM.

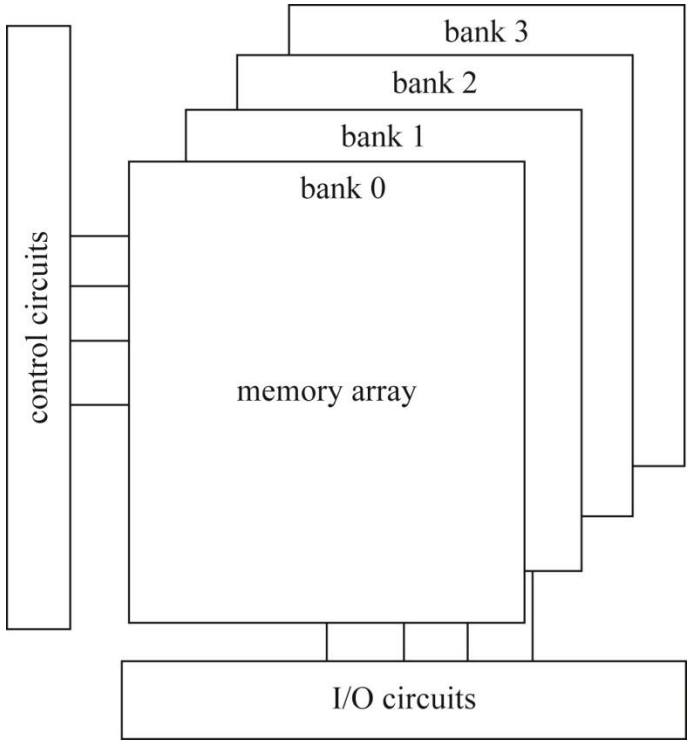


Figure 5.26: DRAM organized into banks.

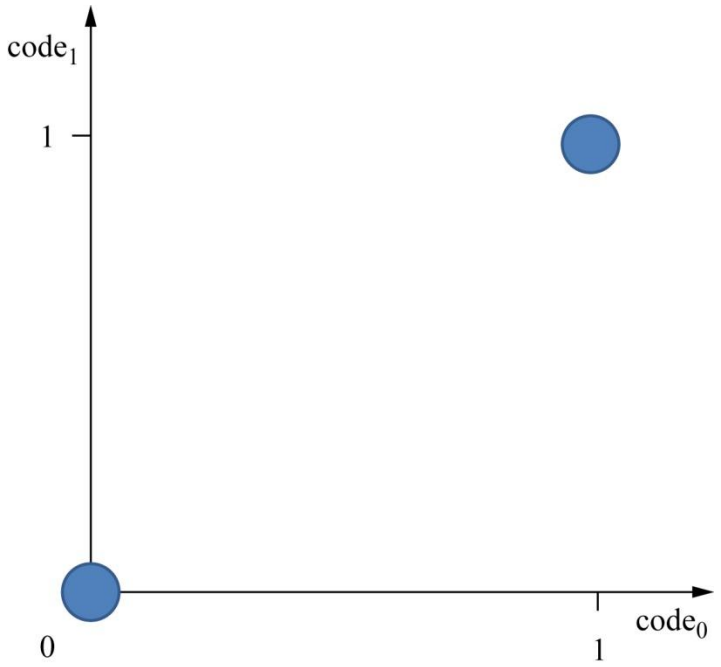


Figure 5.27: An error detection code.

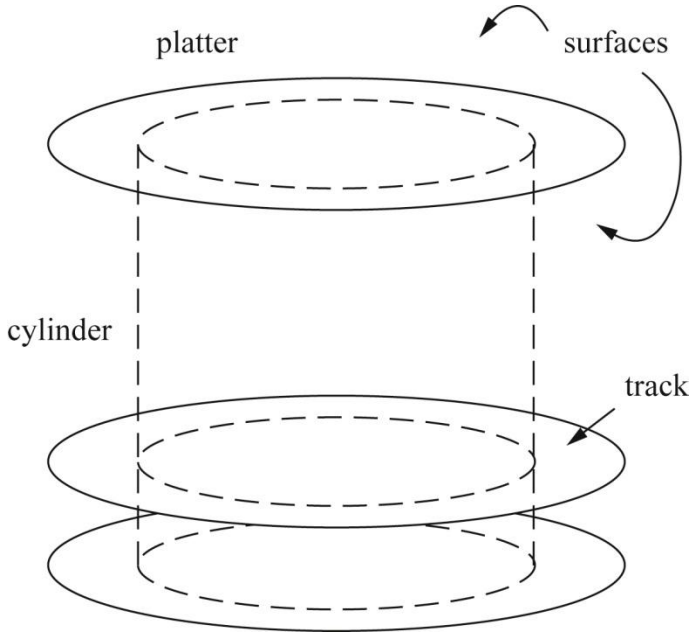


Figure 5.28: Organization of magnetic disk media.

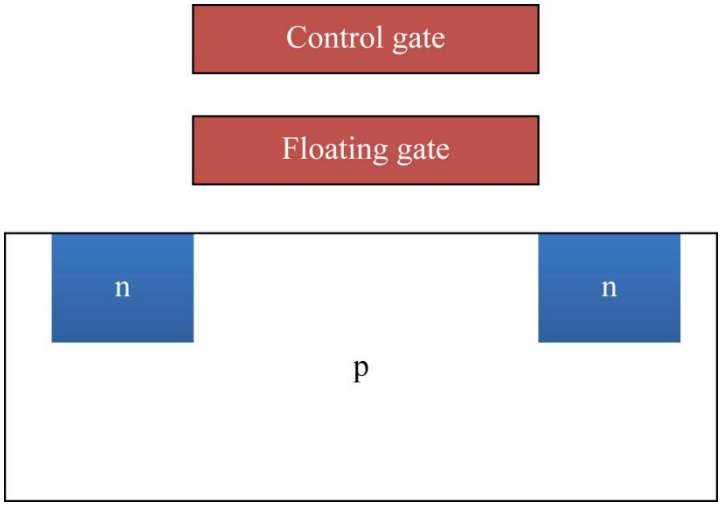


Figure 5.29: A floating-gate cell.

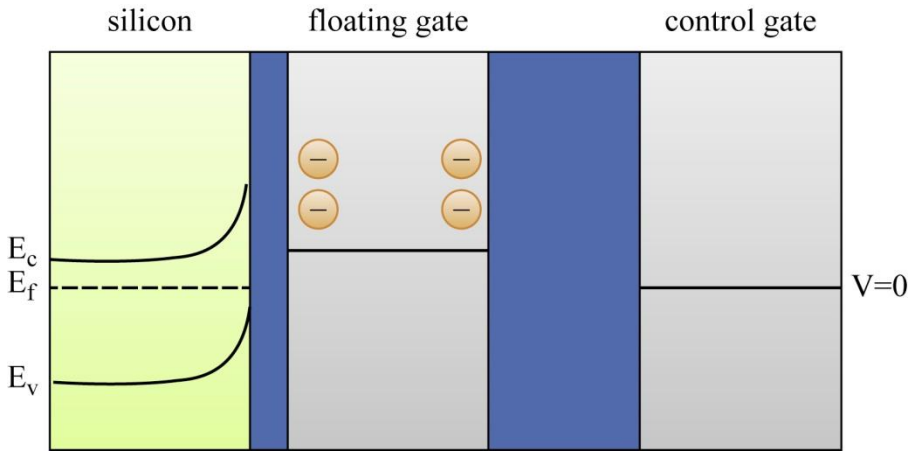


Figure 5.30: Band structure of a floating-gate cell with a stored charge on the floating gate [Kah67].

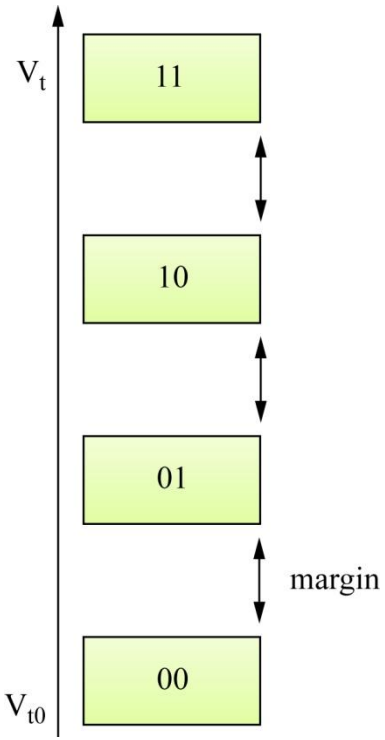


Figure 5.31: Voltage levels in a multilevel flash cell.

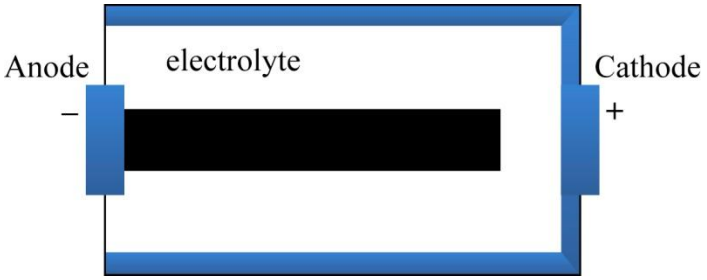


Figure 5.32: Structure of an electrochemical cell.

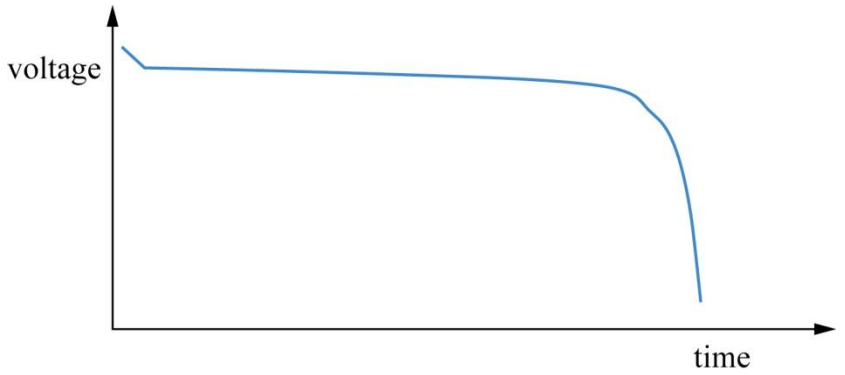


Figure 5.33: Typical battery discharge characteristics.

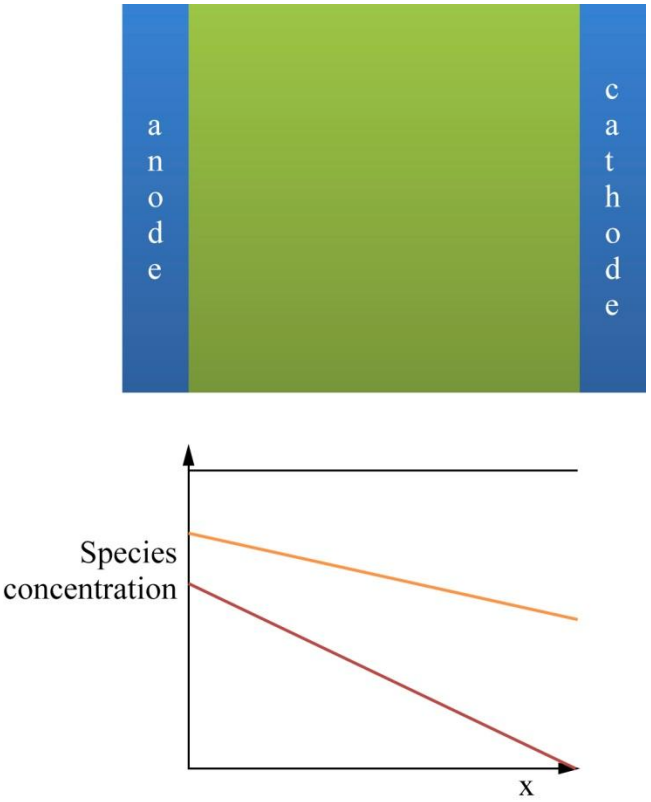


Figure 5.34: The Peukert Effect..

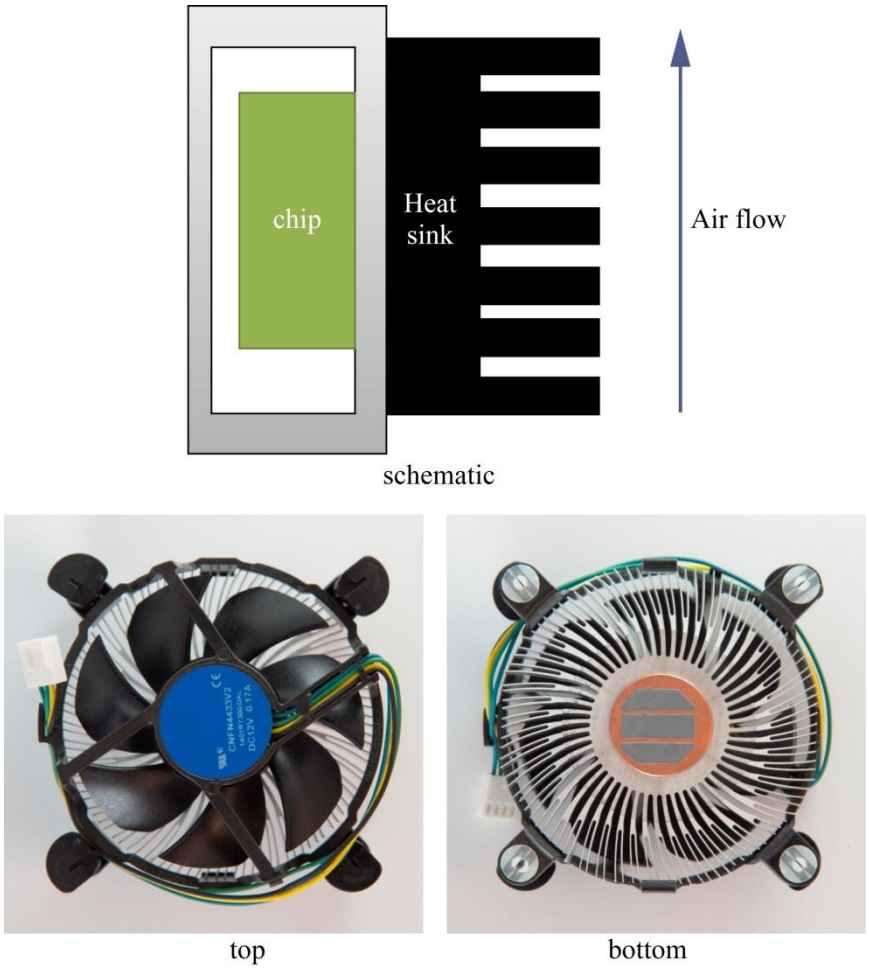


Figure 5.35: A chip and its heat sink..

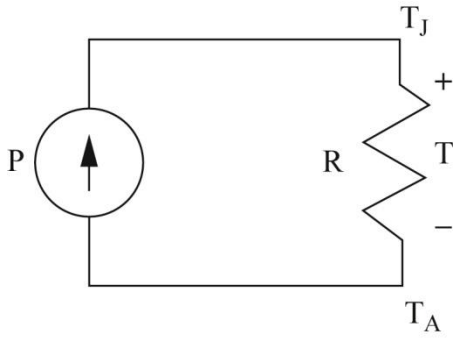


Figure 5.36: A thermal resistance circuit.

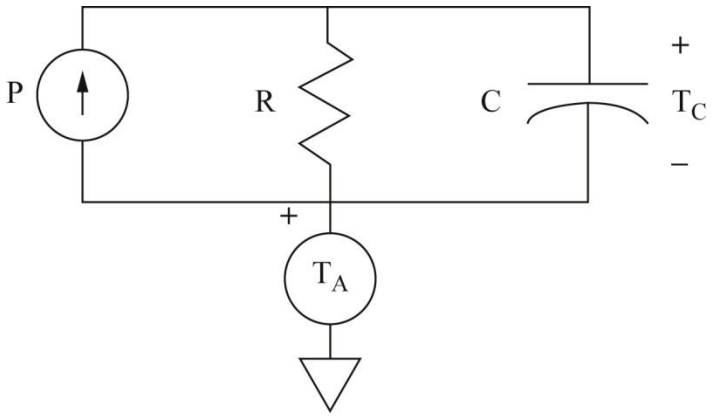


Figure 5.37: A thermal RC model of a chip.

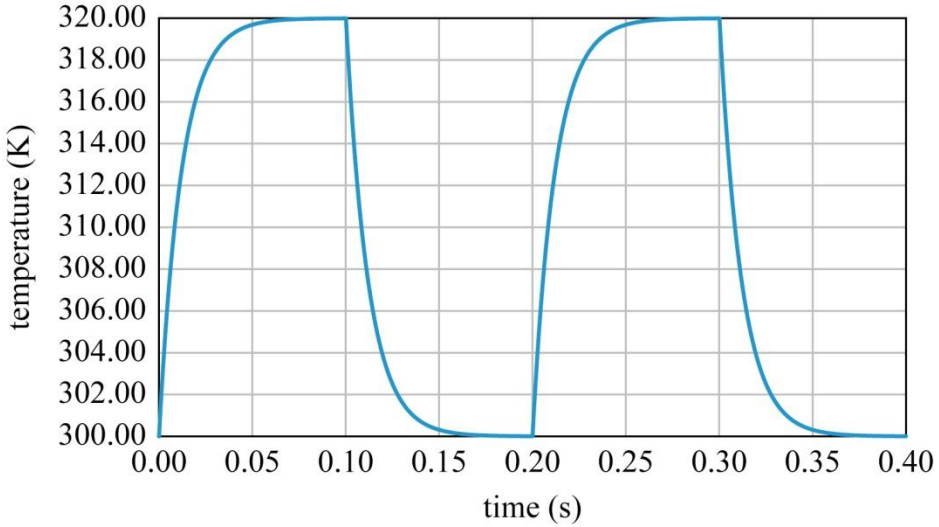


Figure 5.38: Thermal waveform for a thermal square wave.

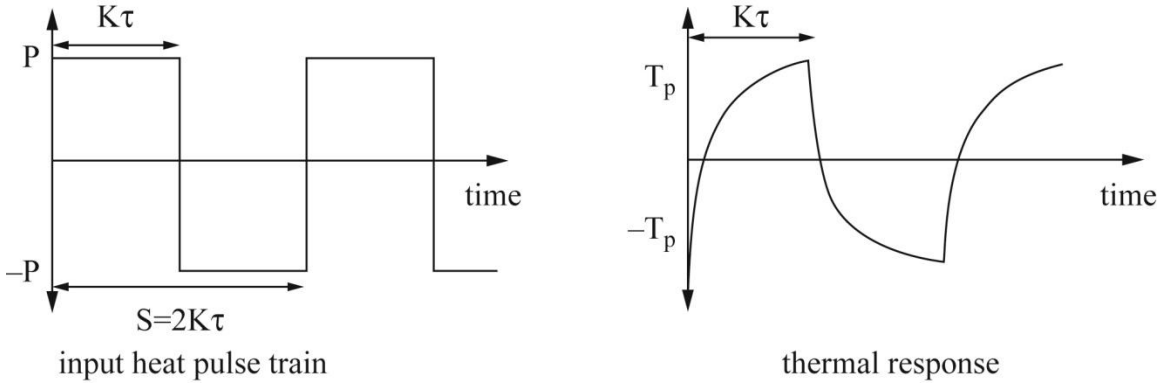


Figure 5.39: Peak-to-peak waveform from a thermal square wave input.

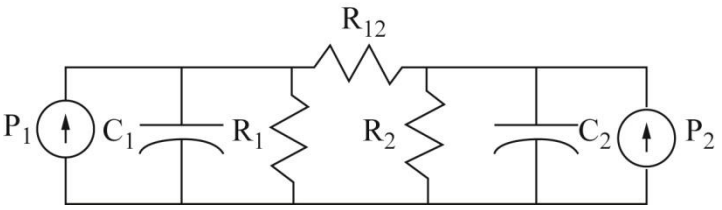


Figure 5.40: A thermal model for a pair of adjacent cores.

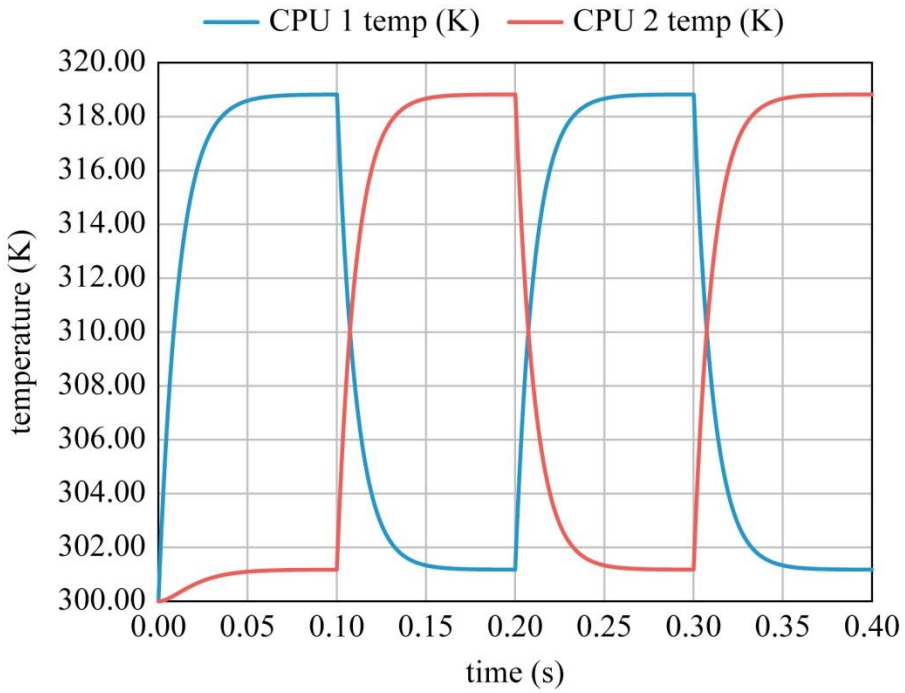
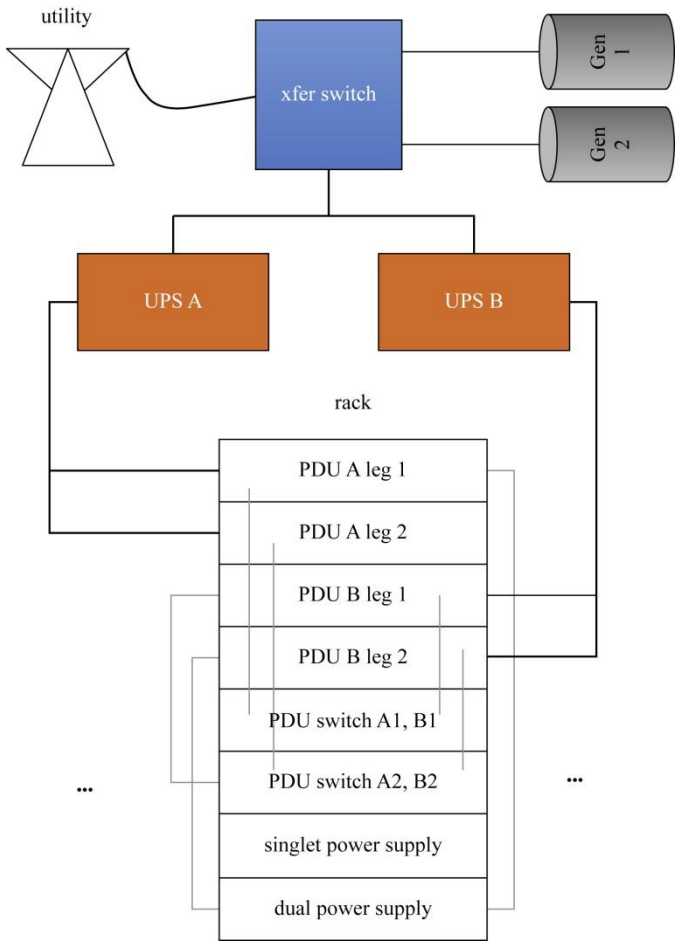
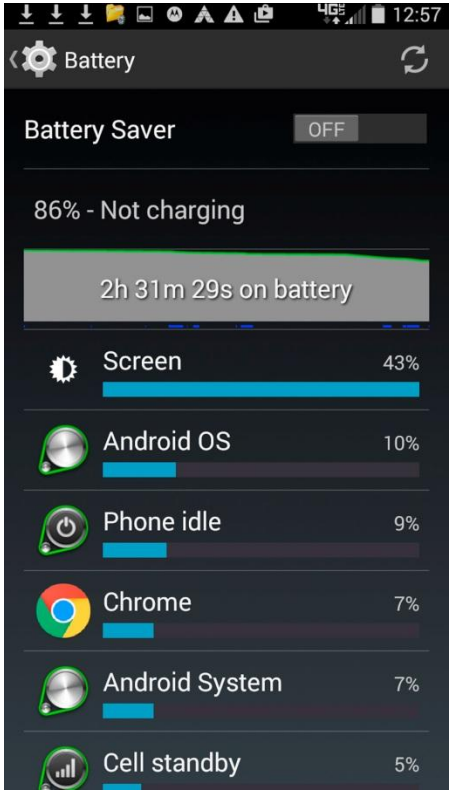


Figure 5.41: Thermal waveforms for a two-core system with alternating operation.

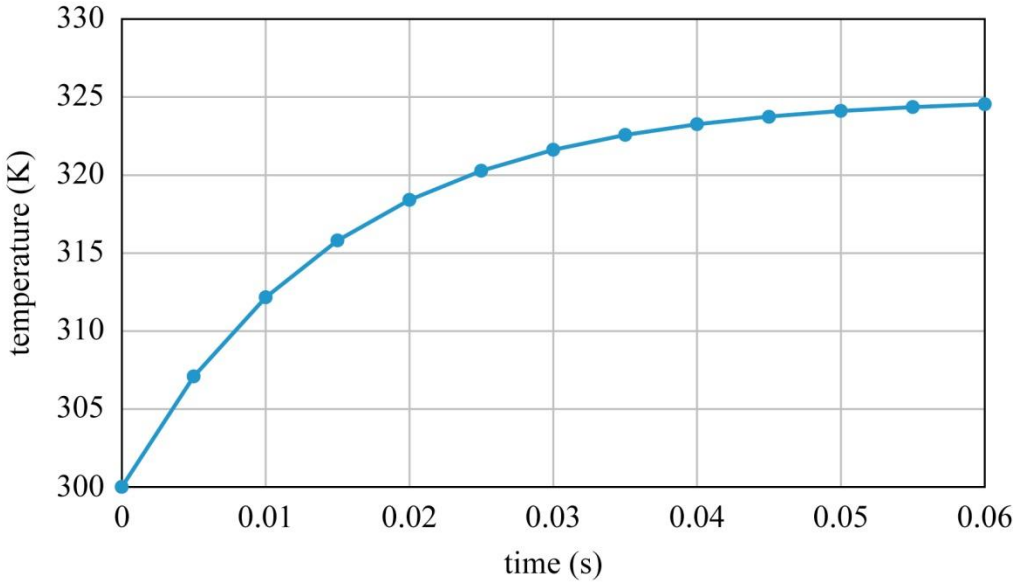
Example 5.3 Planet-Scale Computer



Example 5.9 Data Center Power Distribution.



Example 5.11 Cell Phone Power Utilization



Example 5.17 Thermal RC Model of Chip Temperature