1. **A 40-year Perspective on Scaling**  
   Robert H. Dennard and Dominic Schepis  

This chapter gives a perspective for the future of scaling. The chapter also examines developments related to new materials used and required as a result of scaling. Vertical scaling drives the need for new Gate materials. The new methods of deposition for these materials are discussed. A summary of scaling theory, first presented 40 years ago, and still the basis for transistor miniaturization is presented. Factors like Vt are affected and this in turn affects performance. These relations are explained. The possibility of performance gain by cooling is discussed.

Keywords: Scaling Theory for Transistors, Performance and scaling, Electrical effects and scaling, new materials, new deposition methods, Low temperature role in increased performance.

2. **Scaling – Causes and Consequences**  
   Krishna Seshan  

This chapter discusses the central theme that underlies this Handbook: Scaling. Device scaling is discussed in several parts: Transistor and Front End of the Line (FEOL), Interconnection, as Back End of the line (BEOL), Input –output scaling. The consequences of diminishing dimensions – both horizontal and vertical are discussed with possible future trends.

Keywords: Scaling of Transistors, Gate Oxide scaling, Metal Gates, SOI materials & advantages, Heat generation, Leakage current scaling, Packaging and chip cooling, Reliability effects, Flash Scaling.

3. **Thermalscaling**  
   Krishna Seshan  

Increased heat generation is one of main consequence of scaling of random logic designs. Memory scaling does not increase as dramatically. Heat generation trends, and features of the packages designed to cool the chips are discussed. New materials formulation in Thermal Interface Materials (TIM) has played - and will continue to play - a crucial role in Cooling. The chapter gives a summary of heat generation, cooling challenges and package designs to achieve such cooling.

Keywords: Heat Generation from Microprocessors, scaling and heat generation, Package design, TIM (thermal interface materials).
4. PVD – Special Topics
Andrew H. Simon

The revised edition focuses on the applications of sputter processing to the semiconductor industry. The physical fundamentals behind sputtering (physical vapor deposition (PVD) processes are covered, with a review of the energy dependencies and kinematics of particle ejection, sputter yields and the cosine sputtering law. The physical phenomena in sputter processing apparatus are introduced using the DC diode and Rf plasma to illustrate typical space-charge and current-voltage behaviors. Modern semiconductor-industry applications are introduced with a discussion of magnetron sputtering and its advantages for volume manufacturing of thin-film processes. Reactive sputtering, and enhancements to the directionality and conformality of thin-film sputtering, including collimation, ionization and bias sputtering, is described.

Modern clustered-vacuum tooling provides the capability to deposit multiple layers of sputtered films in conjunction with other processes, such as sputter and reactive cleans, desorption steps, and non-PVD depositions such as ALD and CVD. An illustrative example of a multistep sputter deposition sequence for semiconductor interconnects is used to demonstrate the capability of modern sputter tooling to engineer interface properties and shapes of microelectronic structures. Standard metrology techniques for sputter processes are discussed, including four-point probe and thickness measurement techniques. Finally, contamination control is discussed for both intrinsic mechanisms (shielding design) and extrinsic mechanisms (external contamination control).

Keywords: Sputtering, Physical Vapor Deposition, Magnetron, Collision-Cascade, Sputter Yield, Sputter etching
CVD Special Topics:
Thin Film Strain Engineering and Pattern Effects in Dielectrics CVD
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The chapter covers two different topics which became increasingly important in the semiconductor industry due to the shrinking device dimensions and continuation of scaling: a) effect of intrinsic film stress on a semiconductor device and b) interaction of Chemical Vapor Deposition (CVD) with pattern density. The chapter surveys new developments in deposition of highly strained dielectric thin films and evolution in film properties, especially in film intrinsic stress. The basics of silicon strain engineering as well as silicon strain metrology are covered.

The second part of the chapter describes the microloading effect: dependence of CVD process deposition rate on pattern density. Several manifestations of pattern effects during CVD deposition process are discussed as well as methods aimed at quantifying the microloading effect and improving film thickness variability across various pattern densities on a chip. The chapter also covers the basics of Atomic Layer Deposition (ALD) technique and summarizes ALD precursor information for several major dielectric materials.

Keywords: Atomic Layer Deposition (ALD) -of SiN, SiO2 and HfO2 thin films, Dual Stress Liner (DSL), Plasma Enhanced CVD (PECVD) of dielectric thin films, Microloading, Multilayer films, Pattern Effects in CVD, Silicon Oxide and Silicon Nitride Films Properties, Silicon Strain Metrology, Strained CMOS devices, Stress in Thin Films, Stress Memorization Technique, Step coverage, UV cure (effect on intrinsic film stress)
6. Equipment and Manufacturability Issues in CVD processes
Loren Chow
Intel Corporation

Device scaling continues to drive increasingly stringent requirements of thin films from the transistor through the interconnect layers. Such films that enable scaling include those in the high k gate stack to minimize leakage, channel materials and stressors for mobility enhancement, metals in the back end for low resistance interconnects and low k dielectrics to minimize parasitic capacitance. Chemical vapor deposition is routinely utilized to deposit all the aforementioned films with a quality and throughput that delivers enhanced device performance and a reduced per transistor cost with each succeeding technology node. This chapter provides an overview of chemical vapor deposition equipment and the films CVD is capable of depositing in the device fabrication process.

Reviewed are several chemical vapor deposition technologies (including atmospheric, low pressure, plasma-enhanced and metal-organic CVD) and their applications in semiconductor manufacturing for depositing metals, dielectrics and epitaxial semiconductors. The goal here is to enable the reader to make an educated decision on which CVD technology to use based on application, material and manufacturing needs. Practical matters related to CVD equipment and deposition such as metrology, contamination concerns and equipment procurement are also covered. The chapter begins with a history of CVD and finishes with recent trends in CVD technology.

Keywords: chemical vapor deposition, thin film, semiconductor, silicon, film metrology CVD, deposition, deposition equipment, history of chemical vapor deposition (CVD)

7. CMP Method and Practice
Kenneth C. Cadien and Lucy Nolan

Chemical Mechanical Polishing (CMP) is a powerful fabrication technique that uses chemical oxidation and mechanical abrasion to remove material and achieve very high levels of planarity. In this chapter, the theory and practice of CMP are discussed. Representative tools for both polishing and cleaning are described, as are the various system components. The damascene method of fabrication for copper features is described in detail. The theoretical underpinnings of CMP are discussed, with an emphasis on the electrochemistry of copper. The current literature is also surveyed and several polishing models are summarized. Finally, new CMP techniques and components, driven by the adoption of new materials in the microelectronics industry, are discussed.

Keywords: Chemical Mechanical Polishing (CMP), Planarization, Abrasive(s), Silicon CMP, Shallow Trench Isolation, Cu-CMP, Damascene, Copper electrochemistry, Modeling
8. Process Technology for Copper Interconnects
Jeff Gambino

Copper interconnects have gained wide acceptance in the microelectronics industry due to improved resistivity and reliability compared to Al interconnects. Initially SiO₂ was used as the interlevel dielectric. To reduce interconnect capacitance, C-doped SiO₂ or SiCOH was introduced at the 90 nm node, and porous SiCOH was introduced at the 45 nm node, to achieve a dielectric constant of 2.5 or less. However, there are many process problems with the integration of Cu interconnects and porous low-k dielectrics, including patterning, liner coverage, chemical mechanical polishing (CMP), and packaging. These processes must be optimized to ensure adequate reliability for time-dependent-dielectric breakdown (TDDB), electromigration, stress-induced voiding, and packaging stresses. In this chapter, some of the key integration and reliability challenges are discussed.

Keywords: Copper Interconnect, Low-k dielectric, electromigration, stress-induced voids, time-dependent dielectric breakdown (TDDB), dual damascene

9. Optical Thin Films
Angus Macleod

The material and shape of an optical surface is chosen to manipulate the direction of the light. Other properties such as reflectance or transmittance are rarely ideal and their modification without altering the directional properties is the principal role of an optical coating. Coatings are, therefore, necessary components of virtually every optical system. They consist of assemblies of thin films with performance a function of interference together with the material properties. They can consist of just one layer or even more than a thousand layers deposited to a thickness accuracy of a small fraction of a wavelength. Their mechanical, environmental, and chemical properties are often as important as their optical. This chapter begins with a short review of the fundamental optics required for understanding coatings, presents their basic structures, describes their manufacture including the problems of control, and discusses their incorporation in systems.

Keywords: Optical Coatings, Optical Films, Optical Filters, Optical Coating Manufacture, Interference Filters
10. Thin Films in Photovoltaics
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This chapter describes the role of thin-film processing in photovoltaic applications. A brief overview of photovoltaic structures and operating principles (including efficiency loss mechanisms) is first presented. Manufacturing processes for the major solar cell technologies are then described, with focus given to the role of thin films in these technologies. The various deposition and characterization techniques for these thin-film processes are described in detail. Special attention is given to crystalline silicon technologies (using silicon nitride ARC layers or amorphous silicon/TCO emitter structures) and thin-film absorber technologies (CIGS, CdTe, and amorphous silicon tandem-cell structures). Cost and performance comparisons of these various technologies is presented next, followed by a reliability survey, again with emphasis on the role that the various thin-film technologies play in determining the operational life of the product. The chapter concludes with a summary of the emerging areas of study in the field, which hold the most promise for future growth.

Key words: Photovoltaic, solar cells, optical absorbers, CIGS (copper indium gallium sulfide), CdTe (cadmium telluride), energy conversion, conversion efficiency

11. Thin Films in Memory Applications
Brad Herner

Thin films have been a key enabling factor in the development of semiconductor---based memories. The Application of thin films in volatile memories, principally dynamic random access memory (DRAM), And nonvolatile memories, principally flash memory, is reviewed. Process technologies, including chemical vapor deposition (CVD) and atomic layer deposition (ALD), and their integration into device fabrication are discussed. Finally, thin films in potential future memory devices are discussed, along with the challenges of new device introduction into commercial markets.

Keywords: Semiconductor memory, DRAM, Flash, NAND, Capacitor, Charge trap.