The Role Of Metrology And Inspection In Semiconductor Processing

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1.0 OVERVIEW

As integrated circuits (IC) are incorporated into more and more products, the market demand for lower cost, higher performance devices continues to grow. In order to design and manufacture a high performance integrated circuit cost-effectively, the parameters of the manufacturing process need to be carefully controlled: film thicknesses and material properties must be accurate, uniform and controlled; linewidths and edge profiles must fall within tight limits, and the devices need to be free of defects that affect yield.

Thin film metrology and wafer inspection for defects are integral to controlling the semiconductor manufacturing process. Film properties, linewidths, and defect levels need to be measured, first to optimize the manufacturing process, then later to ensure that it is operating under control.
This chapter explores the subjects of metrology and inspection of integrated circuits. After the introduction, implementation strategies for metrology and inspection are examined from a historical perspective. Then, as we anticipate increasingly complex devices having critical dimensions of 0.18 and 0.13 μm, manufactured on 300 mm wafers, we look at how metrology and inspection will evolve to meet these measurement challenges, while simultaneously meeting increasing pressure for automation, higher throughput and higher reliability. In the final section we provide a technology reference that discusses theory of operation, equipment design principles, main applications, and strengths and limitations of the metrology and inspection systems. The sections are organized as follows:

1.0 Overview
2.0 Introduction to Metrology and Inspection
3.0 Metrology and Inspection Trends: Past, Present and Future
4.0 Theory of Operation, Equipment Design Principles, Main Applications, and Strengths and Limitations of:
   4.1 Film thickness measurement systems
   4.2 Resistivity measurement systems
   4.3 Stress measurement systems
   4.4 Defect inspection systems
   4.5 Automatic defect classification
   4.6 Defect data analysis systems

2.0 INTRODUCTION TO METROLOGY AND INSPECTION

Metrology and inspection systems can be broadly separated into three main classifications by application: critical dimension (CD) and overlay measurements, particle and pattern defect detection, and thin film parameter measurement (such as resistivity, thickness and stress). The typical processing steps, and metrology and inspection equipment used to monitor and/or control them, are given in Table 1.

In the semiconductor industry, the continual demand for denser integrated circuits with higher performance and higher speeds drives technological advances in all facets of manufacturing. A key to the success of semiconductor processing is an understanding of the chemical, mechanical and kinetic properties of the wide range of materials used to make a typical circuit.
Table 1. Typical Metrology and Inspection Parameters Monitored, by Process Step

<table>
<thead>
<tr>
<th>PROCESS STEP USED</th>
<th>MEASURED ATTRIBUTE</th>
<th>METROLOGY SYSTEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si manufacturing</td>
<td>resistivity</td>
<td>4-point probe, eddy current</td>
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<tr>
<td></td>
<td>flatness</td>
<td>flatness tester</td>
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<td></td>
<td>defects:</td>
<td>defect inspection system</td>
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<td></td>
<td>particles</td>
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<td></td>
<td>micro-scratches</td>
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<td>crystalline defects</td>
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<td></td>
<td>haze</td>
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<tr>
<td>Si epitaxy</td>
<td>resistivity</td>
<td>4-point probe, eddy current</td>
</tr>
<tr>
<td></td>
<td>thickness</td>
<td>FTIR</td>
</tr>
<tr>
<td>Conductor deposition (PVD, MOCVD)</td>
<td>resistivity</td>
<td>4-point probe, eddy current</td>
</tr>
<tr>
<td></td>
<td>particulate contamination</td>
<td>defect inspection system</td>
</tr>
<tr>
<td>Dielectric deposition (CVD)</td>
<td>thickness, RI</td>
<td>reflectometer, ellipsometer</td>
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<td></td>
<td>stress</td>
<td>stress gauge</td>
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<tr>
<td></td>
<td>particulate contamination</td>
<td>defect inspection system</td>
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<tr>
<td></td>
<td>dielectric constant</td>
<td>C-V tester</td>
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<tr>
<td>Dopant processes (ion implant, diffusion)</td>
<td>uniformity</td>
<td>4-point probe, thermal wave, FTIR</td>
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<td></td>
<td>depth profile</td>
<td>SIMS, SRP</td>
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<tr>
<td>Planarization</td>
<td>removal rate and uniformity</td>
<td>reflectometer, ellipsometer</td>
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<tr>
<td></td>
<td>local/global planarity</td>
<td>surface profiler (high resolution)</td>
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<tr>
<td></td>
<td>slurry particles,</td>
<td>defect inspection system</td>
</tr>
<tr>
<td></td>
<td>micro-scratches</td>
<td></td>
</tr>
<tr>
<td>Etch</td>
<td>removal rate and uniformity</td>
<td>reflectometer</td>
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<tr>
<td></td>
<td>etch selectivity</td>
<td>SEM, AFM</td>
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<tr>
<td></td>
<td>etch profile</td>
<td>defect inspection system</td>
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<td></td>
<td>particulate contamination</td>
<td>defect inspection system</td>
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<td></td>
<td>pattern defects</td>
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<tr>
<td>Lithography</td>
<td>critical dimension</td>
<td>SEM</td>
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<td></td>
<td>overlay</td>
<td>optical overlay tool</td>
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<td></td>
<td>pattern defects</td>
<td>defect inspection system</td>
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<td></td>
<td>particulate contamination</td>
<td>defect inspection system</td>
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<tr>
<td>Yield monitoring</td>
<td>correlation of metrology and inspection results to yield</td>
<td>fab-wide data management system</td>
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To maintain control of the product, thin film quality is regularly monitored by tools that measure electrical, physical, optical and mechanical properties of films. Film parameters typically monitored include thickness and refractive index, resistivity and stress.

Another key area for process control is the reduction of defects that affect production yield. Defect reduction is typically achieved through an iterative process that involves detection of defects, classification of defects, identification of the source of the yield-limiting defects, correction of the process to eliminate or reduce the defect mechanism, then monitoring the process for yield excursions. The process is iterative in that, while the process is monitored for defect excursions, further defect analysis is conducted in parallel to drive continuous improvement of the yield.

Defect reduction is employed for five main applications:

- Inspection of bare wafers for contamination and surface quality, either during the wafer manufacturing process or as incoming material at the IC manufacturer
- Inspection of bare wafers used to monitor the cleanliness of process (or metrology) equipment
- Inspection of product wafers to decrease defectivity during the early phases of the product life cycle, and throughout the life cycle for continuous improvement
- Inspection of product wafers to monitor processes that introduce contamination, scratches or pattern defects
- Prediction of yield

Specific tool sets have been developed to address each of these needs. Bare wafer or unpatterned wafer inspection systems are optimized for scanning wafers at high throughput without the constraint of coping with the interference of pattern signals. Inspection of patterned wafers for yield improvement or process monitoring requires a system that not only copes with pattern, but provides high capture of key defect types at reasonable throughput. For yield prediction, the ability to integrate defect information—number, type, spatial signature—with other parameters such as electrical test results, becomes the key. Theory of operation as well as equipment design principles for each of these categories of defect inspection systems are described in Sec. 4.0 of this chapter.
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3.0  METROLOGY AND INSPECTION TRENDS: PAST, PRESENT, AND FUTURE

Metrology systems have undergone tremendous changes since the home-built bench top characterization tools of the 1960s. Inspection systems have gone through similar changes, moving from manual inspection by operators to automated inspection tools. As the semiconductor industry has grown and matured, metrology and inspection systems have kept pace. Measurement performance—predominantly sensitivity and repeatability—has steadily improved. The level of automation has dramatically increased, beginning with automated wafer handling, then pattern recognition, remote operation through development of the Semiconductor Equipment Communication Standard (SECS) protocol, development of automated algorithms that “learn” best measurement setups for monitoring a given product and process, and now automatic defect classification. These developments have supported the growing practice of making measurements on product wafers (rather than designated monitor wafers), a practice driven by the increase in wafer diameter to 200 mm, with a consequent rise in monitor wafer cost. Now, increasing attention is being paid to reliability, up-time and ease-of-use attributes, with the goal of increasing overall effectiveness of the equipment.

In the future, price-performance pressures on IC manufacturers will continue to be passed on to equipment manufacturers. The shift from off-line sampling to on-line control will accelerate, with increasing use of in-line and in situ measurements. Reliability and ease-of-use emphasis will drive the implementation of integrated, automated systems for measurement optimization, data interpretation, and adaptive feedback to the process equipment.

3.1  Trends in Metrology

Thin film measurements have progressed from simple single layer thickness measurements to multiple layer thickness and refractive index measurements. The trend towards multiple layer measurements has been partially driven by the increasing use of cluster deposition systems, where no opportunity exists for single layer measurements. Additionally, economics plays a role, in that as wafer sizes increase, cost savings can be realized by reducing the use of monitor wafers. In many cases, measurement of a layer on a product wafer requires measurement of the underlying layer(s) as well.
Measurement of film quality and stoichiometry has become as important as film thickness control. This is especially true with the advent of plasma enhanced CVD films such as silicon-rich anti-reflective oxynitride layers, since the film properties are strong functions of the process parameters such as plasma energy and reactant flow rates.[1]

At the same time, higher accuracy and tighter system-to-system matching are required to facilitate process transfer and reduce the time to start up new wafer fabs.

In the future, significant changes in the approach to process monitoring will occur. The trend will be to monitor processing parameters inside the processing chamber, not film characteristics; that is, process variables, not product variables. The shift from off-line sampling to on-line control will continue, with increasing use of in-line and in situ measurements. Prevention of process excursions by process control sensors should significantly reduce product loss.[2] Sensors can be equipment state (mechanical, electrical), process state (chemical/physical, temperature) or wafer state (product parameter, uniformity).

3.2 Trends in Defect Inspection

In the 1980s the first inspection systems were entirely manual and thus operator-intensive. Typically operators used a bright light source, and conducted visual inspections of incoming silicon, then manual microscope inspection of production wafers at various points in the process. Data was only as accurate and repeatable as the operators themselves. Results from these inspections were commonly written on paper and stored in binders and cabinets. Operators manually correlated defects to yield using two sheets of transparency paper for map-to-map comparisons. Over the intervening years advancements in IC technology, as well as economic pressures, have driven the need for enhancements in sensitivity, throughput, repeatability and automation for the defect reduction process.

In this section, we examine a few key trends in defect inspection:

- How the sensitivity of defect inspection systems has tracked critical dimensions of ICs—and how these systems are predicted to meet sensitivity needs for inspection of 0.18 and 0.13 μm devices, and beyond
- Challenges specific to inspecting 300 mm wafers
• Shifts in inspection strategies: from monitoring processes using bare wafers to using product wafers; towards differentiating yield-learning from in-line inspection; and looking forward to 
  *in situ* inspection and adaptive process control

• Increasing automation of inspection equipment using automated wafer handling, automated data transfer, mini-environments, and remote operation

• The movement towards automated systems for measurement optimization, data interpretation, and adaptive feedback to the process equipment

• The growing emphasis on cost of ownership, overall equipment effectiveness, and ease of use

**Sensitivity Challenges as Critical Dimensions Decrease.** A good rule of thumb in defect inspection is that the critical dimension (smallest linewidth) of the device determines the minimum size of defect likely to affect yield. At early steps in the process, defects as small as one-third the critical dimension can cause an electrical failure; at back-end levels, detecting defects about as large as the CD is sufficient to protect yield. Until recently DRAM devices had the smallest critical dimensions of any device on the market; at present, logic devices also have leading-edge critical dimensions. Historically manufacturers of inspection equipment watched DRAM manufacturers closely, striving to stay ahead of the design rule of the next memory device, so that the inspection system would be able to detect yield-limiting defects. Today we have various industry consortia, and in particular, the National Technology Roadmap for Semiconductors,\(^3\) to guide metrology and inspection equipment manufacturers in the design of next-generation inspection systems.

Figure 1 shows a history of how the detection limit of inspection systems has kept ahead of the critical dimension of IC devices. Unpatterned wafer inspection systems currently on the market can now detect defects as small as 80 nm, whereas patterned-wafer systems can detect defects less than 100 nm.\(^4\) The advances that have allowed inspection systems to continue to improve performance include:

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\(^3\) Quoted detection limits are referenced to NIST-traceable polystyrene latex spheres of known size deposited on clean, well-polished bare silicon wafers.
New optical designs
• More powerful and/or shorter-wavelength light sources
• More accurate wafer stages
• Higher resolution cameras
• Better signal processing algorithms

These evolutionary changes are ongoing for optical-based inspection systems, and the existing technology is proving to be extendible for inspection of 0.18 and 0.13 μm devices.

Figure 1. Critical dimension of integrated circuits (upper line) determines detection limit specifications for defect inspection systems (wide bands). Historically, smaller defects have been detectable using unpatterned systems, where the additional challenge of coping with pattern signal is not present.

An inspection technology based on scanning electron microscopy (SEM) is being used in addition to optical-based inspection systems for development of 0.25 and sub-0.25 μm processes. The biggest challenge for such high sensitivity inspection is providing cost-effective throughput. Despite this challenge, SEM-based automated inspection systems are used in advanced IC lines throughout the world.

SEM-based automated inspection systems provide two unique defect-detection capabilities. The first results from a SEM’s high resolution and large depth of focus: these systems can find small defects hidden in dense geometries where they can not be seen by optical microscopy. The second unique capability is the result of new, nontraditional SEM designs that
enable a properly optimized system to see contrast differences in electrically defective IC features. A common example of this type of defect is an electrical fault caused by voids in the metal that fills a contact or via. Here the structure of the metal plugs appears correct when viewed from the top surface, but a cross-section reveals that the metal doesn’t fill the bottom of the contact hole. In this and similar cases an electron-beam inspection tool that is designed to maximize the charge-induced voltage contrast effect may detect the problem as a slight difference in contrast of the feature in the SEM image. This voltage contrast imaging ability has opened up new applications for automated defect inspection tools. For further information on this capability, see Ref. 4.

**Inspection Challenges for 300 mm Wafers.** As pilot lines are coming up for production of devices on 300 mm wafers, inspection systems that accommodate these wafers are entering the market as well. Unpatterned inspection systems for 300 mm wafers have been on the market since early 1997, as these are required well in advance of production to allow process equipment vendors to develop their 300 mm equipment. Patterned wafer inspection systems are expected to be introduced in 1998. The main challenge for inspecting 300 mm wafers is cost of ownership; particularly the increased footprint of the system, and the challenge of maintaining high throughput. Compared to a 200 mm wafer, a 300 mm wafer has an area 2.25 times as large, and for most equipment designs, throughput scales roughly linearly with inspected area. Maintaining the same wafer-per-hour throughput specifications for 300 mm as currently available for 200 mm wafers could be achieved in one of several ways:

- Evolutionary improvements to subsystems including faster data rates, faster scanners, less reliance on scanning the stage since its mass is relatively large.
- Revolutionary new scanning designs, such as the spinning wafer strategy currently employed on some high throughput unpatterned wafer inspection systems.
- Adapting the sampling strategy to inspect a sparser fraction of the wafer area.

The high cost of 300 mm wafers also exerts economic pressure for devices to be built all the way to the edge of the wafer, and thus inspection closer to the wafer edge is necessary to protect yield.
3.3 Trends in Inspection Strategies

**Shift of Process Monitors from Bare Wafers to Production Wafers.** Monitor wafers have been used widely for tool qualification and process monitoring throughout the IC manufacturing process. Bare wafers have been run on every shift to qualify the equipment for use. In recent years, focused contamination reduction efforts on the equipment have enabled a better understanding and control of the contribution of the process equipment to contamination of product wafers. Defect types and mechanisms are better characterized, and programs for cleaning or preventive maintenance of the equipment are in place. Thus the need for such rigorous equipment monitoring is predicted to decrease.

The cost of monitor wafers has always been significant, and has become more so with the introduction of 200 mm wafers and the imminent move to 300 mm. Thus, more fabs have begun to relegate the use of monitor wafers to bringing up new tools and diagnosing specific contamination problems, while using product wafers to monitor their processes.

Interestingly, the predicted decline in use of monitor wafers has not been reflected in declining sales of unpatterned wafer inspection equipment. The rapid expansion in the semiconductor industry during the 1990s has driven strong growth in unpatterned wafer inspection system sales, dominating any effects of decreasing monitor wafer use.

**Looking Ahead to In Situ Inspection and Adaptive Process Control.** A logical extension to process monitoring is to incorporate the inspection system into the process tool itself. An in situ inspection system could provide information to the process tool, so that when defect excursions are detected, the process tool could be flagged and shut down, or perhaps even adjusted to eliminate the defect mechanism. Having the inspection tool provide closed-loop control of the defectivity of the process is an example of adaptive process control.

The barriers that currently exist for achieving this scenario are significant. At present, the capability of a stand-alone inspection system would be difficult to reproduce inside the economic and physical constraints of a process chamber. Also, understanding how to adapt a process to eliminate the defects detected by the inspection system is nontrivial for a team of experienced engineers. Designing an expert system to replace that body of knowledge would be a significant challenge. However, strong economic pressures exist to reduce the cost of the defect reduction process, and part of the solution may involve meeting the challenges of in situ inspection.
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An alternative approach—and another example of adaptive process control—is to provide tighter control of the process parameters through improvements to in situ environmental sensors. This more direct, causal means of addressing process control issues involves rapid measurement and feedback based on process parameters, e.g., temperature and pressure. In contrast, an in situ inspection system measures the effects of out-of-control process parameters: defects incurred on the product wafer.

**Trends in Automation of Wafer Inspection Equipment.** An ongoing trend for IC inspection has been a growing emphasis on automation of the inspection process: automating the inspection and defect review equipment itself, and integrating it with yield data using defect data management systems. The cost of ownership of the inspection process decreases as automation is introduced, because trained engineers and operators can focus elsewhere in the fab. Repeatability and accuracy increase as the subjective nature of human judgment is replaced by standard algorithms. Automation facilitates the de-localization of a given manufacturing process, allowing the process to be copied exactly from fab to fab around the world. Automation can also support a more rapid return on investment by helping ramp a process to yield in a shorter time.

Automation began with the introduction of automated wafer handling using mechanical robots, and has expanded its scope to include other subsystems within the wafer inspection and defect review tools. In an effort to reduce operator error and increase throughput, Optical Character Recognition (OCR) and Bar Code Reading (BCR) were incorporated into these tools to read lot and wafer information during automatic inspection or review sequences. Signal towers communicate the status of the systems through colored or flashing lights, and mini-environments and pods enclose the wafer cassette or the inspection or review tool to enhance the cleanliness of the local environment.

The development of the Semiconductor Equipment Communication Standard (SECS) protocol allows a host computer to operate the inspection and review systems remotely, initiating automatic inspection and controlling the flow of data from the inspection tool to the review tool to the fab database. One benefit of this automation is the reduction of operator error in the selection of measurement recipes and data entry of basic lot information.

Automated defect data management systems were introduced to deal with the tremendous amount of data generated by automatic defect inspection systems. Yield correlation is one of the primary tasks of the defect data management system. The newest systems automate yield
correlation by overlaying maps of electrical test results with defect maps, bringing in defect type information from review stations, then delivering yield statistics by process level and defect types. This information has given the defect reduction engineer the ability to focus quickly on the defect types and process layers that most affect yield.

Defect data management systems have also adopted the use of statistical process control (SPC) monitors that flag out-of-control defect data. In a typical fab today, the inspection tools automatically feed data (defect count, type, intensity, spatial signature) to the data management system. The data management system constructs SPC charts from the incoming data and checks for out-of-control status (using conditions predetermined by the engineer). If the data are out-of-control, the system alerts the engineer by e-mail or pager.

Automated transfer of data from the inspection system to the review station represented a tremendous step forward in automating the inspection process. Review stations—traditional white-light, laser confocal or SEM; stand-alone or incorporated into the inspection system—take the coordinates of the defects reported by the inspection system and automatically drive to those locations on the wafer. The defects are then quickly reviewed, and classified either manually or using automatic defect classification (discussed in next section). This capability led to faster and better understanding of defect origins and mechanisms and their impact on yield.

**Trends in Automation through Advanced Algorithms.** A further step in automation is the use of algorithms to replace human operators for optimization of system parameters to create “recipes” to inspect a given level for a given set of defect types, and automatic defect classification (ADC). Advancements in these algorithms are likely to reduce cost of ownership of the inspection process substantially over the next few years.

**Automated Recipe Creation Procedures.** When a new device and/or process level is inspected for the first time, a recipe has to be generated that contains optimized measurement parameters such as optical and signal processing configurations. The procedures for creating these recipes—and the number of parameters involved—have become more complex as inspection technology has advanced. Thus, automation of the procedure has escalated in importance. Automated recipe creation is particularly important in an ASIC fab in which many different products are manufactured, and during an excursion when quick recipe creation at a nonstandard inspection point may be needed.
Simply stated, automated recipe creation works by evaluating changes in the signal-to-noise ratio as the different optical and signal-processing parameters are systematically varied. A brute-force approach would try every combination of every parameter. For today’s complex systems, the number of variables would make this a cost-prohibitive task. A more elegant approach would make use of existing knowledge, at least to eliminate certain combinations of parameters, and perhaps even to find an efficient path through the multivariable space that arrives at a unique, repeatable solution.

Today, automated recipe creation results in a recipe that sometimes can benefit from further optimization by a well-trained engineer. Improving automated recipe-creation algorithms is an area of focus for developers of wafer inspection tools, due to its importance in increasing the overall effectiveness of the equipment.

**Automatic Defect Classification (ADC).** One of the biggest bottlenecks in the inspection process is classification of defects, a necessary step to determining and eliminating their source. At present, most defect classification is still manual, requiring a trained operator to judge a microscope image and sort defects into categories based on the operator’s experience (often using a reference book containing pictures of “typical” defects). This process is limited in speed, accuracy and repeatability, and thus does not fit well into an industry driven by time to market and cost control.

For these reasons automatic defect classification (ADC) has gained tremendous attention of late. ADC has begun to reduce significantly the amount of manual classification needed, increasing the throughput of the classification process, and reducing subjectivity and error from operator classification.\[5\] ADC thus enables more and better analysis of defect information.

The current implementation of ADC begins first by teaching the system to recognize the defect types by providing it with clear example images. Then during actual automatic classification a review microscope (off-line or built into the inspection tool) drives to the coordinates of the detected event on the wafer and re-detects the event within the field of view. The review station generates a digital image of the event using traditional optical, confocal or SEM-based techniques. The ADC algorithm then extracts features from the event and compares those features statistically to the example images. The output includes a classification for the event along with a goodness-of-fit value that describes the image’s similarity to the images from the example defects in its class.
The ultimate implementation of ADC would be for classification to happen in parallel with inspection, without having an impact on inspection throughput. Partial accomplishment of the goal of real-time ADC is available today using the techniques of real-time grouping and/or spatial signature analysis.

Real-time grouping (also called real-time defect classification or RTDC) makes maximum use of whatever descriptive information can be recorded during inspection. The intensity of the scattering signal; the difference in intensity seen by collectors spanning different solid angles of the scattering hemisphere; the gray scale intensity or perimeter of the pixels comprising the image—these are examples of types of information that might be captured in real time by an optical inspection system. Separating defects into coarse groups such as “large,” “small,” “bright,” “dark,” and so forth can now be accomplished by many inspection systems during inspection.

The spatial relationship between detected events (also called the signature) can be used to discriminate between typical extended defects found on wafer surfaces. Novel clustering algorithms are used to capture the spatial signature of extended defect types such as polishing scratches, handling damage, crystallographic defects, voids, foreign particles and stress related defects.

Real-time grouping reduces the number of detected events that need to be classified manually or using high-resolution ADC. Every step towards improving time to results provides value for cost-effective IC manufacturing.

The Growing Emphasis on Cost of Ownership, Overall Equipment Effectiveness, and Ease of Use. Many of the trends in inspection technology discussed above are driven by the need for integrated circuits to be brought to market quickly and at contained cost. The challenge to the inspection part of the process is to provide more defect information in an increasingly cost-effective manner. The concept of lowering cost of ownership (COO) has been replaced recently with a new concept: overall equipment effectiveness (OEE). As applied to inspection equipment, COO includes the purchase price of the system and its throughput, whereas OEE also weights heavily those characteristics that enable a system to provide the best defect information in the fastest time, with maximum ease of use and minimum cost, in a production environment.

For inspection equipment, key elements of high overall equipment effectiveness include:
• High defect capture probability, i.e., high probability of detecting a representative fraction of defects from the population of all defect types present on the wafer.

• High correlation of detected events with yield-limiting defects: low false or nuisance counts.

• High throughput.

• Low system purchase price.

• High reliability: high repeatability of measurements; minimum downtime; minimum maintenance.

• System matching: highly correlated results using systems of same model number; easy transfer of recipes between tools and between fabs.

• Ease of use: automated recipe learns and operation with minimum intervention of highly paid personnel.

• Maximum integration of defect inspection, review, classification and analysis process.

Not all of these elements may be captured in equations measuring OEE, but all of them are key elements for operating the defect reduction process at highest possible efficiency and lowest cost.

The final element of successful yield enhancement through defect reduction is close communication between defect metrology and process engineering groups. A highly effective defect reduction program seamlessly integrated with a strong process engineering program is well positioned for success in the semiconductor market.

4.0 THEORY OF OPERATION, EQUIPMENT DESIGN PRINCIPLES, MAIN APPLICATIONS, AND STRENGTHS AND LIMITATIONS OF METROLOGY AND INSPECTION SYSTEMS

This section briefly discusses the theory of operation, main applications, and the strengths and limitations of several thin film metrology systems. For a more detailed theoretical discussion, the reader is encouraged to consult Ref. 6.
4.1 Film Thickness Measurement Systems

**Theory of Operation.** The common optical measurement techniques include reflectometry (using unpolarized or polarized light) and ellipsometry. System implementations use multiple wavelength or multiple angles of incidence. Regardless of the type of system, the data analysis methods that transform the directly measured quantities to the parameters of interest such as thickness and refractive index are similar. The measurement recipe contains information about the film stack to be measured, such as the type of material, approximate thickness of the material, and (implicitly) the refractive index of the material. The Fresnel reflectance equations are used to calculate theoretical spectra for the film stack. The calculated spectra are compared with the measured spectra, and regression analysis is performed by varying the parameters of interest until the best fit is obtained. The best-fit values are reported, along with a figure of merit referred to as the goodness-of-fit (GOF).

The capability of a system to report parameters of interest such as thickness and refractive index values derives from the amount and type of raw data measured by the system. Generally, the information content of the raw measured values (for one wavelength and one angle of incidence) increases in the following order: unpolarized reflectometry ($R$); polarized reflectometry ($R_p$ and $R_s$); and ellipsometry ($\Psi$ and $\Delta$). Although both polarized reflectometry and ellipsometry measure two values at each wavelength and angle, ellipsometry is unquestionably the more powerful technique for a number of reasons.\[7\] Ellipsometry measures the phase of the reflected light (not just amplitude). Ellipsometric measurements are relatively insensitive to intensity fluctuations of the illumination source, temperature drifts of electronic components, and macroscopic roughness. Macroscopic roughness causes light loss by scattering incident light away from the detector, which can be a serious problem in reflectometry but not in ellipsometry, for which absolute intensity measurements are not required. Ellipsometry is inherently a double beam technique, because one polarization component serves as amplitude and phase reference for the other.\[8\]

The other system implementation choice is to collect data using multiple angles of incidence or using multiple wavelengths. Data collected using multiple wavelengths generally have higher information content than data collected using multiple angles of incidence. An examination of the phase term $\phi$ of the Fresnel reflectance equations shows a first order change with wavelength, while a change with angle is contained within a sine term:
Eq. (1) \[ \phi = 4\pi \frac{d}{\lambda} n_1 \cos \theta_i = 4\pi \frac{d}{\lambda} \sqrt{n_1^2 - \sin^2 \theta_0} \]

where \( \theta_i \) is the refracted angle of light in the film, \( \theta_0 \) is the incident angle (in ambient), \( d \) is film thickness, and \( n \) is refractive index.

The consequence is higher sensitivity to film changes with wavelength than angle. (For oxide, the percentage change in the phase term with wavelength from 200 to 800 nm is an order of magnitude higher than with a change in angle from 0 to 90°). Additionally, multiple wavelength systems take advantage of the fact that a physical property of a film, the refractive index, is a function of the illumination wavelength (refractive index dispersion) as illustrated in Fig. 2. Refractive index is not a function of the angle of incidence of the illumination. Therefore, little information about the physical properties of the material can be deduced by measurements using multiple angles. Conversely, the RI dispersion difference between different materials can be exploited by multiple wavelength systems. The consequence is that a change in the thickness (or RI) of one film in a multiple-layer film stack will change the measured spectra differently than a change in a different layer. The different optical penetration depth as a function of wavelength provides additional information to resolve the thicknesses of several layers in multiple layer structures.\(^{[8]}\) This implies that a multiple wavelength metrology system will be sensitive to, and be able to differentiate between, thickness and index changes in multiple-layer film stacks. Spectroscopic ellipsometry provides the highest level of capability of the optical thin film measurement techniques, by collecting ellipsometric data over a large range of wavelengths. Only spectroscopic ellipsometry uses all properties of polarized light: amplitude, phase, and wavelength.

Unpolarized reflectometers measure reflectance (\( R \)) versus wavelength at a single angle of incidence (normal to the wafer). Light reflecting from the top surface of the film interferes with light reflecting from the film to substrate interface, resulting in a periodic variation in reflectance as a function of wavelength spectrum.

Polarized reflectometers measure polarized reflectance (\( R_p, R_s \)) versus angle of incidence at a single wavelength. A high numerical aperture objective lens is used to achieve a small spot size, resulting in multiple angles of incidence. Reflectometers, whether using polarized or unpolarized light, require calibration to known standard wafers (referred
to as a referenced technique). These wafers can be either bare silicon or wafers of a “known thickness.” This is because reflectometers need to know very accurately the value of absolute reflectance, and to be able to compensate for intensity losses through aging of the illumination source, efficiency of the metrology system optics, etc. (referred to as optical throughput).

Ellipsometers measure the amplitude ratio ($\Psi$) and phase change ($\Delta$) of polarized light upon reflection from a sample. Single wavelength ellipsometers are available with a high numerical aperture objective lens to achieve a small spot size, resulting in multiple angles of incidence. The use of multiple angles eliminates the problem of thickness order ambiguity.

![Figure 2](image_url). RI dispersion of materials commonly used in the semiconductor industry. The refractive index $n$ is the upper plot; the extinction coefficient $k$ is the lower plot.
Spectroscopic ellipsometers measure amplitude ratio and phase change versus wavelength at a single angle of incidence. (Research grade spectroscopic ellipsometer systems also offer multiple angles of incidence for material characterization). The angle of incidence is typically 70–75°, near the Brewster angle, selected for its maximum sensitivity to changes in film thickness on silicon substrates (Fig. 3). Attributes of commercially available instruments are summarized in Table 2.

![Graph showing sensitivity of SE technology](image)

**Figure 3.** Sensitivity of SE technology (phase change term, cos Δ) to very thin oxide thickness changes when operating near the Brewster angle.

### Table 2. Typical Instrument Configurations Used in Semiconductor Process Monitoring

<table>
<thead>
<tr>
<th>Property of Light Used</th>
<th>Angle of Incidence</th>
<th>Referenced Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Amplitude</td>
<td>Phase</td>
</tr>
<tr>
<td>Unpolarized Reflectometer</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td>Polarized Reflectometer</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td>Focused Beam Ellipsometer</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Spectroscopic Ellipsometer</td>
<td>yes</td>
<td>yes</td>
</tr>
</tbody>
</table>
Main Applications. Thin film metrology systems are used in every process module in semiconductor fabs; to monitor thickness and/or refractive index uniformity in deposition and diffusion areas, for removal rate and uniformity in etch and planarization areas, and to monitor reflectivity in metal deposition or photolithography areas. Depending on the measurement technique, semitransparent films from several angstroms to several microns in thickness can be measured. Historically, ellipsometry was used in diffusion areas for very thin films, and reflectometry was a general thin film tool. These distinctions are diminishing as advances are made in measurement technology, and many systems now incorporate more than one type of technology.

Strengths. The ability of technologies such as spectroscopic ellipsometry to simultaneously and independently measure multiple film thicknesses and refractive indices offers opportunities to semiconductor manufacturers for reduced cost and enhanced process control. Wafer fabrication costs can be reduced through decreased use of monitor wafers. This is especially important for 200 mm and 300 mm wafers. As an example, the ability to measure nitride over amorphous silicon over oxide in a DRAM structure means that a nitride on silicon monitor wafer can be eliminated. Additionally, the increasing use of multi-process chamber cluster deposition tools requires the ability to measure multiple-layer film stacks, since there is no opportunity to measure each layer after it is deposited.

Semiconductor fabs are becoming more interested in monitoring and controlling film quality, as opposed to merely film thickness. The refractive index of a film is a key indicator of film composition. For films such as amorphous silicon and polycrystalline silicon, the extinction coefficient \( k \) (part of the complex refractive index \( \tilde{N} = n + ik \) ) is directly related to the crystallinity of the film. Process temperature (of the deposition or anneal step) determines the crystallinity. New materials such as silicon-rich oxynitrides and nitrides are increasingly used as anti-reflective layers. The stoichiometry of these films can also be monitored by UV spectroscopic ellipsometry measurement of refractive index. Therefore, the ability to measure refractive index, not only of a single-layer film, but also of a film in a multiple-layer film stack, is beneficial.

Limitations. Reflectometers require calibration using wafers of known reflectance, and can be subject to measurement drift over time. Single wavelength ellipsometry is known for limitations such as thickness order uncertainty, and thickness regions where refractive index cannot be calculated. Multiple angle systems eliminate thickness order ambiguity for single
layer films. Use of a small spot size and a single wavelength can be problematic when measuring rough films that scatter light.

All optical tools require a film stack model for their regression analysis. Accuracy can be affected by selection of an appropriate refractive index dispersion model. Materials which do not have a consistent spatial composition, e.g., their refractive index changes with depth, require special models to measure correctly.

Future gate dielectric process control will be a difficult challenge, if composition information is required as well as thickness uniformity. Increasing attention will need to be paid to the interface between the gate dielectric and the silicon substrate for proper measurement accuracy. There is also an inherent difficulty in monitoring metrology system stability at a 4 nm gate dielectric thickness, as these wafers tend to change thickness over time due to environmental effects.

Measurement spot size considerations result in the use of test structures, typically located in the scribe lines, since no metrology system can currently measure inside of submicron features.

4.2 Resistivity Measurement Systems

Four-Point Probes. Theory of Operation. Four-point probe (4PP) systems measure sheet resistance ($R_s$), the local resistance of a sheet of material, in units of ohms/square. Sheet resistance is expressed in the equation $R_s = R_b/t$, where $t$ is the thickness of the conductive layer, and $R_b$ is the bulk resistivity (ohm-cm) of the layer. For a material with constant bulk resistivity, the sheet resistance is only a function of thickness. A four-point probe consists of four spring-loaded conductive probes (usually in a linear array) which are placed in contact with the material whose sheet resistance is to be measured. (The four-point probe technique requires some isolating junction or blocking layer to the DC current used).

Typically, a known current is forced between the outer probes, and the resulting voltage across the inner two is measured. Ohm’s Law ($V = IR$) is then used, with a geometrical correction factor, to calculate the sheet resistance of the material. To compensate for geometric errors arising from variations in probe tip spacing and proximity to the wafer edge, the dual configuration technique was developed. A second measurement is made, with current forced through pins 1 and 3, and voltage measured between pins 2 and 4 (Fig. 4). The geometrical correction factor can then be calculated based on the ratio of the measured resistivities.
Figure 4. Dual configuration four-point probe measurement setup.

Main Applications. Resistivity systems are used throughout the fab to measure any conductive semiconductor layer; from incoming silicon wafer inspection, to metal deposition and etch/planarization for removal rate and uniformity, to dopant uniformity in diffusion and ion implant operations. Ion implantation was the first process to extensively use 4PP for process control, and also the first to exploit the power of full wafer uniformity mapping as a process diagnostic. The normal range for sheet resistance in semiconductor processing is from less than 0.02 ohm/square for aluminum films, to about 1 mega-ohm/square for low dose implants into silicon.

Strengths. The four-point probe is the most common tool used to measure sheet resistance, due to its accuracy, repeatability (~ 0.2% 1σ), and relatively low cost. The most accurate systems employ temperature compensation, to account for variations in the resistance that occur with variations in ambient temperature. Temperature compensation is especially important to achieve system to system accuracy matching, an increasingly common requirement not only within a fab, but also for process transfers between fabs.
Limitations. Because the 4PP technique is based on physical contact with the wafer, its use is limited to monitor wafers. Care must be taken to ensure low contact resistance between the probe tips and the conductive layer. Probe tip “conditioning” and qualification routines have been developed to manage this concern.

The most challenging applications for 4PP are low energy (ultrashallow junction), low dose (high sheet resistance) ion implants. These processes require enough probe tip pressure to penetrate down to a more conductive depth but not so far as to penetrate past the junction. Reductions in measurement edge exclusion are also required.

Eddy Current (Mutual Inductance). Theory of Operation. Eddy current or mutual inductance techniques determine sheet resistance of a film by creating a time-varying magnetic field from a coil (“probe head”). The coil radiates energy, is placed close to the conductive layer, and eddy currents are generated by the absorbed energy in the conductive layer. The eddy currents in turn create a magnetic field that induces a reverse current in the coil (hence the term mutual inductance). The sheet resistance of the conductive layer determines how much current is induced in the $R_s$ sensing circuit. The more conductive the film, the more energy is trapped in the film to create eddy currents. The magnetic field drops off with distance (depth into the film).

Various configurations exist: “single-side,” where the wafer is placed under the inductive coil (Fig. 5), and “dual-side,” where the wafer is placed inside the turns of the inductive coil. The dual-side approach, developed first, typically has a larger spot size and greater measurement range. The measurement is made in a transmission mode. Decreasing the spot size requires decreasing the distance between the coils. A practical limit of spot size results from clearance between the sample and the coils. The single-side approach, essentially a reflection measurement, offers advantages of higher sensitivity to the top layer than the underlying layer/substrate, smaller measurement spot size, and reduced edge effect.

Main Applications. Historically, eddy current systems have been used for incoming inspection of resistivity of prime silicon wafers. More recently, as the RC time delay of interconnect layers has become a gating item to increasing device speeds, the technique has been applied to measurement of blanket metal layers prior to patterning.\textsuperscript{[11]} Since the metal layer is unpatterned, it supports eddy current formation. Underlying metal films are patterned, which prevents the formation of eddy currents. The typical resistance range covered by eddy current systems is 0.001~50 ohms/square for single-side and 0.01~5000 ohms/square for double-side.
**Strengths.** Because it is a non-contact technique, it can be used on product wafers. This is desirable for several reasons: significant cost savings by reducing monitor wafers, better equipment utilization by processing fewer monitors, and improved process control by measuring actual product wafers.

**Limitations.** Since the magnetic field penetrates through the top metal layer of interest, the technique works best when the resistivity of the underlying layers/substrate is high relative to that of the conductive metal layer (e.g., typical memory applications). In the case of low resistivity substrates, the technique can be extended somewhat by calibration or software correlation. Eddy current systems are typically calibrated using four-point probes. Spot size can be an issue as smaller measurement edge exclusions are required.

### 4.3 Stress Measurement Systems

Although properties like film thickness, density, and resistivity can be immediately related to device performance, the level of stress in a thin film is more important to long term device reliability and lifetime.

Stress in a thin film develops primarily during the deposition process and consists of two components: the intrinsic stress and the extrinsic stress. The intrinsic stress is the component of stress in the film caused by the deposition process itself. For example, a slowly sputtered metal film deposited onto a heated substrate will grow with near zero stress, although the film structure may be metastable. By contrast, a chemical vapor deposition (CVD) oxide film can have a highly variable stress level depending on
film density, moisture content or residual reactants such as hydrogen. Within a wide range, the intrinsic film stress for most materials can be controlled by the process parameters of the deposition system.

The extrinsic stress is the component of stress caused by a change in the external conditions on the wafer. For example, most films have a thermal expansion coefficient different from the silicon substrate, so when the temperature changes, the film and substrate try to expand or contract by different amounts. However, because they are bound together, a stress will develop in both the film and the substrate. Since films are typically deposited above room temperature, the process of cooling after deposition will introduce a thermal component of stress into most films. The total film stress will be the sum of the intrinsic and extrinsic components.

**Theory of Operation.** To maintain static equilibrium, the forces and moments in the film must balance the forces and moments in the substrate, which requires a shape change of the wafer when a stressed film is deposited. For the geometry of a thin uniform film deposited on a much thicker, but platelike wafer, the shape change caused by the addition of a film will be a uniform bowing of the wafer like a spherical bowl or dome, but several assumptions are involved:

- The substrate can be treated as a plate which simplifies the elasticity equations. The basic requirement for meeting the plate geometry is that the characteristic length dimension be more than about 10 times the thickness. The approximation errors can be significant unless the ratio is notably higher, and in the semiconductor industry, a typical 200 mm wafer is under 1 mm thick. The ratio is well over 100:1, so the plate approximation is quite accurate.

- The film is uniform and homogeneous in any feature that can influence stress, primarily the thickness. The stress in a film deposited only on one face of a wafer will give rise to forces and bending moments that change the shape of the wafer. If the film is uniform, the forces will be evenly distributed causing an even shape change. The stress is biaxial, so the elasticity equations can be solved to relate radius of curvature of the resulting shape change to the film stress. Any significant variations in the film thickness, chemical composition or internal structure of the film can lead to nonuniform bending and an inaccurate average stress calculation.
• The film is much thinner than the substrate. The assumption leads to the simplest equation to relate film stress to change in curvature of the wafer which is called the Stoney equation (Eq. 2). Most researchers and equipment companies use the Stoney equation to calculate stress. The equation relies only on the elastic properties of the substrate, so the stress in any film material regardless of quality can be determined. However, if the film thickness reaches about 5% of the substrate thickness, the calculation error will be about 10%. Again, in the semiconductor industry, films are typically less than a few microns on substrates over 500 microns, so the ratio is under 1% and the error is insignificant.

An important point about the typical commercial equipment available to determine stress is that all systems measure curvature or shape. The raw data must be analyzed to yield a radius of curvature before and after film deposition. The change in radius is then used to calculate stress. A tool to accurately and conveniently measure film stress directly does not exist. The stress calculation is based on the Stoney equation,

\[
\sigma_f = \frac{1}{6} \frac{E_s}{1-V_s} \frac{t_s^2}{t_f} \left[ \frac{1}{R_f} - \frac{1}{R_s} \right]
\]

Eq. (2)

The subscripts \(s\) and \(f\) refer to the substrate and film, respectively, while \(E\) is Young’s modulus, \(v\) is Poisson’s ratio, \(t\) is thickness and \(R\) is the measured radius of curvature.

**Main Applications.** Film stress can give rise to a number of problems that can lead to failure in the operation of an integrated circuit, so determining film stress is important for maintaining a reliable process. Two common issues are cracks forming in highly stressed, brittle passivation layers, and voids forming and growing in aluminum lines. Stress also contributes to reliability failures such as electromigration. Other issues include debonding of high stress metal films like tantalum, or sorption of volatiles like water and organic solvents from porous films.

Stress measurement can be divided into two categories with distinctly different goals: testing done at room temperature and testing done while thermally cycling a wafer. Room temperature testing is typically used for monitoring an established deposition process for an SPC style control.
Thermal cycling is typically used for process development and materials characterization.

**Room Temperature Testing.** Room temperature testing provides basic process control data. The stress level in a film can be influenced by controlling the deposition parameters such as temperature, pressure, reactant flow rates and input power, so film stress can be used as part of the process development. Once an acceptable set of deposition conditions are established, continual monitoring of the resultant film stress will give a measure of the long-term stability of the deposition system. The results are ideally suited to a simple SPC control on the film deposition process.

Advanced stress measurement systems include stress mapping capabilities over the surface of the wafer. Information about the stress distribution throughout the film is especially valuable in determining the uniformity of a deposition process beyond basic film thickness uniformity results.

**Thermal Cycle Testing.** Thermal cycling of a film-wafer sample provides data that delves more deeply into the mechanisms of stress generation and evolution. Generally, the thermal expansion coefficient of the film and substrate will be different, so changing the sample temperature will impose a thermal component of strain that can lead to high stresses in the film.

Optical techniques are required in which a laser can be aimed through a transparent window to measure curvature and stress continuously during thermal cycling. Numerous thin film effects have been observed including yield behavior in metals, effusion of volatiles from porous films, phase changes, and hillock formation.

Thermal testing allows for a more fundamental examination of the mechanical behavior of thin film materials. The stress data obtained during thermal cycling can be used to approximately determine thermal expansion coefficient, modulus of elasticity and some activation energies. The technique has also been used on polymeric films to determine glass transition temperatures.

**Deflection Measurement Techniques.** Several techniques relying on differing technologies have been developed to measure film stress, but all basically measure the average radius of curvature of a wafer before and after the film deposition. An overview of four measurement techniques will be given: one directly measures bow optically, and the other three scan the shape of the wafer surface using either a two plate capacitor, a contact stylus profiler, or a laser lever.
Bow Measurements. The most direct measurement technique uses a fiber optic sensor to determine the bow at the wafer center before and after film deposition. The wafer is supported by a knife edge ring of diameter \( D \), so the bow, \( d \), is related to the radius of curvature by the equation

Eq. (3) \[ R = \frac{D^2}{8d} \]

The change in radius caused by the film is related to the stress using the Stoney equation. The fiber optic sensors can measure bow changes with a resolution in the range of 0.05 microns, but using one central measurement to represent the entire wafer shape limits the accuracy of the stress measurement. Advanced versions of these systems include multiple probes that allow deflection and stress mapping over the entire wafer.

Strengths of this technique are that it is simple, non-contact, and sensitive. Limitations are a limited amount of data (one data point) and poor thermal performance.

Capacitance Measurements. The capacitance probe technique measures the capacitance between a small probe and the surface of the wafer from which the distance to the wafer can be determined. By using probes simultaneously on the front and back surface of the wafer, the wafer thickness is determined along with the wafer position between the two probes. The wafer is automatically moved through the probe to obtain a map of thickness and shape. Using the Stoney equation and numerically fitting the shape data, average stress or stress maps can be obtained. The capacitance probes determine bow with a repeatability (1\( \sigma \)) of about 0.5 microns and wafer thickness repeatability (1\( \sigma \)) of about 0.05 microns.

Strengths of this technique are high measurement speed, so a large quantity of data can be collected. A limitation is the lack of thermal capability.

Profilometry. Profilometry uses a contact stylus sensor to determine step heights and general surface topography over a wafer. By scanning over a sufficiently large area of the wafer, a map of the wafer shape can be obtained before and after film deposition. The data are fit to determine the change in radius and put into the Stoney equation. Profilers can achieve exceptional performance with approximately 0.01 micron repeatability (1\( \sigma \)) in vertical resolution of the surface shape.

The main strength of profilometry is its high sensitivity. Limitations are slow measurement speed, the probe tip contacts the sample, no thermal capability, and full wafer data must be “stitched” together.
**Optical Lever Measurements.** Optical lever systems aim a laser at the surface of a wafer and measure the direction of the reflected beam using a position sensitive light detector. From knowledge of the system geometry, the wafer surface normal and therefore the tangent are measured. Scanning over the wafer surface provides a map of tangent versus position which is fit to determine the change in radius and put into the Stoney equation. Optical systems can determine bow with a repeatability (1σ) of about 0.5 microns.

Strengths include simplicity, measurement speed, and thermal capability. Limitations are that the laser is diffracted by patterned wafers, and interference effects occur in some films.

### 4.4 Defect Inspection Systems

This section covers theory of operation and equipment design principles, main applications, and strengths and limitations for unpatterned and patterned wafer inspection systems. The section is organized as follows:

- General Theory of Inspection System Operation and Design
  - Optical Imaging
  - Optical Scattering
- Unpatterned Inspection Systems
  - Applications
  - Strengths and Limitations
- Patterned Inspection Systems
  - Applications
  - Strengths and Limitations

**General Theory of Inspection System Operation and Design.** Very generally, an inspection system must be able to detect the presence of the defects on the wafer and identify their spatial locations. Defect detection requires some kind of contrast mechanism to distinguish the defect from its surroundings. Typical contrast mechanisms include those associated with optical imaging (both dark-field and bright-field); optical scattering (dark-field); and electron imaging. In this section we will focus on the optical techniques as these are the most commonly used in monitoring defectivity for IC production today.
In order to discuss the technology of optical inspection, some usage conventions are helpful. On a perfect mirror surface, the light incident at a given angle reflects at the equivalent angle in the plane of incidence to form the *specular* beam (Fig. 6). On a real surface some of this light will be *scattered*: absorbed, diffracted or otherwise directed to an angle outside the specular beam. Particles, scratches, surface roughness, local device topography or interfaces between different materials can cause light to scatter.

**Figure 6.** Simplified schematic of optical subsystem for optical defect detection. There are three beams of light: the incident beam, the specular beam and a ray representing the scattered light. The plane formed by the wafer surface and the scattered light beam is at an angle $\phi_s$ from the incident plane, which is formed by the wafer surface and the incident beam. The specular beam lies in the incident plane.

**Optical Imaging.** For optical imaging an area of the surface of the wafer is illuminated uniformly. Features and defects within the illuminated area scatter the light according to their material properties and topography. A series of lenses captures the specular beam (bright-field design) or scattered light (dark-field design), imaging its spatial variation on the wafer surface onto an area detector such as a CCD camera or TDI detector. The information conveyed by the image arises from the differences in the way the defects and features on the surface scatter light. Defects are detected by comparing the digital image of one part of a die with the image from equivalent areas in neighboring dies, and identifying differences.
The resolution of an optical imaging system is determined by the pixel size of the area detector, the spectrum of the light source and photon density of the illuminated area, and the optical contrast between the defect and its surroundings.

**Optical Scattering.** For optical scattering, a small spot of high photon density is illuminated on the wafer surface. Features and defects within the illuminated spot scatter light according to their material properties and topography. The specular beam is discarded, and the scattered light is collected over a particular solid angle, then focused onto a point detector such as a photomultiplier tube (PMT). In essence, the amount of light scattered by that illuminated area into a given solid angle is recorded. Various signal processing schemes are then employed to determine whether or not a defect is present at the location of the illuminated spot. For example, this signal could be compared with a signal from an equivalent area elsewhere on the wafer. The entire surface of the wafer is sampled by moving the beam across the wafer, or the wafer under the beam, or a combination thereof.

The resolution of an optical scattering inspection system is determined by the ratio of the light scattered by the defect to that scattered by its surroundings. This is in turn determined by the photon density of the illuminated spot, the wavelength and incident polarization of the light source, the solid angle(s) subtended by the collection optics, the polarization collected in the detector, and details of the optical and topographic properties of the defect and its local environment.

Thus the probability of capturing a defect of a particular shape, material and size, residing on a particular film stack and in the presence of a given local device topography varies with many parameters. The specifics of the optical design of the inspection system—in particular the angles of incidence and of collection—influence the capture probability, as does the signal processing technique. Capture probabilities can be predicted rather well through mathematical modeling for spherical particles on bare wafers.[13] For specific defect types on patterned wafers, simple models can be constructed that also produce useful results.[14]

**Unpatterned Wafer Inspection Systems.** Typically dark-field optical scattering is used for detection of particles, scratches and crystal defects of unpatterned wafers. The complexities of the pattern signal are not present, and the cost of the unpatterned wafer is lower than that of the product wafer. For cost-effective inspection, throughput is very important in unpatterned wafer applications.
The original unpatterned wafer inspection systems used a red helium neon laser (633 nm), but in the early 1990s a switch was made to a blue argon ion laser (488 nm) whose shorter wavelength provides increased sensitivity.\[^{15}\] Unpatterned wafer inspection systems use either a normal-incidence or oblique-incidence design (Fig. 7).

\textbf{Figure 7.} (a) A normal-incident laser-scattering system avoids the specular beam, but collects a large portion of the light in the hemisphere above the wafer. (b) An oblique-incident laser-scattering system avoids the specular beam, but also avoids the higher-angle non-specular light and collects light close to the wafer horizon and to the side of the incident and reflected specular beam.

Many unpatterned inspection systems in use today scan the laser spot in the x-direction while the wafer moves in the y-direction. The scattered light is collected either in a large solid angle near the specular beam (for normal-incidence systems), or to the side of the wafer close to the horizon (for oblique-incidence systems). The beam spot is typically 10s or 100s of micrometers across, and every defect is sampled several times by several sweeps of the laser spot.

Another successful commercial unpatterned inspection system uses a markedly different optical design. For improved sensitivity and uniformity the entire incident and collection optics are held stationary, while the wafer is rotated and translated beneath the optical system (Fig. 8). The laser spot traverses a spiral path to sample the entire wafer surface. The system has two collection channels that together span almost the entire scattering hemisphere. The collection optics are axially symmetric, allowing very uniform defect capture even for defects that scatter light highly directionally,
like scratches. The system also includes a Nomarski differential interference contrast microscope to distinguish concave from convex defects, and to capture large-scale, low-topography defects such as a surface quality problem called “orange peel.” This inspection system is described in more detail in Ref. 16, and Nomarski microscopy is discussed in Ref. 17.

Figure 8. Schematic of unpatterned wafer inspection system showing dynamic wafer stage, and rotationally symmetric (static) collection optics.

During signal processing the scatter arising from surface roughness or haze is separated from the defect scatter. The resulting information is typically divided into three categories: haze, point defects, and large-area scattering events like scratches. The values reported for the defects include their coordinates, scattering cross-section (μm²) and/or “diameter” (μm). The “diameter” values are calibrated from the scattering cross-sections of populations of polystyrene latex (PSL) spheres of known size, deposited on the film of interest.

Applications. Unpatterned inspection systems are used for the main applications shown in Table 3.
Unpatterned inspection systems are used heavily by silicon manufacturers and IC manufacturers for inspection of bare silicon and blanket films. Silicon manufacturers use the systems to measure the number of particles, pits, scratches, and crystal defects\cite{18,19} and to characterize haze on the wafers.\cite{20,21} In IC manufacturing they are typically used to measure PWP—Particles per Wafer Pass—to characterize particles added by process or metrology tools during wafer processing. From this measurement a tool is qualified for production use and/or monitored using SPC charts to understand if the tool is degrading and causing any defect issues. For example, a process tool may be studied with PWP tests to understand how often the chamber needs to be cleaned, and then monitored with PWP tests for any other abnormal excursions.

**Strengths and Limitations.** See Table 4 for some of the strengths and limitations of defect detection systems.

**Patterned Wafer Inspection Systems.** Patterned-wafer inspection systems may use bright- or dark-field imaging, or dark-field scattering, or any combination of these as their fundamental defect detection technology. The challenges specific to patterned-wafer defect inspection come directly from the presence of pattern near the defects, and from the fact that the types of possible defects are extended to include defects in the pattern itself—bridges, opens, missing vias, etc. Several different system designs exist
among successful commercial inspection systems; these can each be
optimized for sensitivity and throughput using several configurable sys-
tem parameters. Capture probability for a given defect type on a given
layer for a given IC product will vary according to the configuration of
the system and its overall design. Determination of the optimum in-
spection system to detect a range of key defects for a given segment of
the process is best determined experimentally.

Table 4. Strengths and Limitations of Defect Detention Systems for
Unpatterned Wafers

<table>
<thead>
<tr>
<th>Unpatterned Wafer Inspection Systems</th>
<th>Strengths</th>
<th>Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>• Can detect defects as small as 80 nm on bare silicon wafers</td>
<td>• Unpatterned wafers only</td>
</tr>
<tr>
<td></td>
<td>• Excellent sensitivity to particles on smooth and rough blanket films</td>
<td>• Defect must have some type of light-scattering signature to be detected: topography, or change in material properties</td>
</tr>
<tr>
<td></td>
<td>• Can detect crystal defects</td>
<td>• Sizing calibration is based on known polystyrene latex spheres</td>
</tr>
<tr>
<td></td>
<td>• Can measure haze/surface roughness</td>
<td></td>
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<tr>
<td></td>
<td>• Low cost per inspection</td>
<td></td>
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<tr>
<td></td>
<td>• Automated</td>
<td></td>
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<td>• High throughput</td>
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</table>

Bright-field imaging systems work by flood-illuminating an area of
the wafer, then using an objective lens to construct an optical image of that
area from the specular beam reflecting off the surface. The image is
captured by a digital camera, and that image is compared with another
image from a similar area on the wafer. In periodic areas such as memory
cells the compared area may be within the same memory cell; for non-
periodic areas an equivalent area from a neighboring die is used. Differ-
ences between images become candidates for identification as defects.
Dark-field imaging is a similar technique, but instead of utilizing information from the specular beam, the detector is placed away from the specular beam to intercept a fraction of the scattered light. Although both dark-field imaging and dark-field scattering use scattered light to detect defects, dark-field imaging differs in that it preserves the spatial relationships among features illuminated within the spot. Both dark-field techniques should provide similar defect capture probabilities, if angles of incidence and collection (and other system parameters) are comparable.

Dark-field scattering technology for patterned wafer inspection is similar in principle to unpatterned wafer inspection technology except that the scattering signal from the pattern must be managed. In the first patterned wafer inspection systems all signals having a period similar to that of the die spacing were discarded, while all aperiodic signals became candidates for identification as defects. The latest dark-field scattering inspection systems retain all signals above a threshold, then employ a die-to-die comparison algorithm similar to that described above for imaging systems.\[22\]

A critical requirement of all patterned wafer inspection systems is fast and reliable alignment of the wafer to the scan axes. This is necessary for proper implementation of the signal processing algorithms, and this requirement has driven the use of highly precise stages and sophisticated alignment algorithms in these systems.

Applications. Patterned wafer inspection systems were introduced in the 1980s to drive yield enhancement by providing a direct look at defect densities on production wafers. These systems replaced the long-standing tradition of inspection by operators using optical microscopes. Today’s inspection systems are very automated and offer higher throughput than an operator, more repeatable and objective results, and significantly higher detection sensitivity and defect capture.

Patterned wafer inspection systems are used to inspect wafers for defects at any level in the IC manufacturing process. Two main applications of these systems have been discussed previously in this chapter: in-line monitoring and yield learning. Patterned wafer inspection systems are usually integrated closely with data analysis systems, review stations, and automatic defect classification (ADC) to provide an entire system for identifying and eliminating yield-limiting defects, and to monitor the process line to catch defect excursions and drive continuous improvement.

Increasingly, these systems are being used for process equipment monitoring with patterned production wafers. The trend towards reducing the cost of monitor wafers in the fab has led to increased dependence on
production wafer defect data to help determine the defect contribution of process equipment.

**Strengths and Limitations.** See Table 5 for some of the strengths and limitations of defect detection systems.

**Table 5.** Strengths and Limitations of Defect Detection Systems for Patterned Wafers

<table>
<thead>
<tr>
<th>Strengths</th>
<th>Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Can detect defects as small as 0.1 μm on front-end, patterned layers, on product wafers&lt;br&gt;- Techniques exist to reduce noise effects of film nonuniformity and process variation&lt;br&gt;- Automated&lt;br&gt;- Integrated with defect review and classification systems, defect data analysis systems</td>
<td>- Defect must have some type of light-scattering signature to be detected: topography, or change in material properties&lt;br&gt;- Lower throughput than unpatterned inspection systems</td>
</tr>
</tbody>
</table>

### 4.5 Automatic Defect Classification

The main goal of Automatic Defect Classification is to reduce the number of defects that require manual review and classification. ADC incorporates several levels of operation to achieve this. The first level involves the use of clustering algorithms that group together defects with certain spatial signatures, such as scratches. These cluster algorithms are normally also available on the inspection system, providing a first-pass defect classification that happens while the wafer is scanned.
After clusters have been removed a smaller group of defects is left behind to classify. This group can be reduced further by using a data analysis system to compare the current defect map with maps from previous layers, and selecting only defects from the current layer. Next, defects can be removed from the remaining group by considering characteristics stored during inspection, such as defect size. After the data set has been significantly reduced by these techniques, the remaining defects are reviewed and classified automatically or manually, comparing the characteristics of the reviewed image of the defect to information in a database. Manual classification involves having a trained operator compare the microscope image to example images in a defect scrapbook. The remainder of this section describes how this part of the review and classification process can be done automatically, via high-resolution automatic defect classification.

The database used for high-resolution ADC is built by the user and requires multiple example images of each type of defect. Typically 5 to 20 examples of each defect type are needed to construct the database. The system measures the value of each of a number of features describing the defect. For a given defect category, each feature spans a particular range. The set of feature ranges distinguishes one defect category from another. These category features are used as a reference for high-resolution automatic classification of new defects.

After the system has been trained, new defects are classified as follows:

If ADC is on board the inspection system the system already has the wafer aligned and in the system. Otherwise the wafer must be loaded and automatically aligned. Using the coordinates determined by the inspection system, the ADC system drives to a defect’s position and re-detects the defect. The re-detection algorithms are similar to the die-to-die processing discussed previously. Depending on the type of device being inspected, the ADC system will drive to another location within the die that has identical pattern (for example, to another location within the memory array for a DRAM), or will drive to one or two adjacent die to compare the corresponding image(s) and subtract the images to determine the defect image. After the defect has been re-detected, the system compares the values of the features of the defect image to those stored in the database.
The final results include the best match of that defect to a known category, and a number indicating how good the match is between the defect’s particular characteristics and that category’s stored characteristics. Some systems will also show the second-best match for the defect being classified.

**Applications.** Early ADC systems in production-level fab focused on a few specific types of layers in the front-end of the process. Continuing developments in ADC technology have opened up the entire process for automatic defect classification. There are several different types of review stations available with various illumination sources (e.g., optical microscopes, confocal laser-scanning microscopes, scanning electron microscopes), and ADC is available with many of these. ADC with white light and with confocal laser-scanning review stations is being used currently in fabs for classification of defects in both the front end and back end of the process (back end being defined here as all process steps used for forming the metal interconnects that wire together all of the transistors formed in front end processing). Future technology advancements in ADC will see the inclusion of ADC with scanning electron microscopes (SEMs). This will be particularly important as the linewidths of devices decrease, and the identification of defects smaller than 0.2 micron becomes necessary on a regular basis. For further reading on automatic defect classification, please see Ref. 23.

**Strengths and Limitations.** Automatic defect classification reduces the amount of time and resources necessary to do in-line monitoring of the IC process. ADC is available integrated directly with the inspection tool, or separated from the inspection tool in an off-line review station. The former is useful because it minimizes the overall time between when the wafer is loaded, and when the defects are classified. The latter is useful because the inspection tool’s time is not occupied with ADC activities (both creating a database and doing actual ADC), and it can therefore remain dedicated to wafer inspection. (See Table 6.)

ADC using a white-light source provides excellent results on front-end layers. Some challenges arise in the back-end of the process when the topography of the surface of the device is complicated by the presence of many etched layers. In this case consistent autofocus on the top surface can be difficult with a white-light microscope, and this can affect ADC by lowering the rate of successful defect re-detection. Fortunately, ADC results using confocal laser scanning have demonstrated improvements in re-detection rates on back-end layers. These systems have a restricted depth of focus with variable height positioning that can be used to generate a digitized 3-D surface image for automatic defect classification.[24]
Table 6. Strengths and Limitations of ADC Systems

<table>
<thead>
<tr>
<th>Automatic Defect Classification Systems</th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Strengths</strong></td>
<td><strong>Limitations</strong></td>
</tr>
<tr>
<td>• ADC is faster, more repeatable and more accurate than classification by operators: faster time and results</td>
<td>• Images of typical defects in each class need to be acquired for setup</td>
</tr>
<tr>
<td>• White light or laser-confocal ADC can be used to reduce number of defects needing slower SEM review</td>
<td>• Differing defect types must have different appearance to be properly classified</td>
</tr>
<tr>
<td>• Flexibility in platform: available off-line from, or integrated with, the inspection system</td>
<td></td>
</tr>
</tbody>
</table>

4.6 Defect Data Analysis Systems

Data analysis became a more critical part of the defect reduction process with the adoption of automated defect inspection systems, particularly patterned wafer inspection systems. Patterned inspectors resulted in a dramatic increase in the amount of defect data generated for analysis. Defect data analysis systems are now networked multi-user systems that provide access to and analysis of inspection data throughout the fab, and incorporate and correlate defect data with other metrology and parametric measurements such as electrical test results.

The data analysis systems function in several ways:

*Defect data analysis systems manage the information flow and maintain a historical database of inspection, review, and metrology and parametric data throughout the fab.* Data analysis systems usually have a large amount of memory allocated for data coming from all types of inspection systems (data include defect density, size, coordinates, etc.) and from review stations (i.e., defect images and classification information). Typically this flow of information between the tools and the analysis system is automated and requires little or no operator intervention.
Defect data analysis systems provide basic SPC functionality and real-time feedback for in-line monitoring of the process. The systems provide basic graphical analysis such as wafer maps and trend charts. Since the flow of data into the system is automated, the system can be programmed to alert an operator or engineer automatically, and shut down the process equipment, if the density of a given defect type at a particular inspection point in the process exceeds set control limits.

Defect data analysis systems provide capabilities for correlating defect data to yield data. Clustering algorithms group defects based on their spatial relationships on the wafer. Identification of these clusters helps track excursions in defect density—and yield—more intelligently. Clustering algorithms may also help identify the source of the defects, as some process equipment may create defects having a distinct spatial signature. Partitioning analysis helps determine at what layer the defects first arose. This information helps significantly to pinpoint the source of defects. Finally, the capability of correlation of defect information with electrical test sort maps establishes which defect types are yield-limiting.

The output of the data analysis system can be in a variety of formats: wafer maps, Pareto charts or histograms, or tabular reports. These systems are also able to output new wafer map review files with only certain defects included. This may be useful, for example, for reviewing only defects added at a given process layer.

For further reading on defect data analysis systems, see Ref. 25.

GLOSSARY

<p>| ADC | Automatic Defect Classification, a means of categorizing detected events by comparing their digital optical images with reference images. |
| AFM | Atomic Force Microscope, an instrument derived from a Scanning Tunneling Microscope and related to a stylus profilometer, used to form 3-D high resolution topographic images of solid surfaces. |
| ASIC | Application Specific Integrated Circuit. |
| Back end | See BEOL. |
| BCR | Bar Code Reader, used for wafer identification and tracking. |</p>
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEOL</td>
<td>Back End Of Line; the process steps used for forming the metal interconnects that wire together the transistors formed in front end processing.</td>
</tr>
<tr>
<td>Bright-field</td>
<td>Describes a technique based on collection of the specularly reflected light from the sample.</td>
</tr>
<tr>
<td>CCD</td>
<td>Charge Coupled Device; in this context describing a type of digital camera.</td>
</tr>
<tr>
<td>CD</td>
<td>Critical Dimension, or smallest linewidth of a conductive line on an IC.</td>
</tr>
<tr>
<td>CMP</td>
<td>Chemical-Mechanical Polishing, a global planarization technique.</td>
</tr>
<tr>
<td>COO</td>
<td>Cost Of Ownership, a metric used to evaluate semiconductor equipment.</td>
</tr>
<tr>
<td>C-V</td>
<td>Capacitance-Voltage.</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical Vapor Deposition, a technique commonly used to deposit dielectric layers.</td>
</tr>
<tr>
<td>Dark-field</td>
<td>Describes a technique based on collection of the non-specularly reflected (scattered) light from the sample.</td>
</tr>
<tr>
<td>Defectivity</td>
<td>The quality of having defects; the number of defects on the wafer.</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic Random Access Memory, a type of semiconductor memory.</td>
</tr>
<tr>
<td>Electromigration</td>
<td>The process resulting in current-induced open circuit failure in metal interconnect lines.</td>
</tr>
<tr>
<td>FTIR</td>
<td>Fourier Transform InfraRed spectroscopy, used for chemical compositional analysis.</td>
</tr>
<tr>
<td>GEM</td>
<td>Generic Equipment Model, a communications standard used for factory automation (newer than SECS).</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit.</td>
</tr>
<tr>
<td>In-line</td>
<td>Relating to measurements that occur in a processing tool, outside of the process chamber.</td>
</tr>
<tr>
<td>In situ</td>
<td>Relating to measurements that occur within a process chamber.</td>
</tr>
<tr>
<td>Term</td>
<td>Description</td>
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<tr>
<td>Junction</td>
<td>The point at which the conductivity changes from p-type to n-type or vice versa.</td>
</tr>
<tr>
<td>MOCVD</td>
<td>Metal-Organic CVD, used for depositing certain conductive layers.</td>
</tr>
<tr>
<td>OCR</td>
<td>Optical Character Recognition, used for wafer identification and tracking.</td>
</tr>
<tr>
<td>OEE</td>
<td>Overall Equipment Effectiveness, a metric used to evaluate semiconductor equipment (newer than COO).</td>
</tr>
<tr>
<td>Off-line</td>
<td>Relating to measurements that occur on a stand-alone metrology system in the manufacturing area.</td>
</tr>
<tr>
<td>Nomarski</td>
<td>Differential interference contrast microscope, a technique for detecting the phase difference between two adjacent points on the sample. This method uses a birefringent crystal, and polarized light, to separate the incident light into two adjacent beams, and determines the phase difference between the beams through interference.</td>
</tr>
<tr>
<td>Pareto analysis</td>
<td>A list of items contributing to a problem communicating the order of their importance.</td>
</tr>
<tr>
<td>PMT</td>
<td>Photo Multiplier Tube, a type of light detector chosen for its fast response, that quantifies the amount of light striking its active area per unit time.</td>
</tr>
<tr>
<td>PSL</td>
<td>PolyStyrene Latex sphere, a standard used to characterize the defect capture performance of defect inspection systems.</td>
</tr>
<tr>
<td>PVD</td>
<td>Physical Vapor Deposition, commonly used to form metal interconnects.</td>
</tr>
<tr>
<td>RC</td>
<td>Resistive-Capacitive, a time delay constant that affects chip operation speed.</td>
</tr>
<tr>
<td>Recipe</td>
<td>An electronic file of system parameter values used to control semiconductor processing or metrology equipment.</td>
</tr>
<tr>
<td>RI</td>
<td>Refractive Index, the ratio of speed of light in a vacuum to speed of light in a material.</td>
</tr>
<tr>
<td>Term</td>
<td>Definition</td>
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<tr>
<td>$R_p, R_s$</td>
<td>The Fresnel reflection coefficients, $p$ and $s$ polarized.</td>
</tr>
<tr>
<td>RTDC</td>
<td>Real Time Defect Classification; a first pass defect classification that uses only information collected during defect inspection, such as intensity, size and spatial distribution of collections of defects $s$ and $p$ polarization, the perpendicular and parallel components (respectively) of the polarization vector.</td>
</tr>
<tr>
<td>SECS</td>
<td>Semiconductor Equipment Communications Standard, used for factory automation.</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope; uses an electron beam to produce very highly magnified images. Used for surface viewing and cross sectional analysis of device dimensions.</td>
</tr>
<tr>
<td>Slurry</td>
<td>An abrasive suspension of hard particles in a viscous chemical solution used in chemical-mechanical polishing.</td>
</tr>
<tr>
<td>SIMS</td>
<td>Secondary Ion Mass Spectrometry, used for characterizing dopant and impurity distribution with depth profiles.</td>
</tr>
<tr>
<td>Solid angle</td>
<td>The 3-dimensional equivalent of angle, often defined by azimuth and elevation.</td>
</tr>
<tr>
<td>SPC</td>
<td>Statistical Process Control, a method of tracking the variations in process parameters to help identify out of control situations.</td>
</tr>
<tr>
<td>SRP</td>
<td>Spreading Resistance Probe, used for characterizing dopant distribution with depth profiles.</td>
</tr>
<tr>
<td>Stoichiometry</td>
<td>The chemical combination of a material composed of other materials.</td>
</tr>
<tr>
<td>TDI</td>
<td>Time Delay Integration, in this context describing a type of camera.</td>
</tr>
<tr>
<td>Yield</td>
<td>The percentage of wafers or die produced in an operation or process that conform to specifications.</td>
</tr>
</tbody>
</table>
REFERENCES


12. *Non Contact Sheet Resistance Measurements on Low Resistivity Wafers*, KLA-Tencor Applications Note RS–18


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