6.11 ACTIVE PULLUPS

Large valued resistors are difficult to fabricate in VLSI technology. For example, $R_{\square}$ is usually on the order of a few tens of ohms for polysilicon, few hundreds of ohms for diffusion, and few hundredths of an ohm for metal. Fabricating a 10-kΩ resistor using polysilicon would require an area hundreds of times larger than that of a minimum sized transistor. Fortunately, MOSFETs themselves make good high-valued resistors — for the same area, the resistance R_{ON} of a minimum sized MOSFET is significantly higher than that of a resistance made out of other materials, such as polysilicon.

Figure 6.55 shows an inverter constructed out of MOSFETs with M_{pu} serving as an active pullup. The pullup MOSFET has its drain tied to the power supply connection, and thus the drain has a voltage V_S applied with respect to ground. To keep the pullup MOSFET permanently in its ON state, its gate is connected to a second voltage V_A, where V_A is at least one threshold voltage higher that the supply voltage. In other words,

$$V_A > V_S + V_T.$$

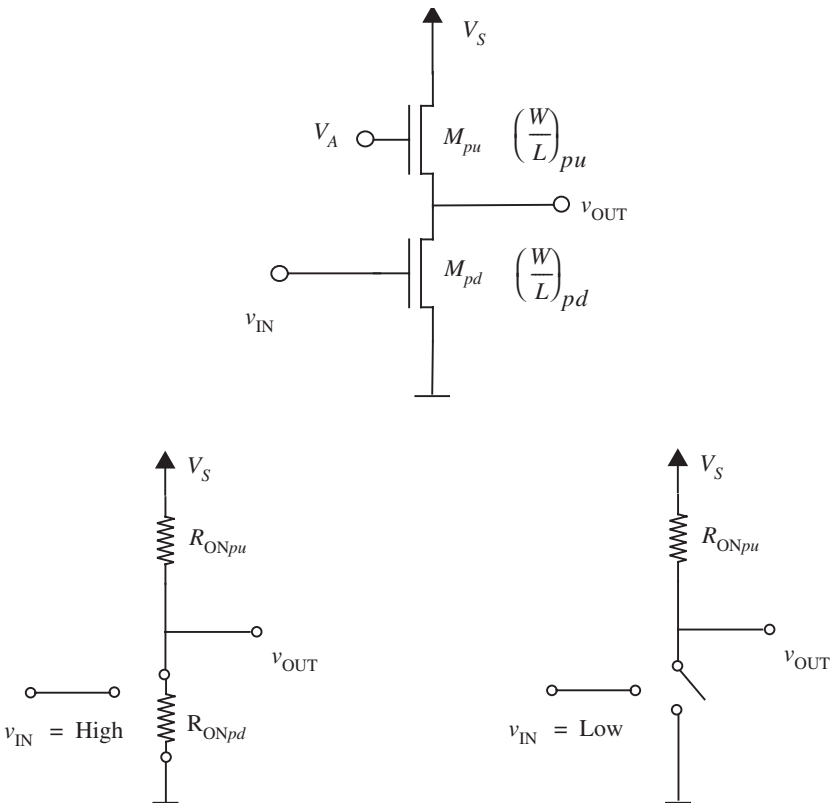

FIGURE 6.55 Logic gate with active pullup. In the circuit, $V_A > V_S + V_T$, so that the pullup MOSFET is always in its ON state.

Let the W/L ratios of the pullup and the pulldown MOSFETs be $(W/L)_{pu}$ and $(W/L)_{pd}$, respectively. Let the corresponding ON-state resistances (according to the SR model) be R_{ONpu} and R_{ONpd}. We also know that

$$R_{\text{ON}} \propto \frac{L}{W}$$

where the constant of proportionality is R_n.[25]

Let us now choose the respective (W/L) ratios so that the inverter satisfies the relationship derived in Equation 6.6, and repeated below for convenience:

$$V_S \frac{R_{\text{ON}}}{R_{\text{ON}} + R_L} < V_T$$

This relationship between the output low voltage of the inverter and the threshold voltage of a MOSFET is necessary for the inverter to be able to drive the MOSFET in another inverter into its OFF state. In the preceding equation, R_L is the resistance of the pullup device, and R_{ON} is the resistance of the pulldown device.

With both an active pullup and an active pulldown,

$$V_T > V_S \frac{1}{1 + \dfrac{R_L}{R_{\text{ON}}}} \tag{6.12}$$

$$> V_S \frac{1}{1 + \dfrac{(L/W)_{pu}}{(L/W)_{pd}}} \tag{6.13}$$

where we have substituted the L/W ratios in place of the resistance values.

25. As mentioned earlier, the MOSFET displays resistive behavior between its drain and its source only when the drain voltage is much smaller than the gate voltage (specifically, $v_{DS} \ll v_{GS} - V_T$). Furthermore, the resistance R_n, and therefore R_{ON}, depends on the value of the applied gate voltage. We will see more appropriate models for MOSFETs in other regions of operation in later chapters. But for now, let us go ahead and use the SR model with a single value for R_n to analyze the active pullup.

For our typical parameters: $V_S = 5$ V and $V_T = 1$ V. Therefore, we get

$$5\frac{1}{1+\frac{(L/W)_{pu}}{(L/W)_{pd}}} < 1 \tag{6.14}$$

$$5 < 1 + \frac{\left(\frac{L}{W}\right)_{pu}}{\left(\frac{L}{W}\right)_{pd}} \tag{6.15}$$

$$4 < \frac{\left(\frac{L}{W}\right)_{pu}}{\left(\frac{L}{W}\right)_{pd}}. \tag{6.16}$$

In other words, we can choose the size of the pullup so its (L/W) ratio is four times that of the pulldown.

EXAMPLE 6.9 SIZING PULLUP DEVICES For a 5-V supply voltage, suppose our static discipline prescribes a $V_{OL} = 0.5$ V. How do we size the pullup MOSFET in Figure 6.56 relative to the pulldown MOSFET to meet the valid output low threshold?

When the pulldown device is on, we know that the output voltage is given by

$$v_{\text{OUT}} = V_S \frac{R_{\text{ON}pd}}{R_{\text{ON}pd} + R_{\text{ON}pu}}.$$

To satisfy the static discipline, we must have $V_{OL} > v_{\text{OUT}}$ when the input is high. Recall that the on-state resistance is proportional to the ratio of the device gate length L and its width W. Thus we have,

$$V_{OL} > v_{\text{OUT}} \tag{6.17}$$

$$> V_S \frac{R_{\text{ON}pd}}{R_{\text{ON}pd} + R_{\text{ON}pu}} \tag{6.18}$$

$$> V_S \frac{(L/W)_{pd}}{(L/W)_{pd} + (L/W)_{pu}} \tag{6.19}$$

$$> 5 \frac{1}{1 + \dfrac{(L/W)_{pu}}{(L/W)_{pd}}}. \tag{6.20}$$

For $V_{OL} = 0.5$ V, it is easy to see that if we choose $\frac{(L/W)_{pu}}{(L/W)_{pd}} > 9$ we will satisfy the static discipline. In other words, if both devices are of the same width W, the pullup device must be sized so its length is nine times that of the pulldown device.

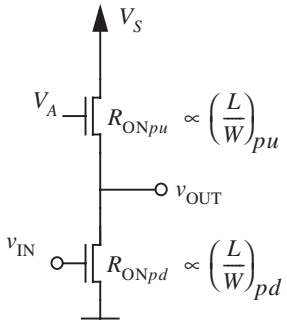

FIGURE 6.56 An inverter with an active pullup.

EXAMPLE 6.10 COMBINATIONAL LOGIC USING MOSFET SWITCHES Let us now rework some of our previous examples using all-MOSFET designs and the SR model. Assume that we need to design our gates such that they satisfy a static discipline with the low output voltage threshold $V_{OL} = V_T^- V$, where V_T is given to be 1 V. Let us design all-MOSFET circuits and let us attempt to make them as small as possible. Assume that the area of the circuit is proportional to the area of the gates ($W \times L$) of the individual MOSFETs. Let us also compute the power dissipated by the circuits. Assume that R_n for the MOSFETs is 1 kΩ.

Let us first consider the expression: $\overline{AB + C + D}$. Figure 6.57 shows a compound gate comprising only MOSFETs that implements this expression. This gate design replaces the load resistor in Figure 6.23 with an active pullup. Our task is to determine the sizes of both the pulldown and the pullup MOSFETs so this gate satisfies the static discipline for $V_{OL} = 1^- V$. Note that the gate must satisfy the static discipline for any combination of inputs.

As we have seen before, the key issue in designing a NMOS logic gate is to choose the relative values of the pullup and the pulldown resistances so that even the highest value for the gate's output low voltage satisfies the V_{OL} constraint. Since we are asked to design the circuit that occupies the least area, and there are more pulldown transistors than pullups, let us start by choosing minimum-sized transistors ($(L/W)_{pd} = 1$) for the pulldown circuit. Therefore the on resistance of an individual pulldown MOSFET is

$$R_{\text{ON}pd} = R_n \left(\frac{L}{W}\right)_{pd} = R_n.$$

The highest value for the output low voltage occurs when the pulldown circuit has its highest resistance. Notice that the pulldown circuit has its largest on-state resistance for an output low when A and B are on, and C and D are off. This largest pulldown resistance is given by the sum of the on-state resistances of the MOSFETs with the A

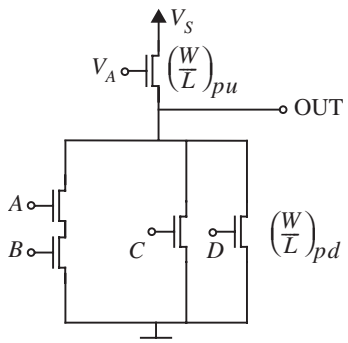

FIGURE 6.57 Transistor-level implementation of $\overline{AB + C + D}$ using an active pullup. In the circuit, $V_A > V_S + V_T$, so that the active pullup is in its ON state at all times.

and B inputs. That is,

$$R_{pdmax} = 2R_{\mathrm{ON}pd} = 2R_n.$$

To satisfy the static discipline, the output voltage of the gate for a logical 0 must be less than V_{OL} for any combination of inputs that can result in a logical 0 at the gate's output. In other words, the highest value for the low output voltage of the gate must be less than V_{OL}, which is given to be V_T^-.

Since the output voltage of the gate is given by

$$V_S \frac{R_{\mathrm{ON}pd}}{R_{\mathrm{ON}pu} + R_{\mathrm{ON}pd}},$$

We can write the following constraint so that the gate satisfies the static discipline for $V_{OL} = V_T^-$:

$$\begin{aligned} V_T &> V_S \frac{R_{\mathrm{ON}pd}}{R_{\mathrm{ON}pu} + R_{\mathrm{ON}pd}} \\ &> V_S \frac{2R_n}{R_{\mathrm{ON}pu} + 2R_n} \\ &> V_S \frac{2R_n}{R_n \left(\frac{L}{W}\right)_{pu} + 2R_n} \\ &> V_S \frac{2}{\left(\frac{L}{W}\right)_{pu} + 2}. \end{aligned}$$

For $V_S = 5$ V and $V_T = 1$ V, the previous constraint simplifies to

$$\left(\frac{L}{W}\right)_{pu} > 8.$$

In other words, the L/W ratio of the pullup must be chosen to be greater than 8. Thus the resistance of the pullup is $8R_n$.

Let us now compute the power dissipated by the circuit. The maximum amount of power is dissipated when the resistance of the pulldown circuit is a minimum. This happens when $A = 1$, $B = 1$, $C = 1$, and $D = 1$. Recalling that the resistances of each of the pulldowns is R_n and that of the pullup is $8R_n$,

$$\begin{aligned} P_{max} &= \frac{V_S^2}{8R_n + 2R_n \| R_n \| R_n} \\ &= 3 \times 10^{-3} \text{ W}. \end{aligned}$$

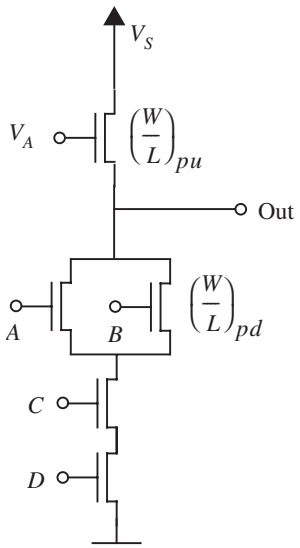

FIGURE 6.58 Transistor-level implementation of $\overline{(A+B)CD}$ using an active pullup. In the circuit, $V_A > V_S + V_T$.

We can also design a circuit for the expression $\overline{(A+B)CD}$ in like manner as depicted in Figure 6.58. In this design, the maximum on-state resistance of the pulldown circuit for an output low is achieved when both C and D is high and only one of A and B is high. The corresponding maximum on-state resistance of the pulldown (assuming minimum sized transistors) is $3R_n$.

As before, the pullup must be designed to have four times the resistance of the pulldown. Since the pulldown circuit has resistance $3R_n$, the L/W ratio of the pullup transistor must be chosen as

$$(L/W)_{pu} = 4 \times (L/W)_{pd} = 4 \times 3 = 12.$$

We can also calculate the maximum power dissipated by computing the minimum resistance in the current path. The minimum resistance occurs when all inputs are high. Thus the total resistance in the current path is given by

$$R_{pu} + R_{pd} = 12R_n + 2R_n + (R_n \| R_n) = 14.5R_n.$$

The corresponding power dissipation is[26]

$$P_{max} = \frac{V_s^2}{14.5R_n} = 1.7 \times 10^{-3} \text{ W}.$$

26. We note that a milliwatt of power per gate would cause today's million-gate circuits on a VLSI chip to dissipate a thousand watts of power! Because VLSI chips cannot dissipate more than few tens of watts without esoteric packaging technologies, modern VLSI chips use another form of logic called CMOS involving both n-channel and the complementary p-channel MOSFETs. We will study this technology in Chapter 11.